Onyx 57791 and 58791

1 or 2 L-band RF tuners, 2-or 4-channel 500 MHz A/D 6U VPX board with Virtex-7 FPGA

Complete radar and software radio interface solution

- Radar and software radio receiver
- Communications receiver
- Analog signal interface for data recording
- Wideband data acquisition
- Remote monitoring
- Sensor interfaces

The 57791 and the 58791 consist of one or two 71791 XMC modules mounted on a VPX carrier board. The 57791 is a 6U board with one 71791 module while the 58791 is a 6U board with two XMC modules rather than one.

They include one or two L-Band RF tuners, two or four A/Ds and four or eight banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, these models include general purpose and gigabit serial connectors for application-specific I/O.

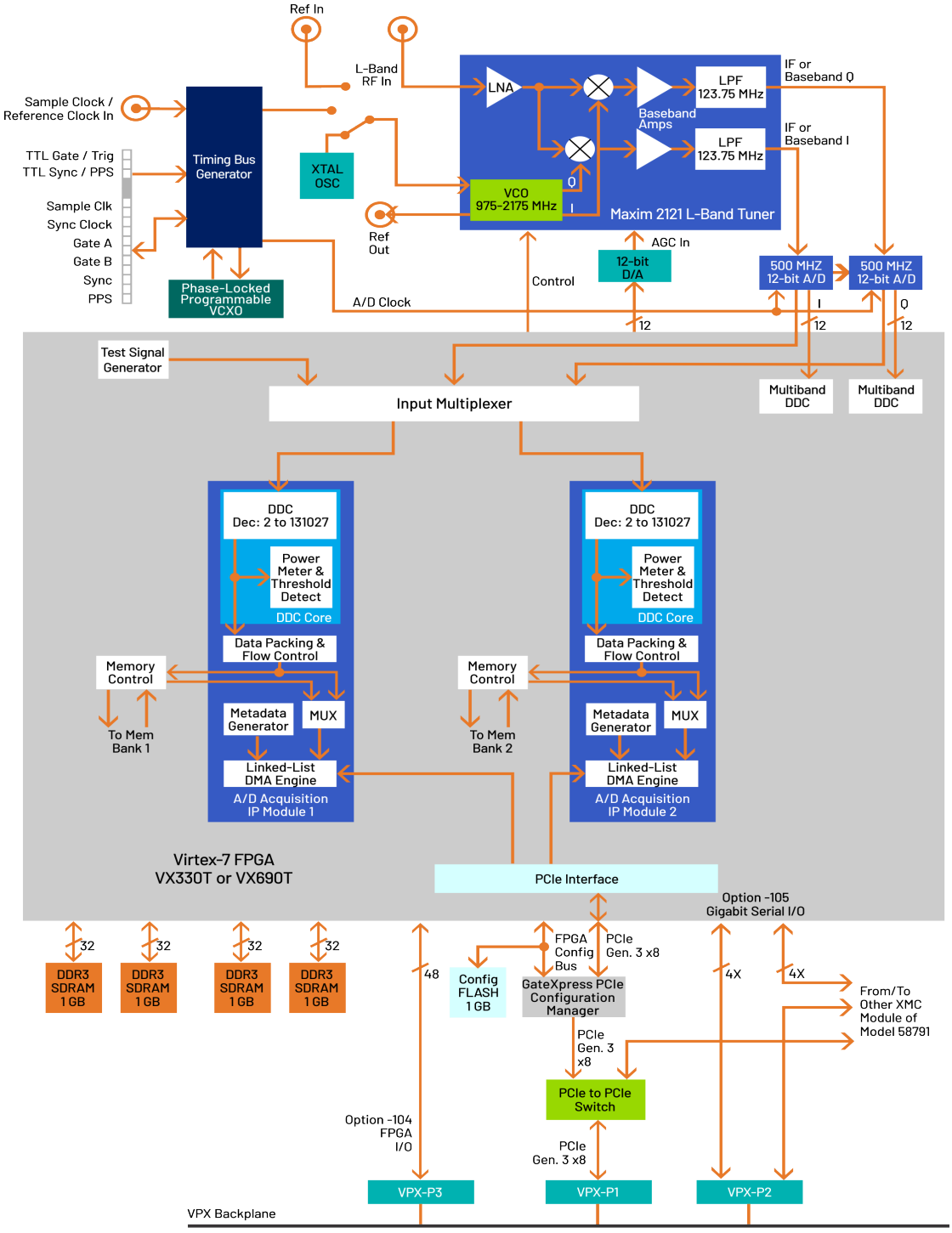
FEATURES

- Accepts RF signals from 925 MHz to 2175 MHz
- GateXpress® supports dynamic FPGA reconfiguration across PCIe
- One or two programmable LNA handles L-Band input signal levels from -50 dBm to +10 dBm
- Programmable analog downconverter provides IF or I+Q baseband signals at up to 123 MHz
- Two or four 500 MHz 12-bit A/Ds digitize IF or I+Q signals synchronously; optional: 400 MHz 14-bit A/Ds
- Two or four FPGA-based multiband DDCs
- Xilinx® Virtex®-7 VX330T or VX690T
- Four or eight GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Xilinx® Virtex®-7 FPGA for custom I/O

BLOCK DIAGRAM

Click on a block for more information.

Block diagram 57791 shows half of the 58791. All resources are actually double of what is shown except for the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5.



THE ONYX ARCHITECTURE

The Pentek Onyx Architecture features one or two Virtex-7 FPGAs. All of the board's data and control paths are accessible by the FPGA, to support factory-installed functions including data acquisition, control, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

The factory-installed functions include two or four A/D acquisition IP modules, four or eight DDR3 memory controllers, two or four DDCs (digital downconverters), RF tuner controllers, one or two clock and synchronization generators, one or two test signal generators, and a Gen 3 PCIe interface.

These models can operate as complete turnkey solutions with no need to develop FPGA IP.

EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. The GateFlow FPGA Design Kits include all of the factory-installed modules as document source code. Developers can integrate their own IP with the factory-installed functions or use the GateFlow kit to completely replace the IP with their own.

XILINX VIRTEX-7 FPGA

The Xilinx Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

A/D CONVERTERS AND DDCS

The analog tuner outputs are digitized by two or four Texas Inst. ADS5463 500 MHz 12-bit A/D converters. Another benefit of using the preferred IF analog output mode is that two or four independent A/D and DDC channels are now available for digitizing and downconverting signals with different center frequencies and bandwidths.

A/D ACQUISITION IP MODULES

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer automatically adapts to the length of the acquisition gate. This is extremely useful in applications where acquisition is driven by an external gate of unknown or variable length.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP CORES

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_S, where f_S is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting two different output bandwidths. Decimations can be set from 2 to 131,072 to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_S/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_S/N.

RF TUNER STAGE

A front panel SSMC connector accepts L-band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). The Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA, a PLL (phase-locked loop) synthesized local oscillator, quadrature (I+Q) downconverting mixers, output low pass filters, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to one of three selectable frequency references: the timing generator output, an external reference input between 12 and 30 MHz, or an on-board crystal oscillator.

Together, the RF LNA and baseband amplifiers accommodate input signal levels from –50 dBm to +10 dBm. The integrated low pass filter has a 3 dB bandwidth of 123.75 MHz.

For best performance, the analog outputs of the MAX2121 should be used in the IF mode instead of the analog baseband I+Q mode. In this case, the IF signal is digitized by the A/D converter and then delivered to the DDC to produce perfectly balanced digital I+Q complex samples, 16 bits each.

A/D CLOCKING AND SYNCHRONIZATION

One or two internal timing generators provide all timing, gating, triggering and synchronization functions required by the A/D converters. They also serve as optional sources for the L-Band tuner references.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/ trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

MEMORY RESOURCES

The architecture of these models supports four or eight independent 1 GB DDR3 SDRAMs for transient capture and buffering data to PCIe.

The factory-installed A/D acquisition modules use memory banks 1 & 2. Banks 3 & 4 can be used to support custom user-installed IP within the FPGA .

PCI EXPRESS INTERFACE

Models 57791 and 58791 include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

GATEXPRESS FOR FPGA CONFIGURATION

The Onyx architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting. Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image:

- The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.
- The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.
- The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without a host computer reset to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

READYFLOW

Mercury provides ReadyFlow® BSPs (Board Support Packages) for all Cobalt, Onyx, and Flexor products. Available for both Linux and Windows, these packages:

- Provide a path for quick start-up through application completion
- Allow programming at high, intermediate and low levels to meet various needs
- Are illustrated with numerous examples
- Include complete documentation and definitions of all functions
- Include library and example source code.

ReadyFlow BSPs contain C-language examples that can be used to demonstrate the capabilities of Cobalt, Onyx, and Flexor products. These programming examples will help you get an immediate start on writing your own application. They provide sample code that is known to work, giving you a means of verifying that your board set is operational.

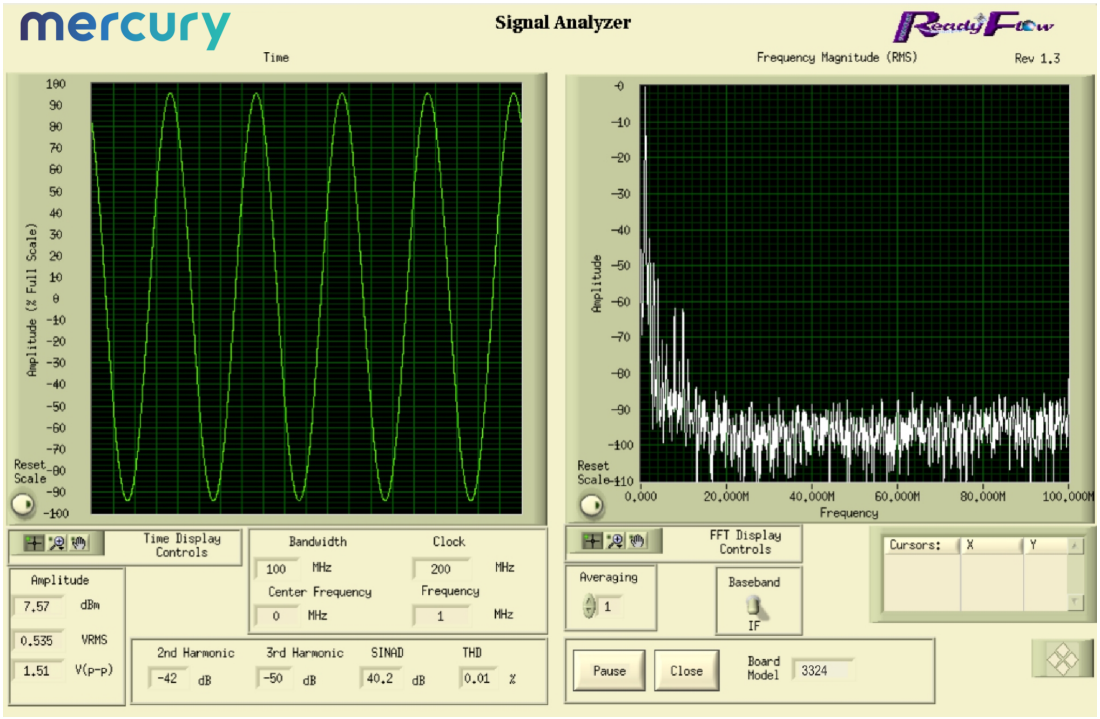
COMMAND LINE INTERFACE

The Command Line Interface provides access to pre-compiled executable examples that operate the hardware right out of the box, without the need to write any code. Board-specific hardware operating arguments can be entered in the command line to control parameters: number of channels to enable, sample clock frequency, data transfer size, reference clock frequency, reference clock source, etc.

The Command Line Interface can be used to call an example application from within a larger user application to control the hardware, and parameter arguments are passed to the application for execution. Functions that control data acquisition automatically save captured data to a pre-named host file or are routed to the Signal Analyzer example function for display.

SIGNAL ANALYZER

When used with the Command Line Interface, the Signal Analyzer allows users to immediately start acquiring and displaying A/D data. A full-featured analysis tool, the Signal Analyzer displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD, and SINAD. Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals.



GATEFLOW

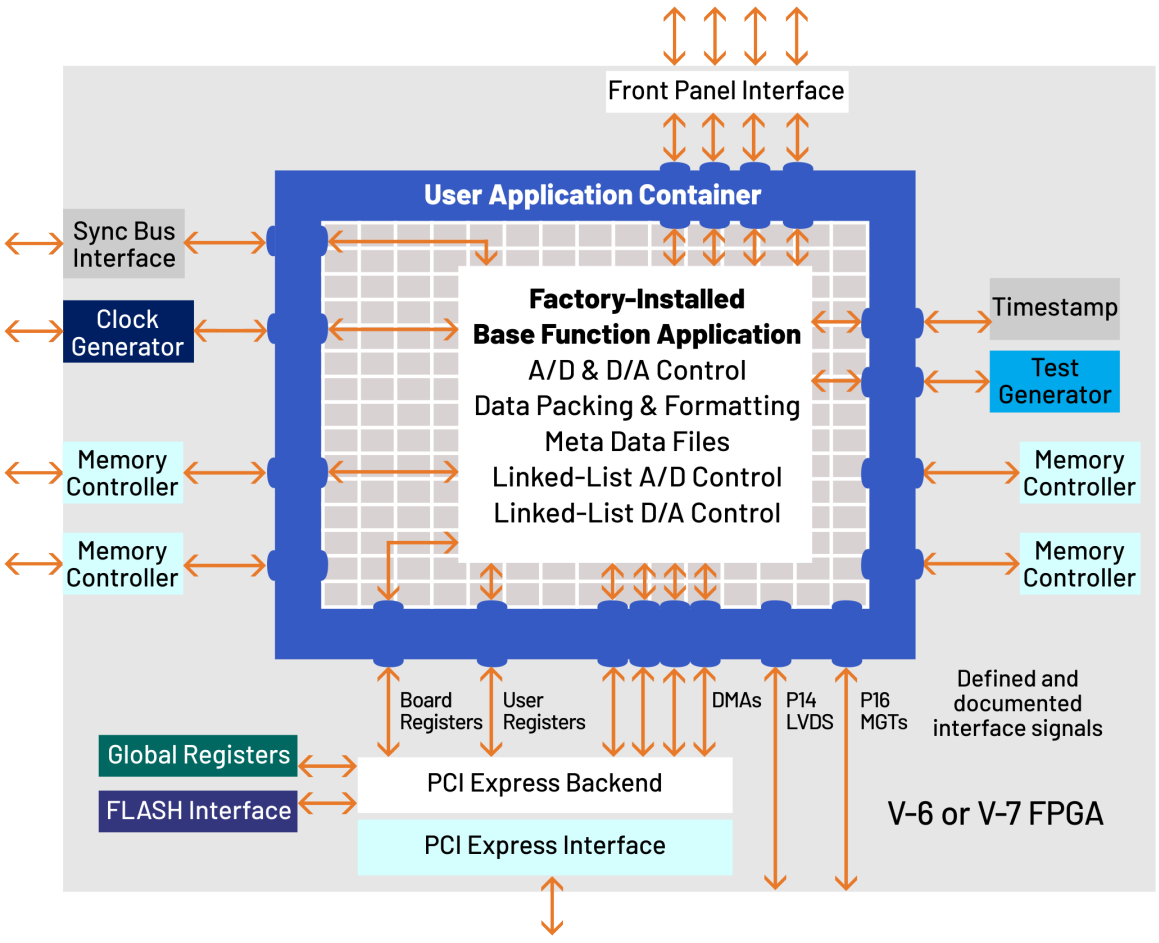
The GateFlow® FPGA Design Kit (FDK) allows the user to modify, replace and extend the standard installed functions in the FPGA to incorporate special modes of operation, new control structures, and specialized signal-processing algorithms.

The Cobalt (Virtex-6), Onyx (Virtex-7), and Flexor (Virtex-7) architectures configure the FPGA with standard factory-supplied interfaces including memory controllers, DMA engines, A/D and D/A interfaces, timing and synchronization structures, triggering and gating logic, time stamping and header tagging, data formatting engines, and the PCIe interface. These resources are connected to the User Application Container using well-defined ports that present easy-to-use data and control signals, effectively abstracting the lower-level details of the hardware.

The User Application Container

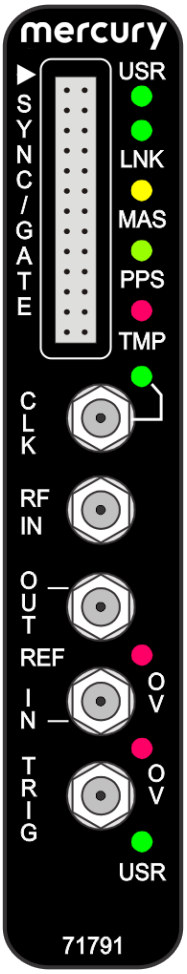
Shown below is the FPGA block diagram of a typical Cobalt, Onyx or Flexor module. The User Application Container holds a collection of different installed IP modules connected to the various interfaces through the standard ports surrounding the container. The specific IP modules for each product are described in further detail in the datasheet of that product.

The GateFlow FDK provides a complete Xilinx's ISE or Vivado project folder containing all the files necessary for the FPGA developer to recompile the entire project with or without any required changes. VHDL source code for each IP module provides excellent examples of how the IP modules work, how they might be modified, and how they might be replaced with custom IP to implement a specific function.



FRONT PANEL CONNECTIONS

The XMC front panel includes five SSMC coaxial connectors and a 26-pin Sync Bus connector for input/output of clock, trigger and analog signals. The front panel also includes nine LEDs.



- **Sync Bus Connector:** The 26-pin Sync Bus front panel connector, labeled **SYNC/GATE**, provides clock, sync, and gate input/output pins for the LVPECL Sync Bus.
- **User LED:** The green **USR** LED is for user applications.
- **Link LED:** The green **LNK** LED blinks when a valid link has been established over the PCIe interface.
- **MAS LED:** The yellow **MAS** LED illuminates when this model is the Sync Bus Master.
- **PPS LED:** The green **PPS** LED illuminates when a valid PPS signal is detected. The LED will blink at the rate of the PPS signal.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the PCB.
- **Clock Input Connector:** One SSMC coaxial connector, labeled **CLK**, for input of an external sample clock.
- **Clock LED:** The green **CLK** LED illuminates when a valid sample clock signal is detected.
- **Reference Clock Input Connector:** One SSMC coaxial connector for a RF analog signal input, labeled **RF IN.**
- **Reference Clock Output Connector:** One SSMC coaxial connector for a tuner reference clock output, labeled **REF OUT.**
- **Analog Signal Input Connector:** One SSMC coaxial connector, labeled **REF IN**, is for a tuner reference clock input.
- **ADC Overload LEDs:** Two red **OV** (overload) LEDs for each A/D channel.
- **Trigger Input Connector:** The SSMC coaxial connector labeled **TRIG** is for input of an external trigger or gate signal. The signal must be a LVTTL signal.
- **User LED:** One green **USR** LED for user applications.

SPECIFICATIONS

57791: 1 L-Band Tuner, 2 A/Ds, 2 DDCs, 1 FPGA

58791: 2 L-Band Tuners, 4 A/Ds, 4 DDCs, 2 FPGAs

Front Panel Analog Signal Inputs (1 or 2)

Connector: Front panel female SSMC

Impedance: 50 ohms

L-Band Tuner (1 or 2)

Type: Maxim MAX2121

Input Frequency Range: 925 MHz to 2175 MHz

Monolithic VCO Phase Noise: –97 dBc/Hz at 10 kHz

Fractional-N PLL Synthesizer: freqVCO = (N.F.) x $freq_{REF}$ where integer N = 19 to 251 and fractional F is a 20-bit binary value

PLL Reference ($freq_{REF}$): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz

LNA Gain: 60 dB range, controlled by a programmable 12-bit D/A converter

Usable Full-Scale Input Range: –50 dBm to +10 dBm

Baseband Low Pass Filter: 3 dB cutoff frequency: 123.75 MHz

A/D Converters (2 or 4)

Type: Texas Instruments ADS5463

Sampling Rate: 10 MHz to 500 MHz

Resolution: 12 bits

Option -014: 400 MHz, 14-bit A/Ds

Sample Clock Sources (1 or 2)

On-board timing generator/synthesizer

A/D Clock Synthesizer (1 or 2)

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

Timing Generator External Clock Input (1 or 2)

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus (1 or 2)

26-pin front panel connector LVPECL bus includes, clock/ sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/ PPS inputs

External Trigger Input (2 or 4)

Type: Front panel female SSMC connector, LVTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)

- Standard: Xilinx Virtex-7 XC7VX330T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O

- Option -104: Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57791; P3 and P5, Model 58791
- Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57791; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58791

Memory Banks (4 or 8)

Type: DDR3 SDRAM

Size: Four banks, 1 GB each

Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3*: x4 or x8

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: 3U VPX

- Depth: 170.6 mm (6.717 in.)
- Height: 100 mm (3.937 in.)

Weight

- VPX Carrier: 110 grams (3.9 oz.);
- XMC Module: Approximately 400 grams (14 oz.) with 2-slot heatsink

ORDERING INFORMATION

Model	Description
57791	L-Band RF Tuner with 2-Channel 500 MHz A/D with DDCs and Virtex-7 FPGA - 6U VPX
58791	Two L-Band RF Tuners with 4-Channel 500 MHz A/D with DDCs and two Virtex-7 FPGAs - 6U VPX

Options	Description
-014	400 MHz, 14-bit A/Ds
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O between the FPGA and P3 connector, 57791; P3 and P5 connectors, 58791
-105	Gigabit link between the FPGA and P2 connector, 57791; gigabit links from each FPGA to P2 connector, 78791
-702	Air-cooled, Level 2
-763	Conduction-cooled, Level 3

Contact Mercury for compatible option combinations.

ACCESSORY PRODUCTS

Model	Description
2171	Cable Kit: SSMC to SMA

FORM FACTORS

Onyx products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Onyx Model 71791 XMC (L-Band RF Tuner and 2-Channel 500 MHz A/D with Virtex-7 FPGA) has the following variants:

Model	
52791	3U VPX board (single XMC)
57791	6U VPX board (single XMC)
58791	6U VPX board (dual XMC)
71791	XMC module
78791	PCIe board (single XMC)

DEVELOPMENT SYSTEMS

Mercury offers development systems for Onyx products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Onyx boards. Please contact Mercury to configure a system that matches your requirements.

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