Cobalt 52630

1 GHz A/D and D/A 3U VPX boards with Virtex-6 FPGA

Complete radar and software radio interface solution

- Radar and communication receiver and transmitter
- Electronic Warfare transponder
- Waveform signal generator
- Wideband data acquisition
- Remote monitoring
- Sensor interfaces

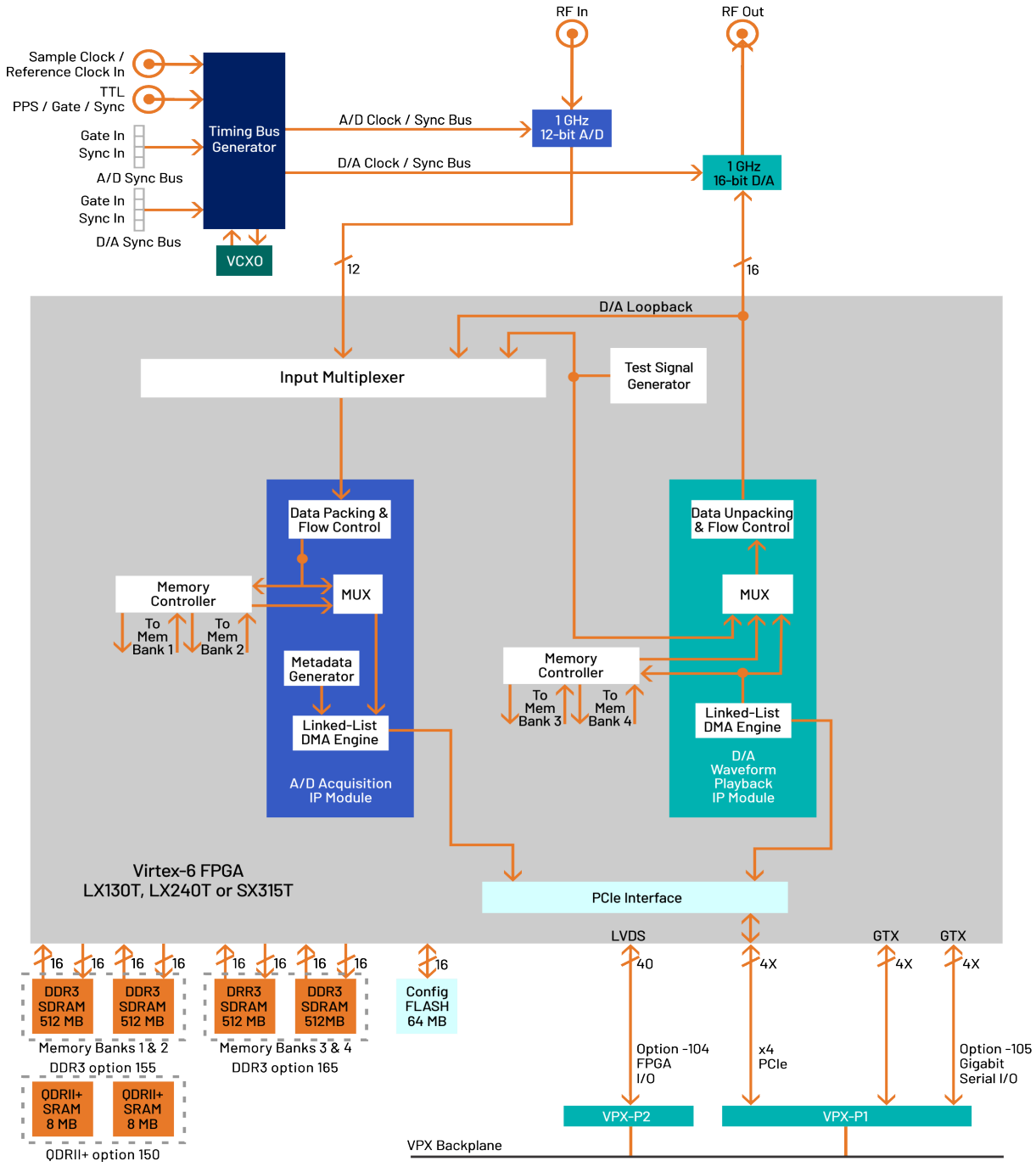
The 52630 is a high-speed data converter, suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution. It includes 1 GHz A/D and D/A converters and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

FEATURES

- Supports Xilinx® Virtex®-6 LXT and SXT FPGA
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- Up to 2 GB of DDR3 SDRAM or 16 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multimodule synchronization
- Optional LVDS connections to the FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with VITA-46, VITA-48 and VITA-65 (OpenVPX™ Specification)
- Ruggedized and conduction-cooled versions available

52630 BLOCK DIAGRAMS

Click on a block for more information.



THE COBALT ARCHITECTURE

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52630 factory-installed functions include an A/D acquisition and a D/A wave-form playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the model to operate as a complete turnkey solution, without the need to develop any FPGA IP.

EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. The GateFlow FPGA Design Kits include all of the factory-installed modules as document source code. Developers can integrate their own IP with the factory-installed functions or use the GateFlow kit to completely replace the IP with their own.

XILINX VIRTEX-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

A/D CONVERTER STAGE

The board's analog interface accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other resources.

A/D ACQUISITION MODULES

The 52630 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Play-back IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A WAVEFORM PLAYBACK IP MODULE

The Model 52630 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

D/A CONVERTER STAGE

The 52630 features a Texas Instruments DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

CLOCKING AND SYNCHRONIZATION

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board's sync and gate/trigger signals.

The Mercury 5292 and 9192 Cobalt Synchronizers can drive multiple 52630 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

MEMORY RESOURCES

The 52630 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of memory for many other purposes.

PCI EXPRESS INTERFACE

The 52630 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

READYFLOW

Mercury provides ReadyFlow® BSPs (Board Support Packages) for all Cobalt, Onyx, and Flexor products. Available for both Linux and Windows, these packages:

- Provide a path for quick start-up through application completion
- Allow programming at high, intermediate and low levels to meet various needs
- Are illustrated with numerous examples
- Include complete documentation and definitions of all functions
- Include library and example source code.

ReadyFlow BSPs contain C-language examples that can be used to demonstrate the capabilities of Cobalt, Onyx, and Flexor products. These programming examples will help you get an immediate start on writing your own application. They provide sample code that is known to work, giving you a means of verifying that your board set is operational.

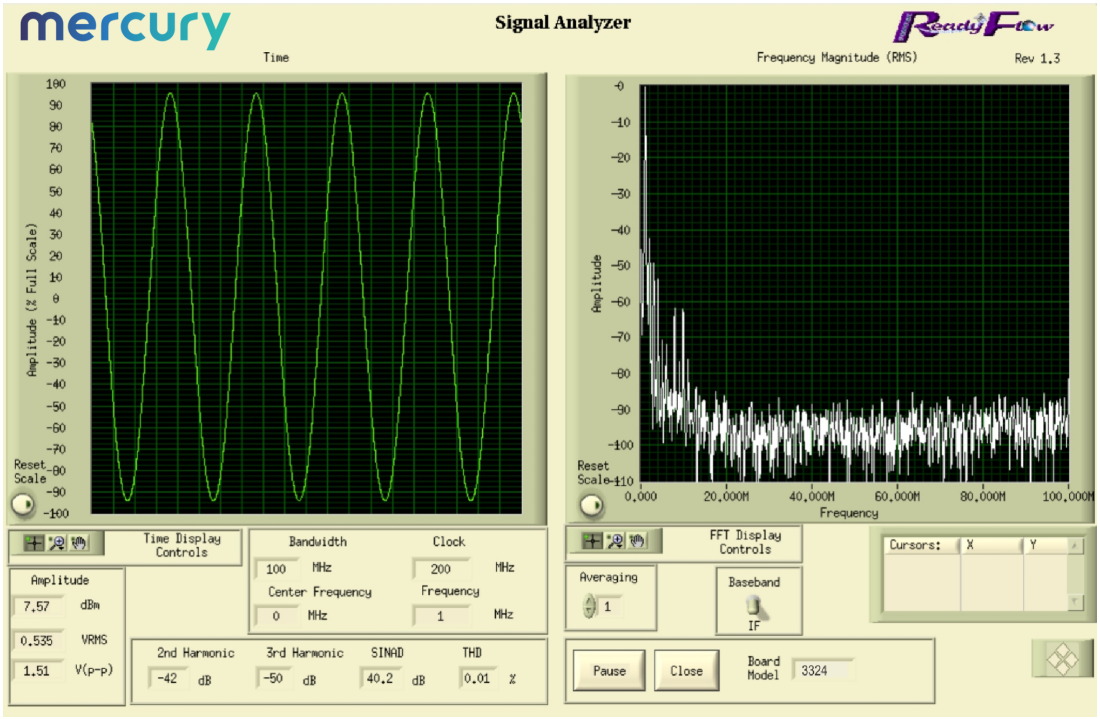
COMMAND LINE INTERFACE

The Command Line Interface provides access to pre-compiled executable examples that operate the hardware right out of the box, without the need to write any code. Board-specific hardware operating arguments can be entered in the command line to control parameters: number of channels to enable, sample clock frequency, data transfer size, reference clock frequency, reference clock source, etc.

The Command Line Interface can be used to call an example application from within a larger user application to control the hardware, and parameter arguments are passed to the application for execution. Functions that control data acquisition automatically save captured data to a pre-named host file or are routed to the Signal Analyzer example function for display.

SIGNAL ANALYZER

When used with the Command Line Interface, the Signal Analyzer allows users to immediately start acquiring and displaying A/D data. A full-featured analysis tool, the Signal Analyzer displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD, and SINAD. Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals.



GATEFLOW

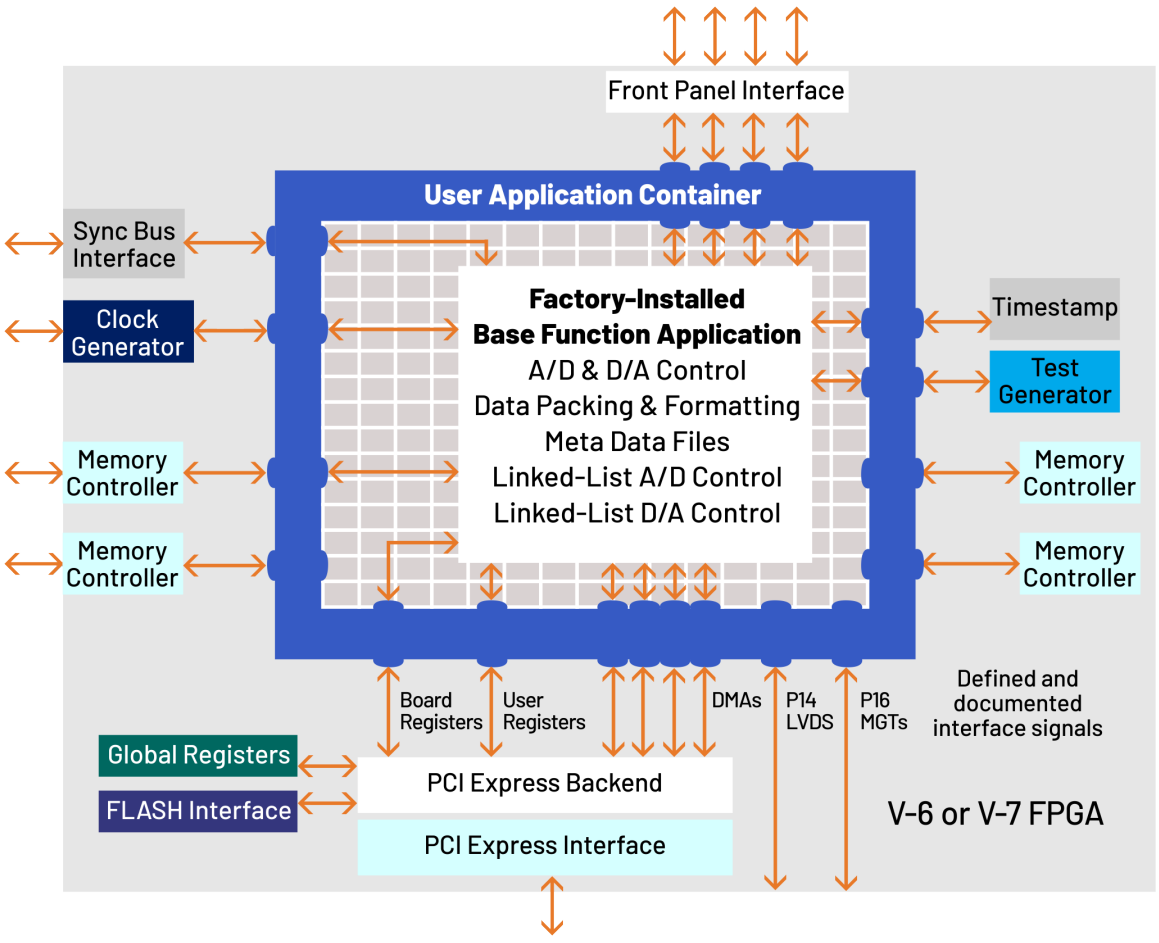
The GateFlow® FPGA Design Kit (FDK) allows the user to modify, replace and extend the standard installed functions in the FPGA to incorporate special modes of operation, new control structures, and specialized signal-processing algorithms.

The Cobalt (Virtex-6), Onyx (Virtex-7), and Flexor (Virtex-7) architectures configure the FPGA with standard factory-supplied interfaces including memory controllers, DMA engines, A/D and D/A interfaces, timing and synchronization structures, triggering and gating logic, time stamping and header tagging, data formatting engines, and the PCIe interface. These resources are connected to the User Application Container using well-defined ports that present easy-to-use data and control signals, effectively abstracting the lower-level details of the hardware.

The User Application Container

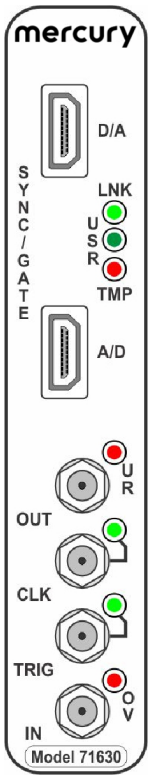
Shown below is the FPGA block diagram of a typical Cobalt, Onyx or Flexor module. The User Application Container holds a collection of different installed IP modules connected to the various interfaces through the standard ports surrounding the container. The specific IP modules for each product are described in further detail in the datasheet of that product.

The GateFlow FDK provides a complete Xilinx's ISE or Vivado project folder containing all the files necessary for the FPGA developer to recompile the entire project with or without any required changes. VHDL source code for each IP module provides excellent examples of how the IP modules work, how they might be modified, and how they might be replaced with custom IP to implement a specific function.



FRONT PANEL CONNECTIONS

The XMC front panel includes two 19-pin µSync connectors, and four SSMC coaxial connectors for input/output of timing and analog signals. The front panel also includes seven LEDs.



- **Sync Bus Connector:** Two 19-pin Sync Bus front panel connectors, labeled **SYNC/GATE**, provide sync, and gate input signals pins for the Sync Bus. The top connector, labeled **D/A** is for DAC timing inputs and the lower connector, labeled **A/D** is for ADC timing inputs.
- **Link LED:** The green **LNK** LED illuminates when a valid link has been established over the PCIe interface
- **User LED:** The green **USR** LED is for user applications.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the printed circuit board (PCB).
- **DAC Underrun LED:** There is one red **UR** (underrun) LED for the D/A output. This LED illuminates when the DAC5681Z FIFO is out of data.
- **Analog Output Connector:** The one SSMC coaxial connect, labeled **OUT**, is for analog signal output from the DAC 5681Z. It is driven by a RF transfer into 50Ω output impedance.
- **Clock Input Connector:** One SSMC coaxial connector, labeled **CLK**, is for input of an external sample clock.
- **Clock LED:** The green **CLK** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed. It is to the right of the **CLK** output
- **Analog Output Connector:** One SSMC coaxial connector, labeled **OUT** for the DAC5681Z output.
- **Trigger Input Connector:** One SSMC coaxial connector, labeled **TRIG** for input of an external gate or trigger signal.
- **PPS LED:** The green LED to the right of the TRIG input illuminates when a valid PPS sign is detected. The LED will blink at the rate of the PPS signal.
- **Analog Input Connector:** One SSMC coaxial connector, labeled **IN** for the ADS5400 input channel.
- **ADC Overload LED:** The red **OV** (overload) LED indicates either an overload in the ADS5400 or an ADC FIFO overrun.

SPECIFICATIONS

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter

Type: Texas Instruments ADS5400

Sampling Rate: 100 MHz to 1 GHz

Resolution: 12 bits

D/A Converter

Type: Texas Instruments DAC5681Z

Input Data Rate: 1 GHz max.

Interpolation Filter: bypass, 2x or 4x

Output Sampling Rate: 1 GHz max.

Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources

On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO or front panel external clock

VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz

Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock

Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

Timing Bus

19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input

Type: Front panel female SSMC connector, LVTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- Standard: Xilinx Virtex-6 XC6VLX130T-2
- Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O

- Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory

- Option 150: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI Express Interface

PCI Express Bus: Gen. 1 or Gen. 2: x4

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: Standard 3U VPX

- Depth: 170.6 mm (6.717 in.)
- Height: 100 mm (3.94 in.)

Weight: VPX Carrier: 110 grams (3.9 oz.); XMC Module: Approximately 14 oz. (400 grams)

ORDERING INFORMATION

Model	Description
52630	Dual-Channel 34-Signal Adaptive IF Relay - 3U OpenVPX

Options	Description
-002*	2-FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
-702	Air-cooled, Level 2
-763	Conduction-cooled, Level 3

*This option is always required. Contact Mercury for compatible option combinations.

ACCESSORY PRODUCTS

Model	Description
5292	High-Speed Synchronizer and Distribution Board
9192	Rackmount High-Speed System Synchronizer

FORM FACTORS

Cobalt products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Cobalt Model 71630 XMC (1 GHz A/D and D/A with Virtex-6 FPGA) has the following variants:

Model	
52630	3U VPX board (single XMC)
57630	6U VPX board (single XMC)
58630	6U VPX board (dual XMC)
71630	XMC module
78630	PCIe board (single XMC)

DEVELOPMENT SYSTEMS

Mercury offers development systems for Cobalt products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Cobalt boards. Please contact Mercury to configure a system that matches your requirements.

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