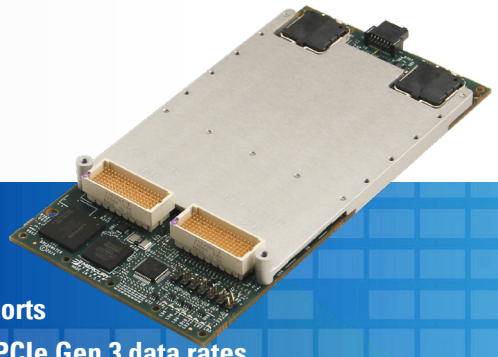
DATASHEET

EnsembleSeries™ IOM-300

XMC I/O mezzanine with sFPDP, Ethernet, Fibre Channel and PCIe gen 3 interfaces



- **Twelve channel, front-panel access fiber I/O or eight channel copper user I/O ports**
- **Supporting sFPDP (VITA 17.1), 10Gb/s Ethernet, Fibre Channel and unrestricted PCIe Gen 3 data rates**
- **Altera® Stratix V FPGA with second FPGA programing and personalized security capability**

The EnsembleSeries™ IOM-300 is a robust, versatile and fast embedded streaming I/O mezzanine that is densely packaged within an open systems architecture (OSA) XMC package (VITA 42). IOM-300 mezzanines are ideally suited for mounting on other EnsembleSeries sensor chain building blocks including LDS6527 and LDS6525 carriers.

Each EnsembleSeries IOM-300 mezzanine is highly configurable, supporting various switch fabrics and data stream protocols. Protocols include PCIe (Gen 2 and 3), serial front-panel data port (sFPDP), Fibre Channel, and 10Gb/s with front-panel I/O in both the fiber (up to 12 onboard fiber transceivers) and copper physical media.

The EnsembleSeries IOM-300's primary processing resource is Altera's fast and highly customizable Stratix V FPGA device. Mercury software defined protocol interfaces are implemented directly on this FPGA resource. Uniquely, the Stratix device is supported by a second FPGA that has its own PCIe interface to the carrier, enabling the IOM-300 to receive mission updates and upgrade its configuration in real-time.

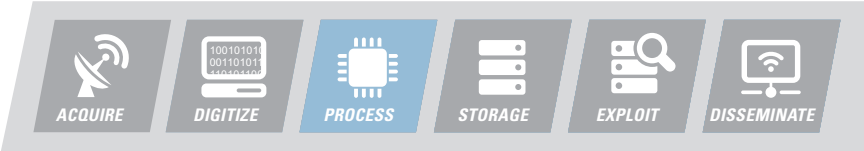
Software Defined Interfaces

Mercury's next-generation, low-latency, high-bandwidth FPGA-enabled interface software enables each mezzanine to refresh/upgrade its mission parameters in real-time and has embedded user customization and security features. This approach has backward compatibility with software protocols including inter-processor communication system (ICS™) and message passing interface/open fabrics enterprise distribution (MPI/OFED).

I/O Intelligence for Serial Front Panel Data Port (SFPDP)

When configured with Mercury's SFPDP FPGA IP, EnsembleSeries IOM-300 mezzanines are more than a traditional digital interface: each channel can be programmed for data distribution without processor intervention. Although the data destination is typically a PCIe targeted memory, with Mercury's system focused approach and drivers, destinations may be anywhere where fabric based connectivity exists, even when mode changes are called for (e.g. at a serial RapidIO® destination via a software enabled PCIe bridge).

Mercury Systems is a leading commercial provider of secure sensor and safety-critical processing subsystems. Optimized for customer and mission success, Mercury's solutions power a wide variety of critical defense and intelligence programs.



EnsembleSeries IOM-300 mezzanines can inspect the input data stream that indicates sensor mode changes and route data appropriately for each different mode. Each mode can be made to correspond with an application-defined direct memory access (DMA) command packet (CP) chain. These command packets cause the channel's DMA controller to route the data toward a predefined destination anywhere within the system's switch fabric. This data-driven distribution takes advantage of information available at the source. DMA command packets can be chained together to automatically distribute sequential data packets to different processors or endpoints.

Synchronization between the sensor I/O XMC and the application program can be accomplished by queuing a transfer request that includes status information at the desired synchronization point within the DMA chain. This block of status information is written to the local memory of the synchronizing processor. The processor can then poll on the receiving memory location for block of status information. The sensor I/O XMC can also be synchronized with a processor, via mailbox interrupts.

Real-Time Reconfiguration for Mode Changes

Mercury's FPGA technology adds the versatility of rapid reconfiguration. High-speed reconfiguration facilitates dynamic, system-level changes in mission and operating mode.

Parts of the application that are simple, fixed-point computations can run on an FPGA, saving space, power and money. Other parts of the application can run on the host processor, which is easier to program. Accordingly, the overall development time is kept manageable while the performance is maximized.

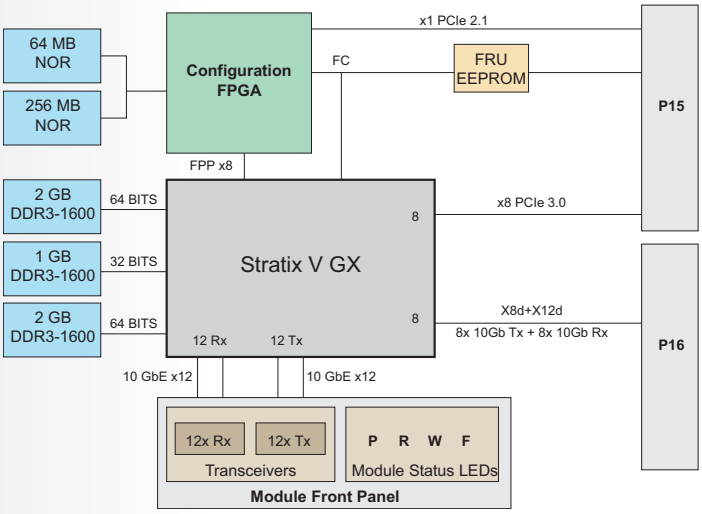


Figure 1 - EnsembleSeries IOM-300 Functional Block Diagram

The host processor allows better integration, communication and control with the on-board FCNs through the PCIe interface without interfering with the other GTP and LVDS interfaces. For example, DMA operations can be managed from the host processor without requiring additional processor boards in the system. In addition, the host processor can be used to manage the loading of the bit streams and diagnostics of the FCNs.

Ethernet Interface

EnsembleSeries IOM-300 mezzanines may be configured with full 10Gb/s Ethernet I/O. Coupled with an Altera Stratix V FPGA, the IOM-300 is well suited to act as an external connection for a signal processing subsystem. It addresses real-time I/O requests and digital signal processing such as a math co-processor for fixed-point operations used in digital image processing. In addition to 10Gb/s Ethernet, the Stratix V's flexible gigabit transceiver blocks allow other high-speed interface protocols to be implemented

Serial FPDP Interface

Serial FPDP (sFPDP) supports a mapping of the FPDP protocol onto the Fibre Channel physical layers (FC-0 and FC-1). Serial data is transmitted at 2.5 Gbaud over the fiber.

Data Frame Management (sFPDP)

EnsembleSeries IOM-300 mezzanines may be configured to enable the sensor to frame the data into "epochs." Any sensor can define its own epoch boundary based on what is most compatible with that type of sensor and how the data will be used by the processing system. In the case of radar data, these epochs are likely to be coherent processing intervals. In the case of images, an epoch is likely to be a line or a frame of an image. IOM-300 mezzanines support the four sFPDP framing options: Unframed, single-frame data, dynamic-size repeating frame data and fixed-size repeating frame data.

Data-Driven Frame Processing (sFPDP)

Many modern sensors change modes during operation. When a sensor changes modes, the processing system must make the corresponding mode change at the correct time. The sensor can also use the first word of each epoch to indicate its current mode. The EnsembleSeries IOM-300 in "cable header" mode may use this word to index a particular DMA command packet chain, and then initiate the chain without processor intervention. This allows each configuration of the sensor to have a dedicated DMA chain and a completely different data distribution from other modes.

When the sensor mode changes are known in advance, the IOM-300 can be programmed to switch DMA chains for the next mode through the use of branching at the end of a SFPDP frame or epoch. This branching capability can also be used for handling errors when the end of the SFPDP frame occurs before it is expected.

Recovering From Input Stream Faults (sFPDP)

With some input interfaces, missing or extra data can cause the interface to lose sync with an input data stream until a processor intervenes. The EnsembleSeries IOM-300 minimizes the system upset by localizing the effects of anomalies in the input stream. To do this, the XMC can re-synchronize its DMA controller to the incoming data at each data frame (epoch boundary). This re-synchronization is done by the hardware, with no processor intervention.

In the event that an end-of-epoch marker is lost, due to a media error, the maximum word count in the DMA CP will prevent data from being written past the end of the buffer.

Sensor I/O XMC Full-Duplex Operation

Each interface can operate in full-duplex mode. In addition, there are separate DMA controllers for transmit and receive on each channel — 2 DMA controllers per channel (24 per card). On each channel, transmit and receive can be synchronized.

Subsystem Scalability

FPGAs within the PCIe environment become part of a scalable system that can expand to provide as many FPGAs and microprocessors as changing applications demand with minimal application recoding and redeployment expense. Multiple FPGA XMC boards can be deployed in a single chassis, along with other boards carrying I/O devices and processors, communicating via a PCIe or a mesh fabric.

Developers can create and test algorithms on small laboratory systems consisting of only a few XMCs, with the assurance that the resulting code can move seamlessly to larger deployment platforms. Additionally, as processing requirements change in future program generations, they can readily resize target platforms with minimal impact to their code

Data-rate Scalable Interconnects

Each EnsembleSeries IOM-300 mezzanine is configured with either VITA 42 or VITA 61 XMC connectors. Air-cooled variants are populated by default with the VITA 42 XMC connector, while rugged conduction-cooled or Air-Flow-By™ variants are populated by default with VITA 61 XMC connectors. The VITA 61 connector offers superior signal integrity characteristics and is a more rugged design, appropriate for high-end XMC modules utilizing Gen3 PCIe interfaces in environmentally challenging applications.

I/O Management Software

EnsembleSeries IOM-300 mezzanines support all Mercury's current and legacy FPGA development kits (FDKs). Mercury provides a data transfer facility layered on top of our standard interprocessor communication system (ICS). This facility consists of a set of user-callable I/O control functions. These functions are used to define I/O transfer requests (DMA command packets) and to link such requests into a chain that is then automatically executed by the designated I/O device.

The FDK provides developers with the necessary components that provide interconnect, communications, command and control, memory, and I/O interfaces for flexibility and faster time to deployment. A multi-channel DMA engine, also supplied, transfers data very close to the theoretical maximum of the PCIe bus.

Mercury Sensor Processing Ecosystem

Modern sensor compute subassemblies are customized assemblies of interoperable building blocks built to open standards. Mercury's hardware and software portfolio of building blocks are physically and electrically interoperable as defined by international industrial standards, including VITA's OpenVPX standards. Mercury subsystems are designed from a suite of sophisticated open architecture building blocks that are combined and scaled to meet a broad range of advanced sensor chain processing requirements.

Mercury subsystems may include analog, digital and mixed-signal receiver modules, single-board computers and signal processing payload modules. Payloads may have acquisition, digitization, processing, and exploitation and dissemination elements and include FPGA, CPU, GPU or ADC/DAC technology, and be made up of multiple subsystems developed to multiple standards, including OpenVPX and others such as ATCA, ATX/E-ATX, or VME/VXS.

VPX-REDI

The VPX (VITA 46) standard defines 6U and 3U board formats with high performance interconnects capable of supporting today's high-speed fabric interfaces. VPX may be paired with the ruggedized enhanced design implementation standard — REDI (VITA 48). EnsembleSeries IOM300 mezzanines when packaged in conduction-cooled or Air Flow-By modules are VPX-REDI compatible. Air-cooled equivalents conform to the same OpenVPX form-factor and are suitable for less challenging environments. Targeted for harsh embedded environments, VPX-REDI supports higher functional density and two-level maintenance (2LM). 2LM allows maintenance personnel to replace a failed module.

Specifications

FPGA Compute node

FPGA processor Altera® Stratix V - 5SGXA5 or 5SGXA7 (Industrial Grade)

Configuration FPGA (PCIe Gen 2.1 interface)

DDR3 SDRAM

Capacity 5 GB - Bandwidth ~32 GB/s (peak aggregate)

Flash memory

Capacity 128 MB (typically 3–4 bit stream images)

PCIe ports to host processor

Gen 2 x8 or Gen 3 x8

Fiber links (front-panel, optional)

Up to 12 pairs at 10 Gb/s each, full-duplex 850 nm multi-mode fiber (~range 150m)

Options:

- Front-panel connectors LC or MTP
- Number of channels 4, 8 or 12 fiber pairs at 3.125Gb/s and 5Gb/s
- Fiber, 62.5 or 50µm multi-mode fiber
- TX, RX or both

XMC P16 Ports

8 SERDES at up to 10Gb/s – allows for rear transition or remote fiber use (amongst other uses)

12+19 LVDS pairs (various speeds, 19 LVDS pairs separable to single ended)

Compliance

XMC (6.5" x 2.9")

VITA 65 (OpenVPX)

VITA 46.0, 46.3, 46.4, 46.6, 46.7, 46.9, 46.11 (VPX)

VITA 48.0, 48.1, 48.2 (REDI)

VITA 61 (optional – High-speed XMC interconnect)

VITA 17.1 (sFPDP)

Environmental

See Environmental Protections for Operation at the Tactical Edge for specific ruggedness levels and cooling options.

www.mrcy.com

MADE IN AMERICA

mercury systems™

INNOVATION THAT MATTERS™

Corporate Headquarters
50 Minuteman Road • Andover, MA 01810 USA
(978) 967-1401 • (866) 627-6951 • Fax (978) 256-3599

Europe Mercury Systems, LTD
Unit 1 - Easter Park, Benyon Road, Silchester, Reading
RG7 2PQ United Kingdom
+ 44 0 1189 702050 • Fax + 44 0 1189 702321