Cobalt 52641

1-channel 3.6 GHz or 2-channel 1.8 GHz, 12-bit A/D w/ wideband DDC 3U VPX boards with Virtex-6 FPGA

Complete radar and software radio interface solution

- Radar and software radio receiver
- Communications receiver
- Analog signal interface for data recording
- Wideband data acquisition
- Remote monitoring
- Sensor interfaces

Model 52641 is a high-speed data converter with a programmable digital downconverter, suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

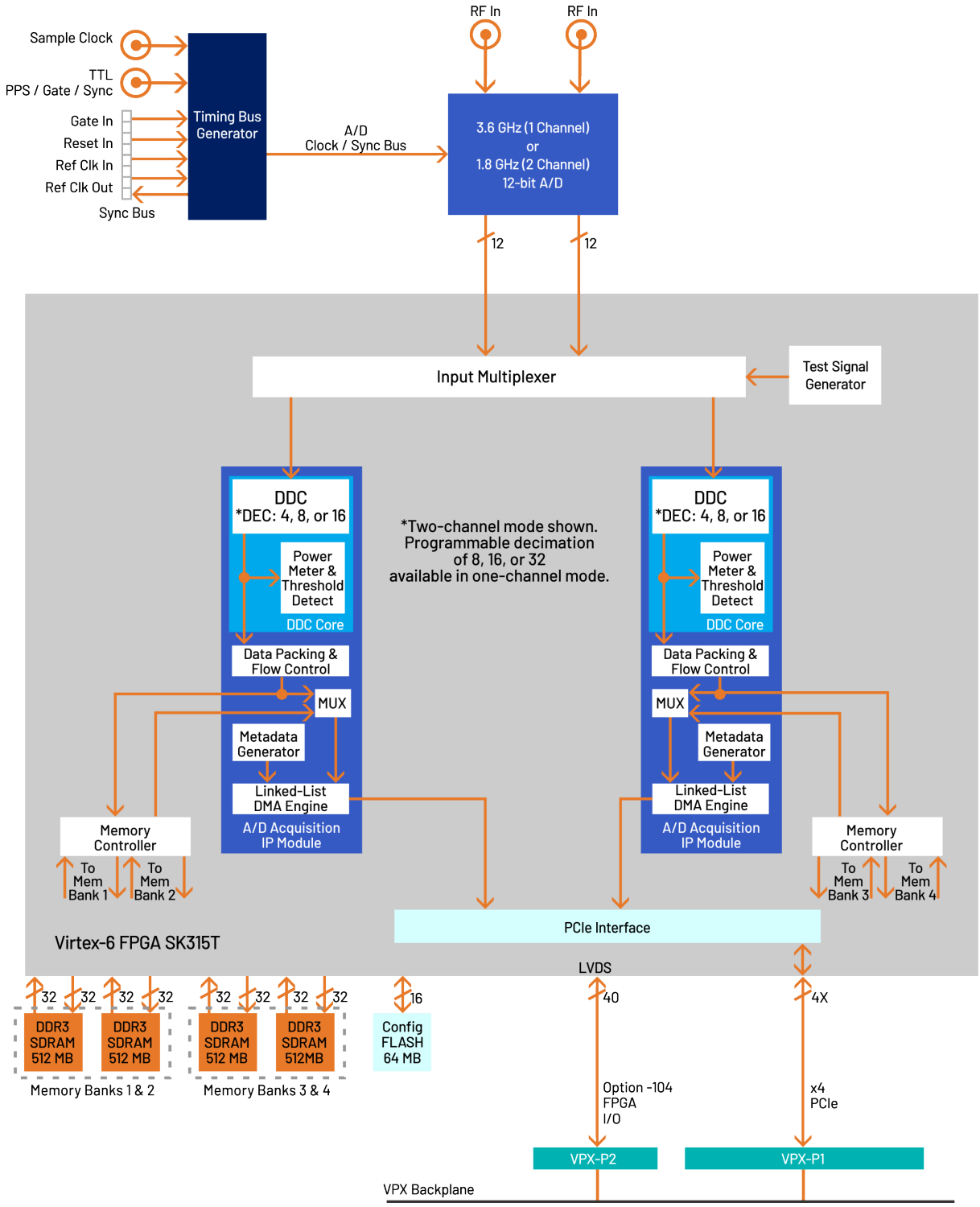
The 52641 includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

FEATURES

- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 GB of DDR3 SDRAM
- Programmable one- or two-channel DDC (Digital Downconverter)
- PCI Express (Gen. 1 & 2) interface, up to x4
- Sync bus for multiboard synchronization
- Optional LVDS connections to the FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with VITA-46, VITA-48 and VITA-65 (OpenVPX™ Specification)
- Ruggedized and conduction-cooled versions available

52641 BLOCK DIAGRAMS

Click on a block for more information.



THE COBALT ARCHITECTURE

The Cobalt® Architecture features a Xilinx Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52641 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52641 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

For applications that require additional control and status signals, option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. The GateFlow FPGA Design Kits include all of the factory-installed modules as document source code. Developers can integrate their own IP with the factory-installed functions or use the GateFlow kit to completely replace the IP with their own.

XILINX VIRTEX-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

A/D CONVERTER STAGE

The board's analog interface accepts analog HF or IF inputs on a pair of front panel SSMC connector with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 52641 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

A/D ACQUISITION MODULE

The 52641 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is very useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

CLOCKING AND SYNCHRONIZATION

The 52641 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multipin sync bus connector allows multiple boards to be synchronized, ideal for larger multichannel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple 52641s can be synchronized using the Cobalt high-speed sync board to drive the sync bus.

MEMORY RESOURCES

The 52641 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

PCI EXPRESS INTERFACE

The 52641 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

DDC IP CORES

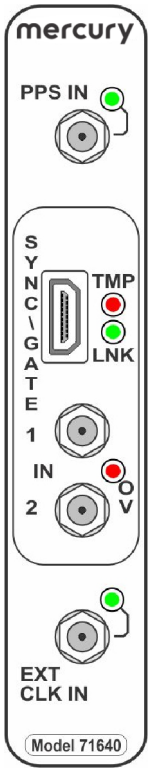
Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_S, where f_S is the A/D sampling frequency. In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_S/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_S/N.

FRONT PANEL CONNECTIONS

The XMC front panel includes four SSMC coaxial connectors, and a 19–pin µSync connector for input/output of timing and analog signals. The front panel also includes five LEDs.



- **PPS LED:** The green **PPS IN** LED illuminates when a valid PPS signal is detected. The LED will blink at the rate of the PPS signal.
- **PPS Input Connector:** One SSMC coaxial connector, labeled **PPS IN** for the input of an external PPS or Gate signal.
- **Sync Bus Connector:** The 19-pin Sync Bus front panel connectors labeled **SYNC/GATE**, provides clock reset, reference clock, and gate inputs for A/D processing, and reference clock output for synchronizing multiple boards using an external sync module.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the PCB.
- **Link LED:** The green **LNK** LED blinks when a valid link has been established over the PCIe interface.
- **Analog Input Connectors:** Two SSMC coaxial connector, labeled **IN 1** and **IN 2** for the ADC12D1800 A/D converter input channels.
- **ADC Overload LED:** The red **OV** (overload) LED indicates either an overload in the ADC12D1800 or an ADC FIFO overrun.
- **Clock LED:** The green **EXT CLK IN** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.
- **Clock Input Connector:** One SSMC coaxial connector, labeled **EXT CLK IN** for the input of an external sample clock for the ADC12D1800 A/D converter.

SPECIFICATIONS

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter

Type: Texas Instruments ADC12D1800

Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz

Resolution: 12 bits

Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz

Full Scale Input: +2 dBm to +4 dBm, programmable

Digital Downconverters

Modes: One or two channels, programmable

Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz

Decimation Range: One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x

LO Tuning Freq. Resolution: 32 bits, 0 to f_s

LO SFDR: >120 dB

Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: User-programmable 18-bit coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources

Front panel SSMC connector

Sync Bus

Multipin connectors, bus includes gate, reset and in and out reference clock

External Trigger Input

Type: Front panel female SSMC connector, TTL

Function:Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Xilinx Virtex-6 XC6VSX315T-2

Custom I/O

Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory

Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI Express Interface

PCI Express Bus: Gen. 1 or Gen. 2: x4

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: Standard 3U VPX

Depth: 170.6 mm (6.717 in.)

Height: 100 mm (3.94 in.)

Weight: VPX Carrier: 110 grams (3.9 oz.); XMC Module: Approximately 14 oz. (400 grams)

ORDERING INFORMATION

Model	Description
52641	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-6 FPGA - 3U VPX

Options	Description
-002*	2-FPGA speed grade
-064*	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
-702	Air-cooled, Level 2
-763	Conduction-cooled, Level 3
-730	2-slot heat sink

*This option is always required. Contact Mercury for compatible option combinations.

ACCESSORY PRODUCTS

Model	Description
2171	Cable Kit: SSMC to SMA
5292	High-Speed Synchronizer and Distribution Board
9192	Rackmount High-Speed System Synchronizer

FORM FACTORS

Cobalt products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Cobalt Model 71641 XMC (1-Channel 3.6 GHz or 2-Channel 1.8 GHz 12-bit A/D with DDC with Virtex-6 FPGA) has the following variants:

Model	
52641	3U VPX board (single XMC)
57641	6U VPX board (single XMC)
58641	6U VPX board (dual XMC)
71641	XMC module
78641	PCIe board (single XMC)

DEVELOPMENT SYSTEMS

Mercury offers development systems for Cobalt products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Cobalt boards. Please contact Mercury to configure a system that matches your requirements.

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