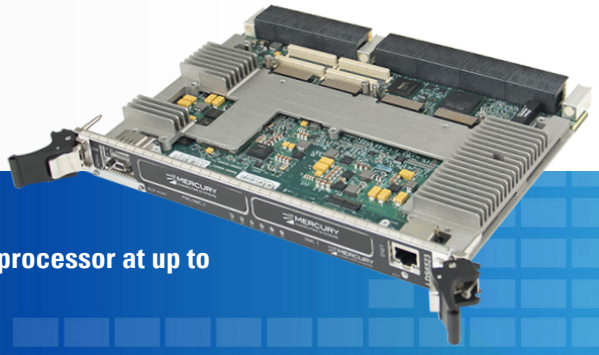
DATASHEET

EnsembleSeries™ LDS6523

6U OpenVPX SBC powered by Intel 3rd Gen i7 Quad-core processor



- **Intel® 3rd Generation Core™ i7 (Ivy Bridge mobile-class) Quad-core™ processor at up to 2.3 GHz**
- **40 Gigabit Ethernet or InfiniBand high bandwidth switching**
- **Gen3 PCIe co-processing and I/O expansion plane communications**
- **Optional built-in BuiltSECURE System Security Engineering**

The EnsembleSeries™ LDS6523 SBC features an Intel 3rd Generation Core i7 Quad-core Ivy Bridge mobile-class processor, Mellanox ConnectX-3 bridge for fast fabric data rates and configurable mezzanine I/O site in a single 6U OpenVPX SBC. The LDS6523 provides a next-generation architecture that balances the disruptive computational capabilities of the AVX-enabled Core i7 processor with QDR InfiniBand or 40 Gigabit Ethernet data paths. This combination provides a powerful and scalable computing architecture that is well aligned with high-end radar, electronic warfare and image processing applications.

Optional BuiltSECURE

For deployment at the tactical edge and export to allies, EnsembleSeries LDS6523 SBCs optionally embed BuiltSECURE technology to counter nation-state reverse engineering with System Security Engineering (SSE). BuiltSECURE is built-in SSE that enables turnkey or private and personalized security solutions to be quickly configured. The extensible nature of Mercury's SSE delivers system-wide security that evolves over time, building in future proofing. As countermeasures are developed to offset emerging threats, Mercury's security framework keeps pace, maintaining system-wide integrity. Please contact Mercury directly for BuiltSECURE configurations.

Intel 3rd Generation Core i7 Ivy Bridge Mobile-Class Processor

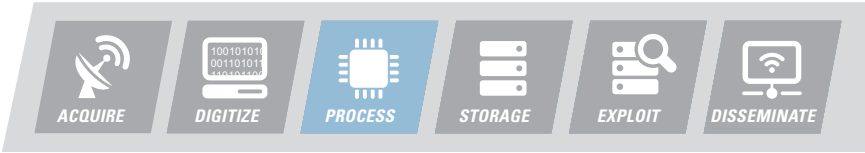
At the heart of the LDS6523 is the Intel 64-bit 3rd Generation Core i7 3615QE processor, running at up to 2.3 GHz. This is based on the Ivy Bridge processor architecture, which includes the Intel Advanced Vector Extensions (AVX) instruction set and is fabricated using a 22 nm manufacturing process. The AVX instruction set doubles the width of the processor's SIMD engine from 128 bit to 256 bit, delivering a significant improvement in floating-point processing.

Simultaneously, the 3615QE processor delivers a higher operating clock frequency than the preceding 2nd Generation Core i7 processor without an increase in power dissipation, due to the 22 nm manufacturing process. The combination of these two architectural advancements enables EnsembleSeries LDS6523 SBCs to deliver approximately 147 peak GFLOPS.

The 3615QE includes a large 6 MB cache shared between the cores, allowing many high-performance calculations to remain cache resident. This accelerates processing by eliminating the potential latency required to access DRAM to fetch upcoming data.

The Intel 3rd Generation Core i7 3615QE processor supports dual high-speed DDR3-1600 memory controllers, providing up to 25 GB/s of raw memory bandwidth. Each LDS6523 has 8 GB of DDR3-DRAM with ECC support and makes use of the Panther Point Platform Controller Hub (PCH) chipset, which provides integrated graphics capabilities along with I/O bridging between the Intel processor and external devices.

Mercury Systems is a best-of-breed provider of commercially developed, open sensor and Big Data processing systems, software and services for critical commercial, defense and intelligence applications.



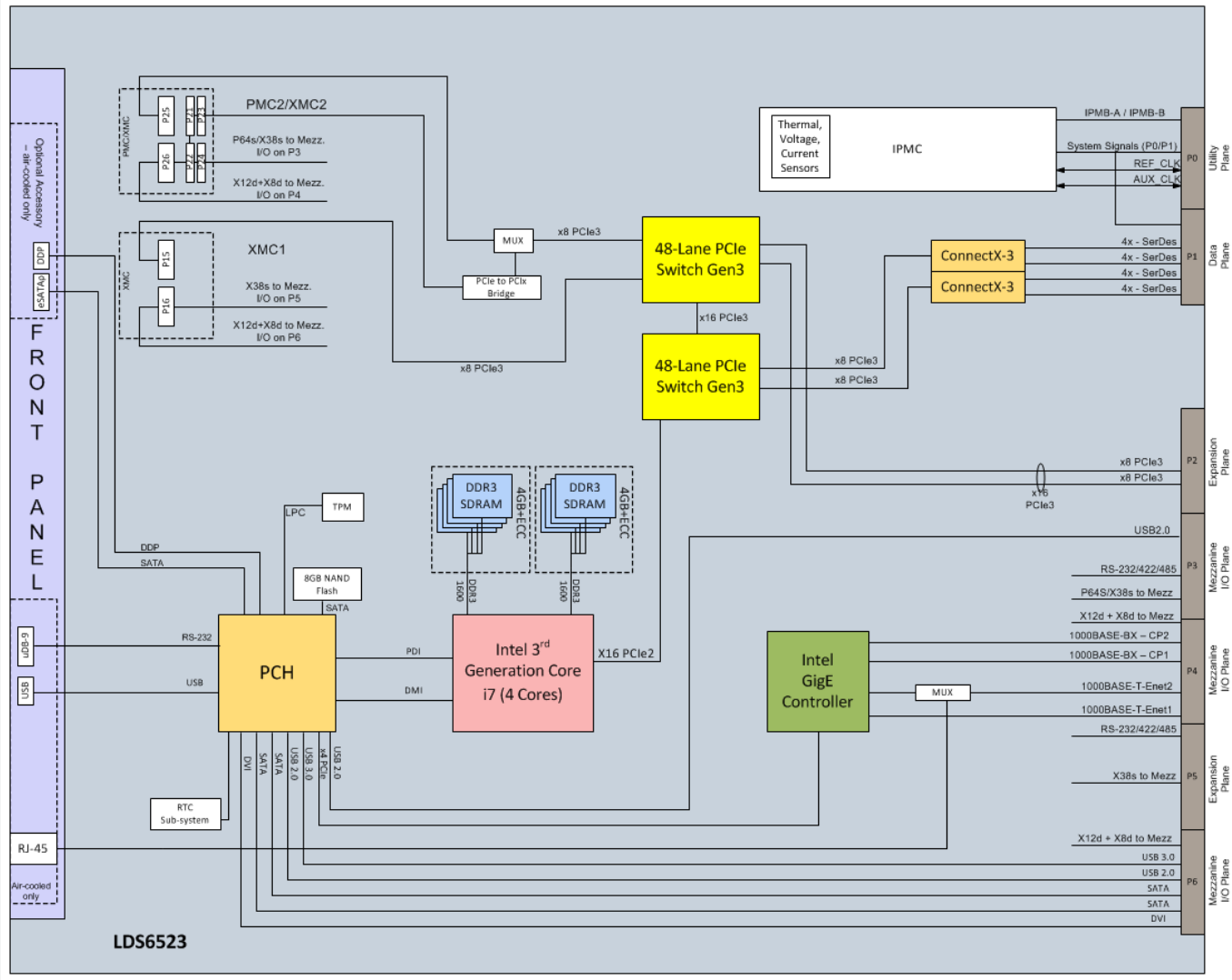


Figure 1. *LDS6523 functional block diagram*

Wide Data Plane Bandwidth

The Ensemble LDS6523 is the first embedded processing module to utilize dual Mellanox ConnectX-3 host adaptors for data plane communications. Bridging between the native Gen3 PCIe interfaces on the Intel processor and the OpenVPX data plane, the ConnectX-3 can be configured to support SDR, DDR, QDR, FDR10, 10GbE or 40GbE as the data plane protocol. This scales the data plane bandwidth up to a peak theoretical rate of 5 GB/s per port, or 20 GB/s aggregates across the entire four-port OpenVPX data plane. By scaling the data plane bandwidth to match the increase in processing performance, the LDS6523 architecture ensures that the processor is never starved for data.

EnsembleSeries LDS6523 SBCs are compliant with the VITA 65 module profile MOD6-PAY-4F1Q2U2T-12.2.1-n, where (n) can vary based on the ConnectX-3 configuration. LDS6523 SBCs are supported in chassis slots that are compliant with VITA 65 slot profile SLT6-PAY-4F1Q2U2T-10.2.1.

PCIe Architecture

EnsembleSeries LDS6523 SBCs provide dual 48-lane Gen3 PCIe switches for both on-board switching and off-board expansion. This switch complex provides an x8 PCIe interface to each of the two XMC sites, and an x4 connection to a PCIe to PCI-X bridge for the single PMC site. This enables mezzanines to operate at full bandwidth, optimizing the flow of I/O into the processing subsystem. Additional Gen3 x8 interfaces are provided to the ConnectX-3 devices, allowing bridging to the data plane without bottlenecking.

Externally, the LDS6523 implements a full Gen3 x16 PCIe connection to the OpenVPX expansion plane on the P2 VPX connector. This expansion-plane interface enables SBC compatibility with Mercury's GPU or FPGA based co-processing modules. The x16 PCIe connection can be user-configured as dual x8 connections. These configuration options let the module effectively act as an upstream/downstream PCIe switch to allow the "chaining" of PCIe devices.

Mezzanine Card Flexibility

EnsembleSeries LDS6523 SBCs have two mezzanine sites: one PMC/XMC and one XMC-only. Each standard site can be configured with off-the-shelf mezzanine cards to bring additional I/O into the system for processing or control. PMC cards are supported with a 32-bit or 64-bit PCI/PCI-X interface at up to 133 MHz on the PMC/XMC site, with PMC user-defined I/O mapped to the backplane. XMCs are supported with x8 PCIe supported on the J15/J25 connector per the VITA 42.3 standard. There are 20 differential pairs and 38 single-ended signals of XMC users I/O mapped to the backplane via the J16/J26 connector.

Multiple I/O Options

In addition to the flexibility offered via the on-board mezzanine sites, EnsembleSeries LDS6523 SBCs offer a variety of additional built-in I/O options:

- One 10/100/1000BASE-T Gigabit Ethernet connection can be routed to the front-panel on air-cooled configurations or to the backplane.
- One additional 10/100/1000BASE-T Gigabit Ethernet connection is routed to the backplane.
- Two 1000BASE-BX SERDES Ethernet connections are routed to the backplane per the OpenVPX control-plane specification.
- One DisplayPort interface is routed to an optional I/O adaptor, supporting front-panel graphical display if required.
- One DVI graphics interface is provided to the backplane.
- One TIA-232 serial port is routed to the front-panel on air-cooled configurations, or to the backplane on conduction-cooled configurations. When routed to the backplane, the serial interface can be configured for either TIA-232 or TIA-422/TIA-485 signaling.
- One front-panel USB 2.0 interface is available on air-cooled configurations.
- Configurations with an additional USB provided via an optional I/O adaptor.
- Two backplane USB interfaces are available (one 2.0, one 3.0) with both air-cooled and conduction-cooled configurations.
- One front-panel eSATA interface is provided on air-cooled configurations via an optional I/O adaptor.
- Two SATA interfaces to the backplane are provided to easily interface with storage devices.
- Eight GPIO lines act as discrete I/O usable as input, output, or to generate interrupts on the module.
- Several additional bused signals enhance the functionality of each LDS6523 SBC.

System Management

EnsembleSeries LDS6523 SBCs implement the advanced system management functionality architected in the OpenVPX specification to enable remote monitoring, alarm management, and hardware revision and health status.

Using the standard I2C bus and IPMI protocol, the on-board system-management block implements the Intelligent Platform Management Controller (IPMC) in accordance with the VITA 46.11 standard. This enables LDS6523 SBCs to:

- Read sensor values
- Read and write sensor thresholds, allowing an application to react to thermal, voltage or current variations that exceed those thresholds
- Reset the entire module
- Power up/down the entire module
- Retrieve module Field Replaceable Unit (FRU) information
- Be managed remotely by a Chassis Management Controller at the system level, such as implemented on Mercury's 6U OpenVPX switch fabric modules

Additional Features

EnsembleSeries LDS6523 SBCs provide all the features typically found on a single-board computer. In addition to the sophisticated management subsystem and fabric interconnect, LDS6523 SBCs provide users with a toolkit enabling many different application use cases.

Features include:

- Real-time clock with granularity to 1 ms and time measurement of up to 30 years
- General-purpose timers for synchronization
- Watchdog timer to support processor interrupt or reset
- Multiple boot paths, including netboot, USB boot, and boot from SATA or the on-board 8 GB flash device

Open Software Environment

Mercury leverages over 35 years of multicomputer software, including recent multicore processor expertise across its many platforms. This strategy is fully applied to the LDS6523 SBC. The same Linux® development and run-time environment is implemented on the LDS6523 as on other Intel-based Mercury platforms across the EnsembleSeries 3000, 5000 and 6000 Series. Off-the-shelf open software such as OFED and OpenMPI are fully supported by the Mellanox ConnectX-3 data plane.

Mercury OpenVPX Ecosystem

Mercury Sensor Processing Ecosystem

Modern sensor compute solutions are customized assemblies of interoperable building blocks built to open standards. Mercury's hardware and software portfolio of building blocks are physically and electrically interoperable as defined by international industrial standards, including VITA's OpenVPX standards.

These subsystems may include analog, digital and mixed-signal receiver modules, single-board computers and signal processing payload modules. Payloads may have acquisition, digitization, processing, and exploitation and dissemination elements and include FPGA, CPU, GPU or ADC/DAC technology, and be made up of multiple subsystems developed to multiple standards, including OpenVPX and others such as ATCA, ATX/E-ATX, or VME/VXS.

Module Packaging

VPX-REDI

The VPX (VITA 46) standard defines 6U and 3U board formats with a modern, high-performance connector set capable of supporting today's high-speed fabric interfaces. VPX is most attractive when paired with the ruggedized enhanced design implementation standard – REDI (VITA 48). The EnsembleSeries LDS6523 SBC is a 6U implementation of VPX-REDI, with air and conduction-cooled and Air and Liquid Flow-By™ variants in the same VPX form factor, available for less rugged environments.

Targeted primarily for harsh-environment embedded applications, VPX-REDI offers extended mechanical configurations supporting higher functional density, such as two-level maintenance (2LM). 2LM allows maintenance personnel to replace a failed module and restore the system to an operational state quickly, minimizing potential damage to the module.

Rugged Air Cooling, Air Flow-By™

Air- and conduction-cooled subsystems rely on filtration to remove contaminants from their cooling air streams. Mercury's Air Flow-By technology eliminates filtration with the most elegant cooling solution available within a sealed and rugged package. Fully compliant to VITA standards (including VITA 48.7), Air Flow-By maintains OpenVPX's 1-inch pitch requirement, is highly resilient to liquid and particle contamination, boosts SWaP, reduces operating temperature, extends MTBF by an order of magnitude, and enables embedded deployment of the most powerful and reliable processing solutions.

Specifications

Intel 3rd Generation Core™ i7 Ivy Bridge Processor

Quad-core with Advanced Vector Extensions (AVX)
- 2.3 GHz 3615QE
- Peak performance 147 GFLOPS (peak theoretical)
- Threads per core 2

Intel Virtualization Technology
- DDR3-1600 8 GB with ECC
- Raw memory bandwidth 25 GB/s (total)

Local SATA flash 8 GB

BIOS SPI flash

Mellanox ConnectX-3 VPI Host Card Adaptors

Provides fabric bridging to data plane

Supports DDR or QDR InfiniBand, or 40 Gigabit Ethernet protocols*

*The LDS6523 currently supports DDR InfiniBand. Planned variants will support QDR InfiniBand or 40 GigE. Variants may require changes to the system infrastructure such as connectors, backplane, etc.

IPMI (System Management)

On-board IPMI Controller

Voltage and temperature monitor

Geographical address monitor

Power/reset control

On-board FRU EEPROM interface

FPGA, CPU and CPLD interfaces

Ethernet Connections

1000BASE-BX Ethernet to P4 connector: 2
- OpenVPX control plane

10/100/1000BASE-T Ethernet to P4 connector: 1
- Accessible via OpenVPX RTM or external chassis interface

10/100/1000BASE-T Ethernet connection: 1
- To front panel (air-cooled module) or backplane P4 connector (conduction-cooled module)

Ethernet functions supported by the chipset include:
- UDP, TCP, SCTP, ARP, IPv4, IPv6, IEEE1588, flow control, 802.1P (priority) and 802.1Q (VLAN)

OpenVPX Multi-Plane Architecture

System management via IPMB-A and IPMB-B link on P0 management plane

InfiniBand or 40 Gigabit Ethernet interfaces on P1 data plane

Full x16 or dual x8 Gen3 PCIe expansion plane to P2 connector

Dual 1000BASE-BX Ethernet control plane

PMC-X/XMC Sites

Mezzanine sites:

- 1 PMC/XMC
- And 1 XMC only

PCI-X-to-PCIe bridge Connects PMC site to on-board PCIe switch

PMC PCI support:

- 33 and 66 MHz

PMC PCI-X support:

- 66, 100, and 133 MHz

PMC user-defined I/O from J14 to backplane

PCIe XMC sites per VITA 42.3 with XMC user-defined I/O from Jn6 to backplane

Additional I/O Capabilities

One RS-232 serial interface to front panel (air-cooled) or backplane (conduction-cooled)

Configurable for RS-232 or RS-422 signaling when routed to backplane

One additional RS-232/RS-422 serial interface to backplane

One front-panel USB 2.0 interface (air-cooled configurations only)

One USB 2.0 interface to backplane

One USB 3.0 interface to backplane

One front-panel DisplayPort interface (with optional I/O adaptor)

One DVI interface to backplane

One front-panel eSATA interface (with optional I/O adaptor)

Two SATA interfaces to backplane

Eight single-ended GPIO interfaces to backplane

System signals to backplane

NVMRO, ChassisTest, Environmental Bypass, MemoryClear

Mechanical

6U VPX (air-cooled and conduction-cooled)

1.0" slot pitch

OpenVPX and VPX-REDI

Compliance

OpenVPX standard encompasses VITA 46.0, 46.3, 46.4, 46.6, 46.11

Compatible with VITA 65

VITA 46/48.1/48.2 (REDI)

Environmental

		Environmental Qualification Levels				
		Air-cooled			Air Flow-By	Conduction-cooled
		Commercial L0	Rugged L1	Rugged L2	Rugged L4	Rugged L3
Ruggedness		•	••	••	•••	•••
Moisture/dust protection		•	••	••	•••	•••
Typical cooling performance		~140W*	~140W*	~150W*	~200W*	~150W**
Temperature	Operating*	0°C to +40°C	-25°C to +55°C	-45°C to +70°C	-40°C to +60°C	-40°C to +71°C
Operating temperature maximum rate of change		N/A	5°C/min	10°C/min	10°C/min	10°C/min
Temperature	Storage	-40°C to +85°C	-55°C to +85°C	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C
Humidity	Operating*	10-90%, non-condensing	5-95%, non-condensing	5-95%, non-condensing	5-95%, non-condensing 100% condensing	5-95%, non-condensing 100% condensing
	Storage	10-90%, non-condensing	5-95%, non-condensing	5-95%, non-condensing	5-95%, non-condensing 100% condensing	5-95%, non-condensing 100% condensing
Altitude	Operating*‡	0-10,000ft	0-30,000ft	0-30,000ft	0-30,000ft	0-70,000ft
	Storage	0-30,000ft	0-50,000ft	0-70,000ft	0-70,000ft	0-70,000ft
Vibration	Random	0.003 g^2/Hz; 20-2000 Hz, 1 hr/axis	0.04 g^2/Hz; 20-2000 Hz, 1 hr/axis	0.04 g^2/Hz; 20-2000 Hz, 1 hr/axis	0.1 g^2/Hz; 5-2000 Hz, 1 hr/axis	0.1 g^2/Hz; 5-2000 Hz, 1 hr/axis
	Sine	N/A	N/A	N/A	10G peak; 5-2000 Hz, 1 hr/axis	10G peak; 5-2000 Hz, 1 hr/axis
	Shock	z-axis: 20g; x and y-axes: 32g; (11ms ½-sine pulse, 3 positive, 3 negative)	z-axis: 50g; x and y-axes: 80g; (11ms 1/2-sine pulse, 3 positive, 3 negative)	z-axis: 50g; x and y-axes: 80g; (11ms 1/2-sine pulse, 3 positive, 3 negative)	z-axis: 50g; x and y-axes: 80g; (11ms 1/2-sine pulse, 3 positive, 3 negative)	z-axis: 50g; x and y-axes: 80g; (11ms 1/2-sine pulse, 3 positive, 3 negative)
Salt/Fog		N/A	Contact Factory	Contact Factory	10% NaCl	10% NaCl
VITA 47		Contact Factory				

* Customer must maintain required cfm level. Consult factory for the required flow rates.

** Card edge should be maintained below 71°C

Storage Temperature is defined per MIL-STD-810F, Method 502.4, para 4.5.2, where the product under non-operational test is brought to an initial high temperature cycle to remove moisture. Then the unit under non-operational test will be brought to the low storage temperature. The low temperature test is maintained for 2 hours. The product is then brought to the high storage temperature and is maintained for 2 hours. The product is then brought back to ambient temperature. All temperature transitions are at a maximum rate of 10°C/min. One cold/hot cycle constitutes the complete non-operational storage temperature test. This assumes that the board level products are individually packaged in accordance with ASTM-D-3951 approved storage containers. These tests are not performed in Mercury shipping containers, but in an unrestrained condition. Please consult the factory if you would like additional test details.

All products manufactured by Mercury meet elements of the following specifications: MIL-STD-454, MIL-STD-883, MIL-HDBK-217F, and MIL-I-46058 or IPC-CC-830, and various IPC standards. Mercury's inspection system has been certified in accordance with MIL-I-45208A.

Additional Services

Optional Environmental Screening and Analysis Services		Standard Module, Optional Services	
• Cold Start Testing	• Safety Margin Analysis	• Engineering Change Order (ECO) Notification	• Alternate Mean Time Between Failure (MTBF) Calculations
• Cold Soak Testing	• Temperature Cycling	• ECO Control	• Hazmat Analysis
• Custom Vibration	• Power Cycling	• Custom Certificate of Conformity (CofC)	• Diminished Manufacturing Sources (DMS) Management
• CFD Thermal Analysis	• Environmental Stress Screening	• Custom UID Labeling	• Longevity of Suppy (LOS)
• Finite Element Analysis			• Longevity of Repair (LOR)
Contact factory for additional information			

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mercury systems™

INNOVATION THAT MATTERS ®

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