

EnsembleSeries™ LDS6525

6U OpenVPX SBC Powered by Intel 4th Gen i7 Processor



- Intel® 4th Generation Quad-Core™ i7 processor (Haswell mobile class)
- Software defined Gen 2 serial RapidIO® & 10 Gigabit Ethernet switch fabrics
- Integrated Gen 3 PCIe switching for on/off-board co-processing
- XMC and XMC/PMC mezzanine sites

The EnsembleSeries™ LDS6525 is a 6U OpenVPX™ SBC featuring a 4th Generation Intel Quad-core i7 processor (Haswell mobile class), firmware-upgradable FPGA implemented switched fabrics and configurable mezzanine I/O. The LDS6525 SBC provides a next-generation architecture that blends the computational capabilities of the AVX2-enabled Core i7 processor with Gen 2 serial RapidIO or 10 Gigabit Ethernet data paths. This combination provides a powerful and scalable computing architecture that is well aligned with high-end radar, electronic warfare, and image processing applications.

Intel 4th Generation Core i7 Haswell Mobile-Class Processor

At the heart of the LDS6525 SBC is the Intel 64-bit 4th Generation Core i7-4700EQ processor, running at up to 2.4 GHz. This processor includes an Advanced Vector Extensions-2 (AVX2) instruction set which doubles the width of the processor's SIMD engine from 128 bit to 256 bit, and contains Fused Multiply-Add (FMA), delivering a significant improvement in floating-point processing.

The 4700EQ includes a large 6 MB cache shared between the cores, allowing many high-performance calculations to remain cache resident. This accelerates processing by eliminating the potential latency required to access DRAM to fetch upcoming data. The processor supports dual high-speed DDR3-1600 memory controllers, providing up to 25 GB/s of raw memory bandwidth. Each LDS6525 has 8 GB of DDR3-DRAM with ECC support.

The four processor cores are supported by the latest on-die GT2 GPU for high-definition graphical and intensive, parallel data processing. Programming options include the device's native OpenCL support and the efficiency of Intel's FMA.

Software Defines Interfaces

Mercury's next generation, low-latency, high-bandwidth FPGA-enabled interface software allows each mezzanine to refresh/upgrade its mission parameters in real-time and has embedded user customization and security features. This approach has backward compatibility with software protocols, including an inter-processor communication system (ICS™) and message passing interface/open fabrics enterprise distribution (MPI/OFED).

Mercury Systems is the better alternative for affordable, secure processing subsystems designed and made in the USA. These capabilities make us the first commercially based defense electronics company built to meet rapidly evolving next-generation defense challenges.



ACQUIRE



DIGITIZE



PROCESS



STORAGE



EXPLOIT



DISSEMINATE

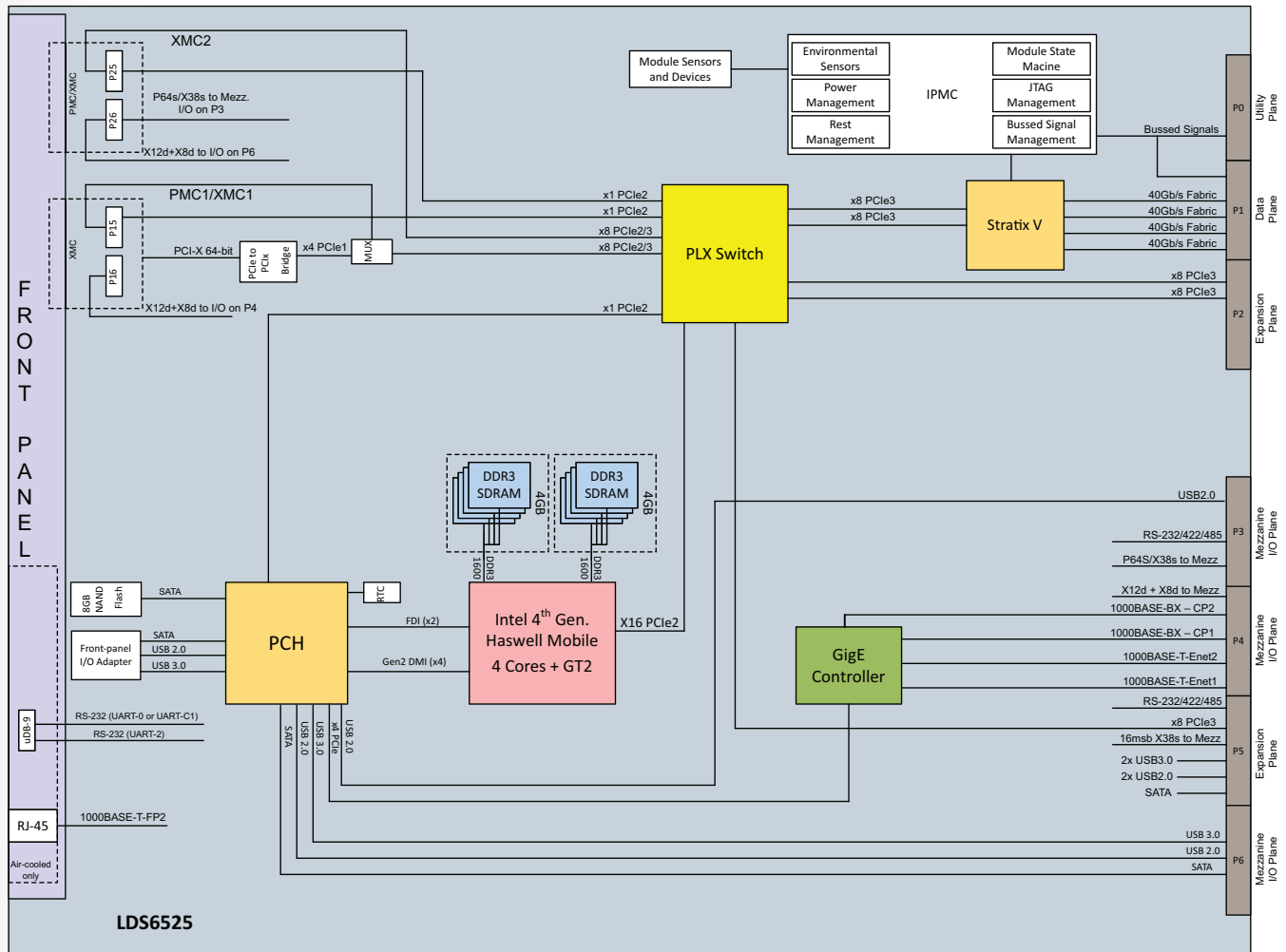


Figure 1. LDS6525 functional block diagram

PCIe Architecture

EnsembleSeries LDS6525 SBCs provide single 81-lane Gen 3 PCIe switches for both on-board switching and off-board expansion. This switch complex provides an x8 PCIe interface to each of the two XMC sites, as well as an x4 connection to a PCIe to PCI-X® bridge for the single PMC site. This enables mezzanines to operate at full bandwidth, optimizing the flow of I/O into the processing subsystem.

Externally, the LDS6525 implements a full Gen 3 x16 PCIe connection to the OpenVPX expansion plane on the P2 VPX connector. This expansion plane interface enables the LDS6525 to communicate with Mercury's GPU or FPGA based co-processing modules. These configuration options let the SBC effectively act as an upstream/downstream PCIe switch to allow the "chaining" of PCIe devices.

Mezzanine Card Flexibility

EnsembleSeries LDS6525 SBCs have two mezzanine sites: one PMC/XMC and one XMC-only. Each of these standard sites can be configured with off-the-shelf mezzanine cards to bring additional I/O into the system for processing or control. PMC cards are supported with a 32 or 64-bit PCI/PCI-X interface at up to 133 MHz on the PMC/

XMC site, with PMC user-defined I/O mapped to the backplane. XMCs are supported with x8 PCIe on the J15/J25 connector per the VITA 42.3 standard. There are 16 differential pairs and 38 single-ended signals of XMC user I/O mapped to the backplane via the J16/J26 connector.

EnsembleSeries LDS6525 SBCs support this configuration with either VITA 42 or VITA 61 XMC connectors. Air-cooled variants are populated by default with the VITA 42 XMC connector, while rugged conduction-cooled or Air Flow-By variants are populated by default with VITA 61 XMC connectors. The VITA 61 connector offers superior signal integrity characteristics and has a more rugged design, appropriate for high-end XMC modules utilizing Gen 3 PCIe interfaces in environmentally challenging applications.

Multiple I/O Options

In addition to the flexibility offered via the on-board mezzanine sites, LDS6525 SBCs offer a variety of additional built-in I/O options:

- One 10/100/1000BASE-T Gigabit Ethernet connection can be routed to the front-panel on air-cooled configurations or to the backplane.
- One additional 10/100/1000BASE-T Gigabit Ethernet connection is routed to the backplane.
- Two 1000BASE-BX SERDES Ethernet connections are routed to the

backplane per the OpenVPX control plane specification.

- One TIA-232 serial port is routed to the front-panel on air-cooled configurations, or to the backplane on conduction-cooled configurations. When routed to the backplane, the serial interface can be configured for either TIA-232 or TIA-422 signaling.
- One front-panel USB 3.0 interface is available on air-cooled configurations.
- Two backplane USB interfaces are available (one 2.0, one 3.0) with both air-cooled and conduction-cooled configurations.
- Two SATA interfaces to the backplane are provided to interface with storage devices.
- Eight GPIO lines act as discrete I/O usable as input, output, or to generate interrupts on the module.
- Several additional bused signals enhance the LDS6525 functionality.

System Management

EnsembleSeries LDS6525 SBCs implement an advanced system management functionality, architected in OpenVPX standard to enable remote monitoring, alarm management, hardware revision, and health status. Using the standard I2C bus and Intelligent Platform Management Controller (IPMC) protocol, the on-board system management block implements the IPMC.

This enables the LDS6525 SBCs to:

- Read sensor values
- Read and write sensor thresholds, allowing an application to react to thermal, voltage or current variations
- Reset the entire module
- Power up/down the entire module
- Retrieve module Field Replaceable Unit (FRU) information
- Manage remotely by a Chassis Management Controller at the system level, such as implemented on Mercury's 6U OpenVPX switched fabric modules

VPX-REDI

The VPX (VITA 46) standard defines 6U and 3U board formats with a modern, high-performance connector set capable of supporting today's high-speed fabric interfaces. VPX is most attractive when paired with the ruggedized enhanced design implementation standard – REDI (VITA 48). The EnsembleSeries LDS6525 SBC is a 6U implementation of VPX-REDI, with air and conduction-cooled and Air and Liquid Flow-By™ variants in the same VPX form factor available for less rugged environments.

Targeted primarily for harsh-environment embedded applications, VPX-REDI offers extended mechanical configurations supporting higher functional density, such as two-level maintenance (2LM). 2LM allows maintenance personnel to replace a failed module and restore the system to an operational state quickly, minimizing potential damage to the module.

Rugged Air Cooling: Air Flow-By™

Air- and conduction-cooled subsystems rely on filtration to remove contaminants from their cooling air streams. Mercury's Air Flow-By technology eliminates filtration with the most elegant cooling solution available within a sealed and rugged package. Fully compliant to VITA standards (including VITA 48.7), Air Flow-By maintains the OpenVPX 1-inch pitch requirement, is highly resilient to liquid and particle contamination, boosts SWaP, reduces operating temperature, extends MTBF by an order of magnitude, and enables embedded deployment of the most powerful and reliable processing solutions.

Additional Features

EnsembleSeries LDS6525 SBCs provide all the features typically found on a single-board computer. In addition to the sophisticated management, subsystem and switched fabric interconnect, LDS6525 SBCs provide users with a toolkit enabling many different application use cases. Features include:

- Real-time clock with granularity to 1 ms and time measurement of up to 30 years
- General-purpose timers for synchronization
- Watchdog timer to support processor interrupt or reset
- Multiple boot paths, including netboot, USB boot and boot from SATA or the on-board 8 GB flash device.

Open Software Environment

Mercury leverages over 35 years of multicomputer software expertise, including recent multicore processor expertise, across its many platforms. This strategy is fully applied to the LDS6525 SBC. The same Linux® development and run-time environment is implemented on the LDS6525 SBC as on other Intel-based Mercury platforms across the EnsembleSeries 3000, 5000 and 6000 Series. Off-the-shelf open software such as OFED, OpenMPI and MultiCore Plus™ are fully supported by the software-enabled data plane.

Specifications

Processor

Single 2.4GHz 4th Generation Intel i7 Quad-Core mobile (Haswell mobile) CPU (i7-4700EQ)

Threads per core: 2 (8 total per CPU)

On-die GT2 GPU

Processor support: AVX2, 256 bit vector engine incorporating

Fused Multiple-Add (FMA)

Peak performance per module:

Processor: 307 GFLOPS

GT2 GPU: 208 GFLOPS

PCIe Gen 3 (x8)

OpenCL

PCH (Platform Controller Hub) LynxPoint mobile QM87

Intelligent Platform Management Interface (IPMI)

On-board IPMI controller

Voltage and temperature monitor

Geographical address monitor

Power/reset control

On-board FRU EEPROM interface

FPGA, CPU and CPLD interfaces

Ethernet Connections

1000BASE-BX Ethernet to P4 connector

OpenVPX control plane

10/100/1000BASE-T Ethernet to P4 connector

Accessible via OpenVPX RTM or external chassis interface

10/100/1000BASE-T Ethernet connection

To front-panel (air-cooled module) or backplane P4 connector (conduction-cooled module)

Control plane functions supported by the chipset include:

UDP, TCP, SCTP, ARP, IPv4, IPv6, IEEE1588, flow control, 802.1P (priority) and 802.1Q (VLAN)

OpenVPX Multi-Plane Architecture

System management via IPMB-A and IPMB-B links on P0 management plane

Gen 2 serial RapidIO or 10 Gigabit Ethernet interfaces on P1 data plane

Full x16 or dual x8 Gen3 PCIe expansion plane to P2 connector

Dual 1000BASE-BX Ethernet control plane

PMC/XMC Sites

Mezzanine sites 1 PMC/XMC and 1 XMC

PCI-X to PCIe bridge Connects PMC site to on-board

PCIe

PMC PCI support 33 and 66 MHz

PMC PCI-X support 66, 100, and 133 MHz

PMC user-defined I/O from J14 to backplane

PCIe XMC sites per VITA 42.3 with XMC user-defined I/O from Jn6 to backplane

Additional I/O Capabilities

One RS-232 serial interface to front-panel (air-cooled) or backplane (conduction-cooled)

Configurable for RS-232 or RS-422 signaling when routed to backplane

One additional RS-232/RS-422 serial interface to backplane

One front-panel USB 3.0 interface (air-cooled configurations only)

One USB 2.0 interface to backplane

One USB 3.0 interface to backplane

One DVI interface to backplane

Two SATA interfaces to backplane

Eight single-ended GPIO interfaces to backplane

System signals to backplane

NVMRO, Chassis Test, Environmental Bypass, Memory Clear

Mechanical

6U OpenVPX

1.0" slot pitch

OpenVPX and VPX-REDI

Compliance

OpenVPX system standard encompasses VITA 46.0, 46.3, 46.4, 46.6, 46.11

Compatible with VITA 65

VITA 46/48.1/48.2 (REDI)

Serial RapidIO, PCIe, 10 Gigabit Ethernet

Environmental

MOTS+ rugged packaging for extreme environmental protection

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3019.06E-1022-DS-LDS6525



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