Jade 71132

8-channel 250 MHz A/D with multiband DDCs XMC module with Kintex UltraScale FPGA

Complete radar and software radio interface solution

- Radar and software radio receiver
- Communications receiver
- Analog signal interface for data recording
- Wideband data acquisition
- Remote monitoring
- Sensor interfaces

The 71132 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

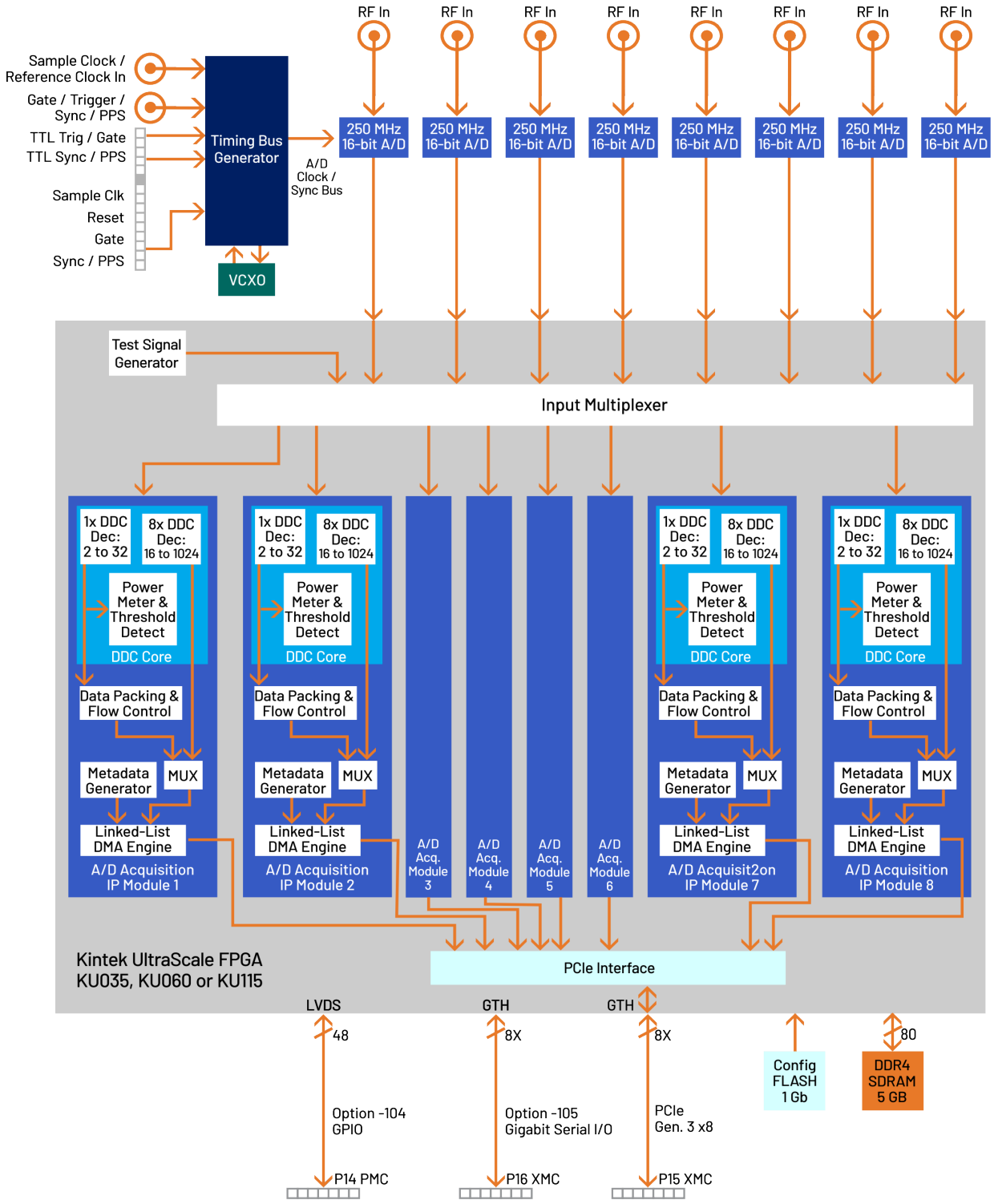
It includes eight A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the 71132 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

FEATURES

- Supports powerful Xilinx® Kintex® UltraScale FPGAs
- Eight 250 MHz 16-bit A/Ds
- Eight wideband DDCs (digital downconverters)
- 64 multiband DDCs
- 5 GB of 2400 MHz DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express interface (Gen. 1, 2 & 3) up to x8
- VITA 42.0 XMC compatible with switched-fabric interfaces
- Optional LVDS port and gigabit serial connections for custom FPGA I/O
- Ruggedized and conduction-cooled versions
- Navigator Design Suite for software and custom IP development

71132 BLOCK DIAGRAM

Click on a block for more information.



THE JADE ARCHITECTURE

Evolved from the proven designs of the Mercury Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71132 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 71132 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

XILINX KINTEX ULTRASCALE FPGAS

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs: KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

A/D CONVERTER STAGE

The board's analog interface accepts eight analog HF or IF inputs on front panel MMCX connectors with transformer coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16 bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other module resources.

A/D ACQUISITION IP MODULES

These models feature eight or 16 A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the A/Ds or test signal generators.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP CORES

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each acquisition module can choose between the two cores allowing for a very flexible down conversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to fs, where fs is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to fs, where fs is the A/D sampling frequency. Decimations can be programmed from 16 to 1024 in steps of 8.

The decimating filter for all DDCs accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*fs/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of fs/N.

CLOCKING AND SYNCHRONIZATION

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In

this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Up to three additional modules can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

MEMORY RESOURCES

The 71132 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Mercury-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI EXPRESS INTERFACE

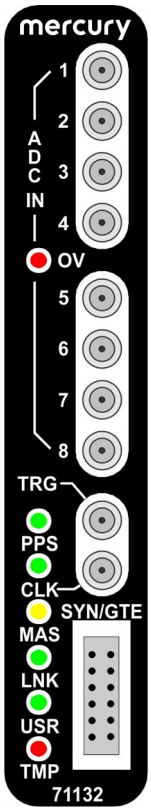
The 71132 includes an industry standard interface fully compliant with PCI Express Gen. 1, 2, and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

XMC INTERFACE

The 71132 complies with the VITA 42.0 XMC specification. A connector provides a single 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71132 supports x8 PCIe on the first XMC connector leaving the second free to support user-installed transfer protocols specific to the target application.

FRONT PANEL CONNECTIONS

The front panel includes ten MMCX coaxial connectors for clock, trigger, and analog input signals, and a 12-pin Sync Bus input/output connector. The front panel also includes seven LED indicators.



- **Analog Input Connectors:** Eight MMCX coaxial connectors, labeled **In 1, 2, 3, 4, 5, 6, 7,** and **8**: one for each ADC input channel.
- **ADC Overload LED:** There is one red **OV** (overload) LED for all ADC inputs. This LED indicates either an overload detection in one of the ADS42LB69s, or an ADC FIFO overrun.
- **Trigger Input Connector:** One MMCX coaxial connector, labeled **TRIG**, for input of an external trigger.
- **PPS LED:** The green **PPS** LED illuminates when a valid PPS signal is detected. The LED will blink at the rate of the PPS signal.
- **Clock LED:** The green **CLK** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.
- **Clock Input Connector:** One MMCX coaxial connector, labeled **CLK**, for input of an external sample clock.
- **Master LED:** The yellow **MAS** LED illuminates when this board is the Sync Bus Master. When only a single board is used, it must be a Master.
- **Link LED:** The green **LNK** LED indicates the link speed when a valid link has been established over the PCIe interface, as follows: Gen 1 - LED blinks slowly (less than once per second); Gen 2 - LED blinks about once per second; Gen 3 - LED will be constantly on.
- **User LED:** The green **USR** LED is for user applications.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the PCB.
- **Sync Bus Connector:** The 12-pin µSync front panel connector, labeled **SYNC/GATE**, provides clock, sync and gate input/output signals for the Low Voltage Positive Emitter Coupled Local (LVPECL) Sync Bus.

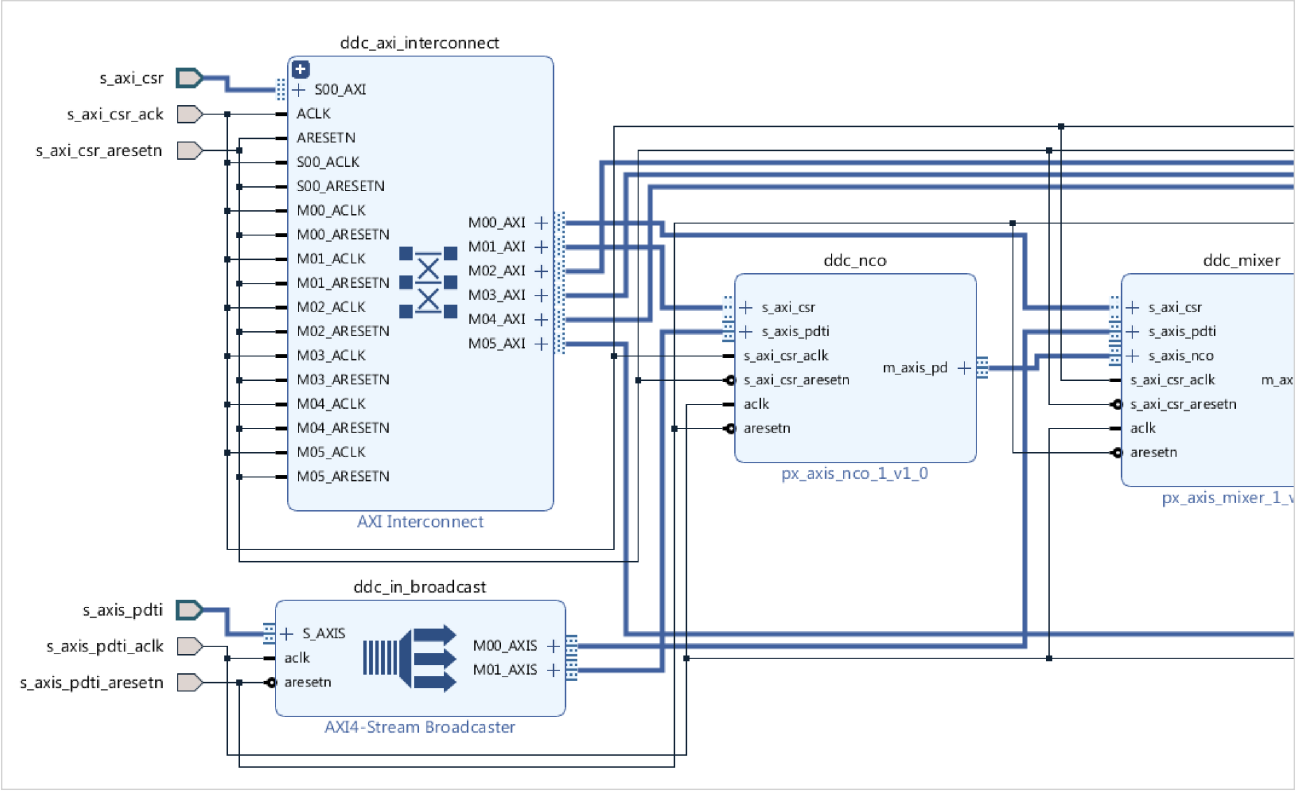
NAVIGATOR DESIGN SUITE

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into the factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

The **Navigator FPGA Design Kit (FDK)** for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Jade product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Jade design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations.

Navigator FDK includes an IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.

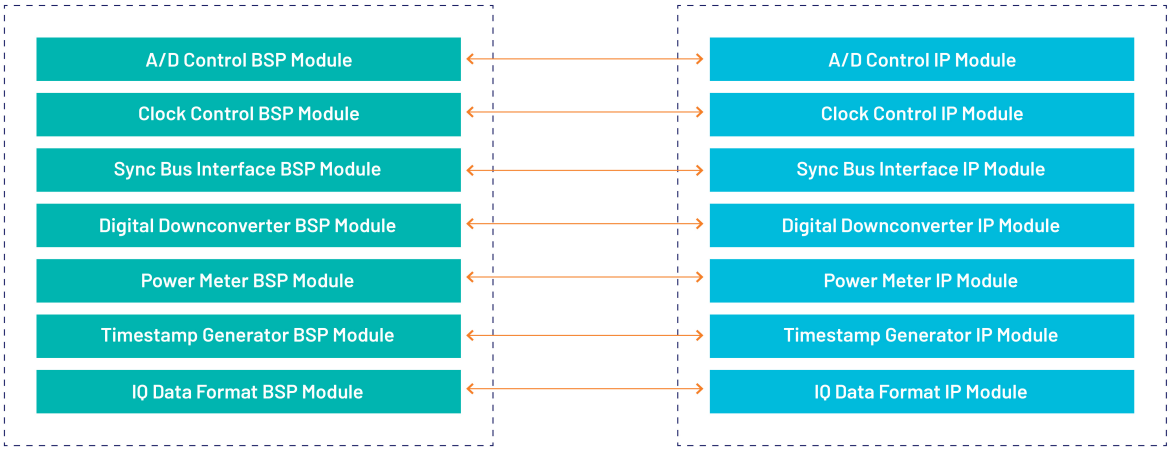
The **Navigator Board Support Package (BSP)** provides software support for Jade boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA. The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.



Navigator IP FPGA Design viewed in IP Integrator

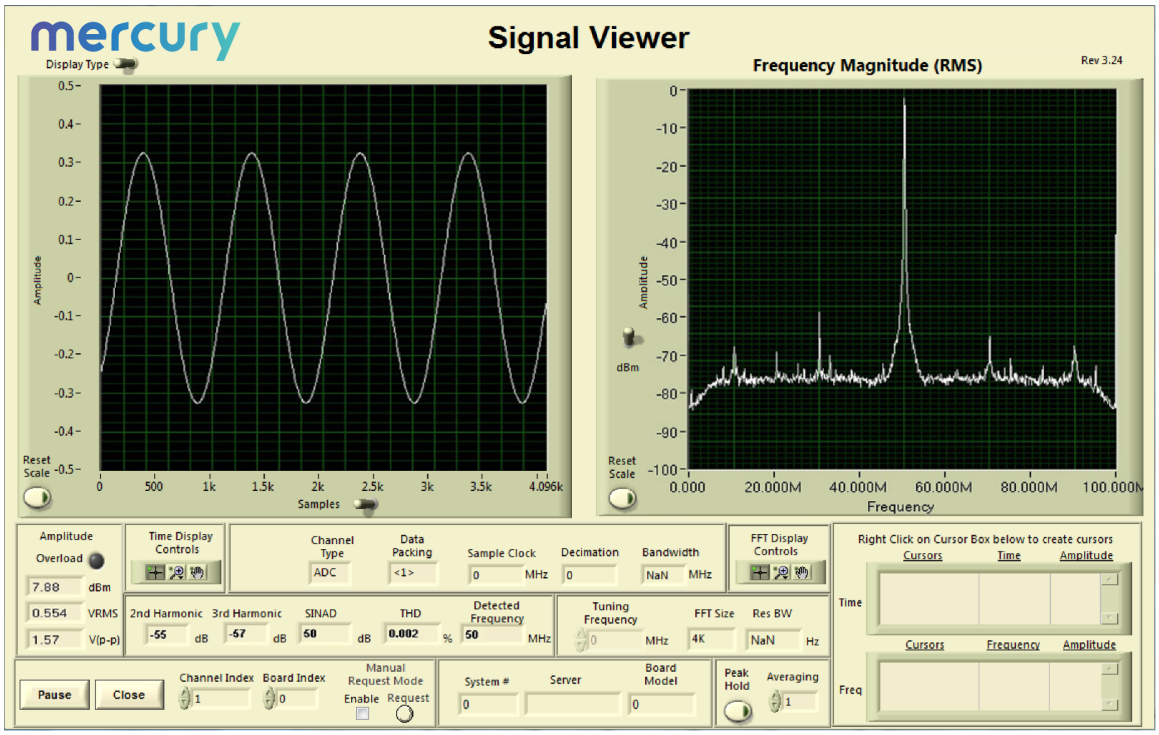
NAVIGATOR BOARD SUPPORT PACKAGE

NAVIGATOR FPGA DESIGN KIT



Because all Jade boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the **Signal Viewer**, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Jade board and Navigator BSP and start viewing analog signals immediately.



SPECIFICATIONS

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS42LB69

Sampling Rate: 10 MHz to 250 MHz

Resolution: 16 bits

Wideband Digital Downconverters

Quantity: Eight channels

Decimation Range: 2x to 32x

LO Tuning Freq. Resolution: 32 bits, 0 to f_s

LO SFDR: >120 dB

Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters

Quantity: 8 banks, 8 channels per bank

Decimation Range: 16x to 1024x in steps of 8

LO Tuning Freq. Resolution: 32 bits, 0 to f_s, independent tuning for each channel

LO SFDR: >120 dB

Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources

On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 3, 4, 6, 8, or 16, independently for the A/D and D/A clock

External Clock

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus

12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female MMCX connector, LVTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- Standard: Xilinx Kintex UltraScale XCKU035-2
- Option -084: Xilinx Kintex UltraScale XCKU060-2
- Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O

- Option -104: Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- Option -105: Installs the XMC P16 connector providing 8X serial connections to the FPGA

Memory

Type: DDR4 SDRAM

Size: 5 GB

Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -713: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: Single XMC module

- Depth: 149.0 mm (5.87 in)
- Height: 74 mm (2.91 in)

Weight: Approximately 14 oz (400 grams)

ORDERING INFORMATION

Model	Description
71132	8-channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - XMC

Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-100	27 MHz crystal for MAX2121
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-702	Air-cooled, Level 2
-713	Conduction-cooled, Level 3

Contact Mercury for compatible option combinations and complete specifications of rugged and conduction-cooled versions. Options may change, so be sure to contact Mercury for the latest information.

ACCESSORY PRODUCTS

Model	Description
9192	Rackmount high-speed system synchronizer

DEVELOPMENT SYSTEMS

Mercury offers development systems for Jade products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Jade boards. Please contact Mercury to configure a system that matches your requirements.

FORM FACTORS

Jade products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Jade Model 71132 XMC (8-Channel 250 MHz A/D with Multiband DDC, Kintex UltraScale FPGA) has the following variants:

Model	
52132	3U VPX board (single XMC)
57132	6U VPX board (single XMC)
58132	6U VPX board (dual XMC)
71132	XMC module
78132	PCIe board (single XMC)

Corporate Headquarters
50 Minuteman Road
Andover, MA 01810 USA
+1 978.967.1401 tel
+1 866.627.6951 tel
+1 978.256.3599 fax

International Headquarters
Mercury International
Avenue Eugène-Lance, 38
PO Box 584
CH-1212 Grand-Lancy 1
Geneva, Switzerland
+41 22 884 5100 tel

Learn more

Visit: mrcy.com/go/MP71132

For technical details, contact:
mrcy.com/go/CF71132