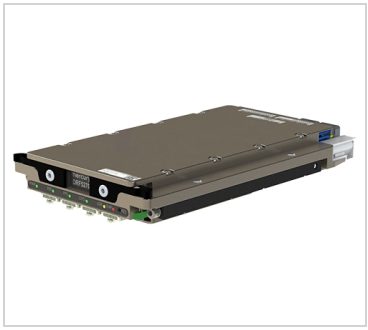
DRF5270

3U VPX SOSA Aligned 8-Channel A/D and D/A Board based on the Altera® Agilex® 9 Direct RF-Series

Developed in alignment with the SOSA Technical Standard

- High-bandwidth data streaming
- Waveform signal generator
- Communication receiver and transmitter
- Electronic Warfare transponder
- Analog I/O for digital recording and playback
- Sensor interfaces



The DRF5270 is a high-performance, SOSA™ aligned board based on the Altera Agilex 9 Direct RF-Series. Eight 40 to 64 GSPS A/D and D/A converters are integrated into the Agilex 9's multiprocessor architecture, creating a multichannel data conversion and processing solution on a single chip. The DRF5270 brings Agilex 9 performance to 3U VPX with a complete system on a board.

Complementing the Agilex 9's on-chip resources are the DRF5270's sophisticated clocking section for multichannel and multiboard synchronization, a modular front end for RF input and output, 16 GBytes of DDR4, a 10 GigE interface, a 40 GigE interface, a gigabit serial optical interface capable of supporting dual 100 GigE connections and general-purpose serial and parallel signal paths to the FPGA.

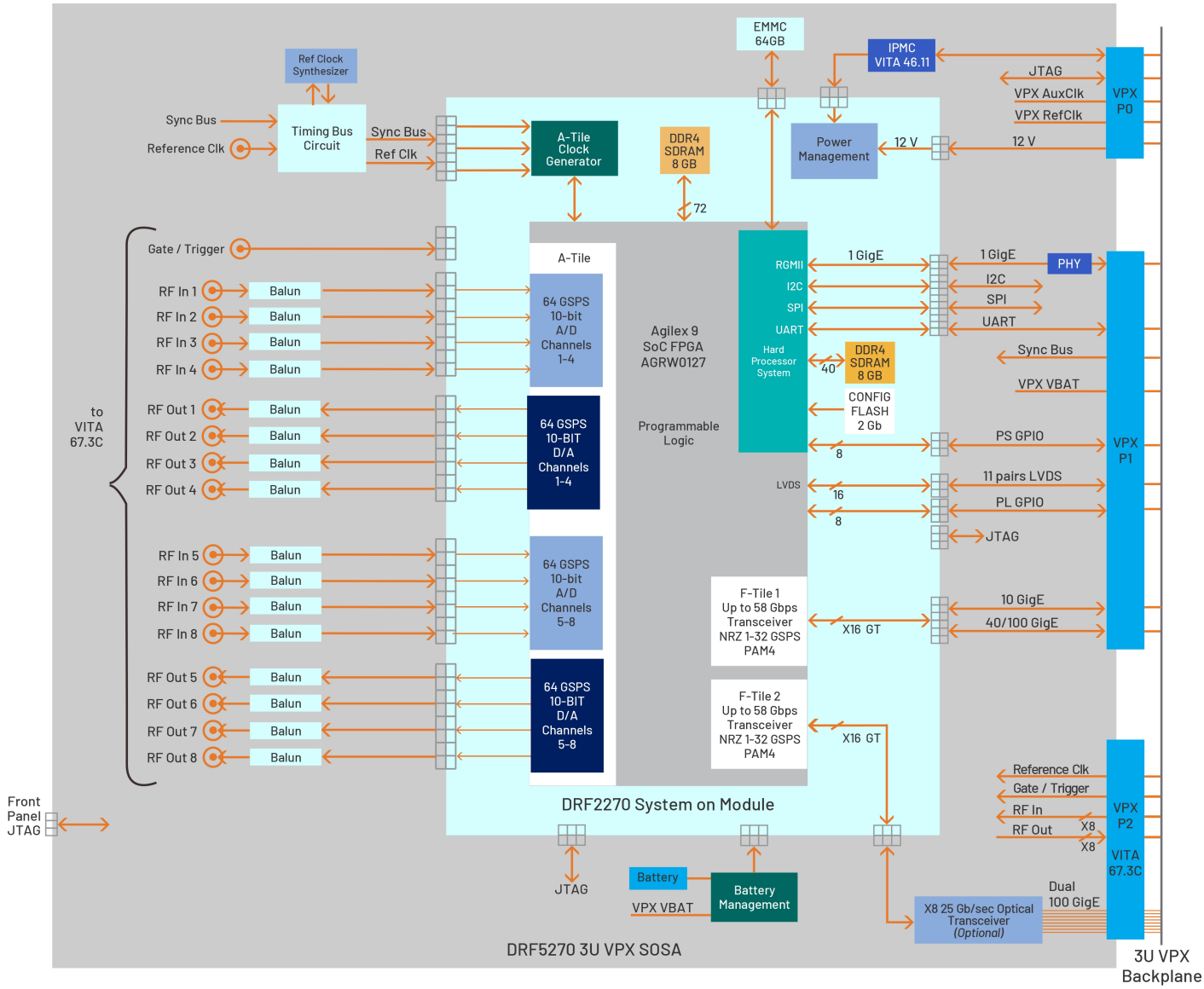
FEATURES

- Developed in alignment with the SOSA™ Technical Standard
- Incorporates Altera Agilex 9 Direct RF AGRW027
- 16 GB of DDR4 SDRAM
- 1 GigE Interface
- 10 GigE Interface
- 40 GigE Interface
- Optional VITA 67.3C optical interface for gigabit serial communication
- Dual 100 GigE UDP interface
- Compatible with several VITA standards including: VITA 46, VITA 48, VITA 67.3C, and VITA 65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled
- Unique system-on-module design enables migration to other form factors
- Board Support Package (BSP) for software development
- FPGA Design Kit (FDK) for custom IP development

SOSA™ Sensor Open Systems Architecture

DRF5270 BLOCK DIAGRAM

Click on a block for more information.



BOARD ARCHITECTURE

The DRF5270 board design places the Agilex 9 as the cornerstone of the architecture. All control and data paths are accessible by the programmable logic and processing system. A full suite of Mercury-developed IP and software functions utilize this architecture to provide data capture, waveform generation, and interface solutions for many of the most common application requirements.

EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. Mercury's FPGA Design Kit (FDK) includes the board's entire FPGA design that can be edited using Altera's Quartus® Prime Software. For all supplied IP, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the factory-installed functions or use Mercury's BSP and FDK to completely replace the IP provided by Mercury with their own.

A/D CONVERTER STAGE

The analog interface accepts analog RF inputs on eight coax connectors located within a VITA 67.3C connector. These inputs are transformer-coupled (2 to 20 GHz bandwidth) into the Agilex 9's A-Tile. Inside the Agilex 9, the analog signals are routed to eight 40 to 64 GSPS, 10-bit A/D converters. The A/D digital outputs are delivered into the programmable logic and processor system for signal processing, data capture or for routing to other resources.

D/A CONVERTER STAGE

The Agilex 9's eight D/A converters accept baseband real or complex data streams from the FPGA's programmable logic. The analog output of each of the 40 to 64 GSPS, 10-bit D/As is transformer-coupled (2 to 20 GHz bandwidth) to a coax connection located within a VITA 67.3C connector.

CLOCKING AND SYNCHRONIZATION

The DRF5270's Timing Bus Circuit can generate all required clocking needed to operate all features of the board. In addition, it can receive a 10 to 100 MHz reference clock from either an on-board synthesizer, the VITA 67.3C connector, or from the VPX-P1 sync bus interface. The Timing Bus Circuit includes a jitter cleaner and provides the reference clock and sync signals to the A-Tile Clock Generator. A multifunction gate/trigger input is also available on one of the VITA 67.3C connectors for external control of data acquisition and playback. For larger systems requiring multiboard synchronization, a multisignal sync bus interface is provided on the VPX P1 connector. These signals include the reference clock and all required complementary timing signals to provide synchronization across multiple boards.

MEMORY RESOURCES

The DRF5270 architecture supports 8 GBytes of DDR4 SDRAM memory accessible from the Programmable Logic. User-installed IP, together with the Mercury-supplied DDR4 controller core within the FPGA, can take advantage of the memory for custom applications. An additional 8 GByte bank of DDR4 SDRAM is available to the Quad-core ARM Cortex-A53 processor as program memory and storage.

1, 10 AND 40 GIGE INTERFACE

The DRF5270 includes 1, 10 and 40 GigE interfaces for control and data transfers. These interfaces are independent of the optical 100 GigE interfaces. The 1 GigE interface provides a direct connection to the ARM processor.

EXPANDABLE I/O

The DRF5270 supports eight 25 Gb/sec full duplex optical lanes to the VITA 67.3C connector. With the built-in dual 100 GigE UDP interface or installation of a user-provided serial protocol, this optical interface enables a high-speed gigabit data streaming path between boards.

FLEXIBLE MODULAR DESIGN

While the DRF5270 follows the form factor of a standard 3U OpenVPX board, the unique modular design of the DRF2270 System on Module (SoM) provides the flexibility to deploy this solution in many different situations. The DRF2270 SoM contains all of the key components including the Agilex 9 FPGA, DDR4 SDRAM, and power and clock management.

In the case of the DRF5270, the SoM is mounted on a SOSA aligned 3U VPX carrier which complements the design with a timing bus circuit, analog signal conditioning, and an 8x 25 Gbps optical transceiver. As a module and carrier board set, the DRF5270 becomes a complete, ready-to-deploy 3U OpenVPX solution available for conduction-cooled SOSA aligned deployment.

The DRF2270 can also be mounted on other carriers available from Mercury to support standard form factors; or for applications that require a non-standard footprint, Mercury supports the module with a design kit for users to engineer and build their own custom carrier. As a complete and tested module, the DRF2270 encapsulates best-in-class electrical and mechanical design, eliminating some of the most challenging aspects of embedded circuit design and allowing the user to focus on the application-specific carrier design.

SPECIFICATIONS

Field Programmable Gate Array

Type: Altera Agilex 9 SoC FPGA AGRW027

Agilex 9 RF Signal Chain

Analog Inputs

- Quantity: 8
- Connector: VITA 67.3C
- Input Type: Transformer-coupled (2 to 20 GHz)

A/D Converters

- Quantity: 8
- Sampling Rate: 40 to 64 GSPS
- Resolution: 10 bits

Analog Outputs

- Quantity: 8
- Connector: VITA 67.3C
- Output Type: Transformer-coupled (2 to 20 GHz)

D/A Converters

- Quantity: 8
- Sampling Rate: 40 to 64 GSPS
- Resolution: 10 bits

Reference Clock

- Source: Switchable between on-board synthesizer, external source, sync bus (used for multiboard sync)
- Connector Type: VITA 67.3C (for external source)

Gate/Trigger:

- Source: Programmable through software or external source
- Connector Type: VITA 67.3C (for external source)
- Level: LVCMOS

Hard Processing System

Quad-core 64-bit ARM Cortex-A53:

- Speed: Up to 1.2 GHz (-2 speed grade)
- -1 Speed: Up to 1.35 GHz (future availability)

Processor I/O:

- Interface: 1 GigE, UART
- Location: VPX-P1

FPGA I/O

Interface: GPIO

- Quantity: 11 Pairs
- Type: LVDS
- Location: VPX-P1

Interface: 10 GigE

- Location: VPX-P1

Interface: 40 GigE

- Location: VPX-P1

Interface: Optical

- Quantity: 8 full duplex lanes
- Connector: VITA 67.3C
- Speed: 25 Gb/sec
- Laser: 850 nm
- Protocol: Factory-installed dual 100 GigE UDP IP cores provide greater than 24 GB/sec data transfers, other protocols supported with user-installed IP

JTAG

Location: VPX-P0 or front panel

Memory

- Type: DDR4 SDRAM
- Quantity: 8 GB, 40 bit
- Quantity: 8 GB, 72 bit

FPGA Configuration FLASH:

- Type: QSPI NOR Flash
- Size: 2 x 1 Gbit

Environmental

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

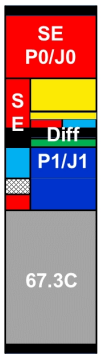
Dimensions: VPX board

- Depth: 170.61 mm (6.717 in)
- Height: 100 mm (3.937 in)

OpenVPX Compatibility

The DRF5270 is compatible with the following module profile, as defined by the VITA 65 OpenVPX Specification:

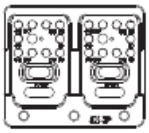
SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11n.



ORDERING INFORMATION

Model	Description
DRF5270	3U VPX SOSA aligned 8-channel A/D and D/A board with Altera Agilex 9 Direct RF

RF AND OPTICAL MODULES

Module Size	VITA 65 Module Designation	Backplane Module Layout	RF Contact Interface	# RF Contacts	# MTs
Full module VITA 65 Aperture H Backplane per VITA 67.3C	6.4.5.6.7	 RF+ Optical	Nano/RF	20	2

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