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Onyx 57751 and 58751

2- or 4-channel 500 MHz A/D, DDC, DUC, 2- or 4-channel 800 MHz D/A
6U VPX board with Virtex-7 FPGA

Complete radar and software radio interface solution

- Radar and communication receiver and transmitter
- Electronic Warfare transponder
- Waveform signal generator
- Wideband data acquisition
- Remote monitoring
- Sensor interfaces

The 57751 and the 58751 consist of one or two 71751 XMC modules mounted on a VPX carrier board. The 57751 is a 6U board with one 71751 module while the 58751 is a 6U board with two XMC modules rather than one.

These models include two or four A/Ds, two or four multiband DDCs, one or two DUCs, two or four D/As and four or eight banks of memory.

FEATURES

- Supports Xilinx® Virtex®-7 VXT FPGA
- GateXpress® supports dynamic FPGA reconfiguration across PCIe
- Two or four 500 MHz 12-bit A/Ds
- Two or four multiband DDCs (digital downconverters)
- One or two DUCs (digital upconverters)
- Two or four 800 MHz 16-bit D/As
- Four or eight GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Xilinx® Virtex®-7 FPGA for custom I/O
- Optional 400 MHz 14-bit A/Ds
- Ruggedized and conduction-cooled versions available

BLOCK DIAGRAM

Click on a block for more information.

Block diagram 57751 shows half of the 58751. All resources are actually double of what is shown except for the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5.
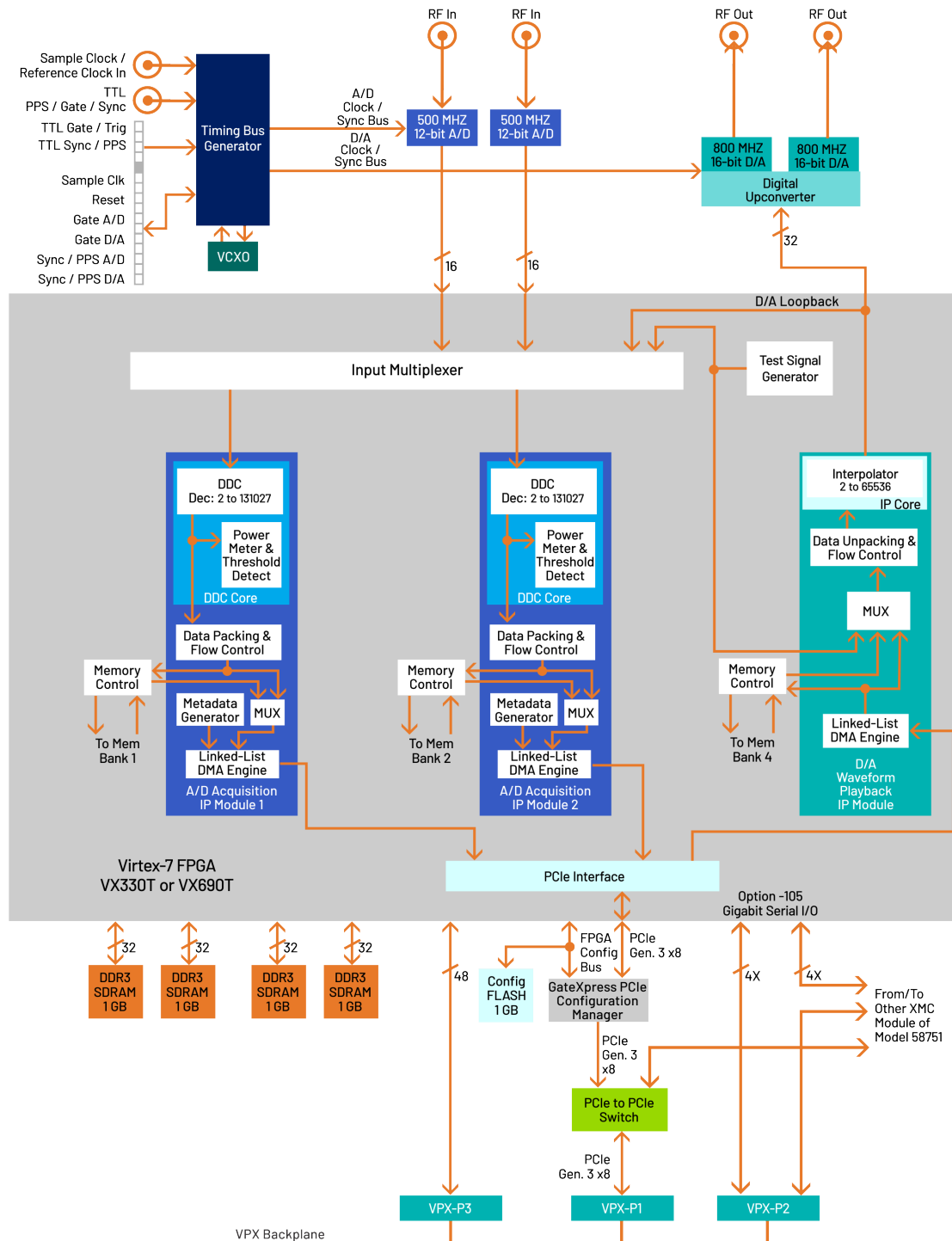
THE ONYX ARCHITECTURE

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions in these models include two or four A/D acquisition and one or two D/A waveform playback IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules.

IP modules for DDR3 memories, controllers for all data clocking and synchronization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as a complete turnkey solutions, without the need to develop any FPGA IP.

XILINX VIRTEX-7 FPGA

The Xilinx Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

A/D CONVERTER STAGES

The board's analog interface accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two or four Texas Instruments ADS5463 500 MHz, 12-bit A/D converters. Optionally, Texas Instruments ADS5474 400 MHz, 14-bit A/Ds may be installed.

The digital outputs are delivered into the Xilinx® Virtex®-7 FPGA for signal processing, data capture and for routing to other board resources.

A/D ACQUISITION IP MODULES

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP Module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP CORES

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A WAVEFORM PLAYBACK IP MODULE

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

DIGITAL UPCONVERTER AND D/A STAGE

One or two Texas Instruments DAC5688 DUCs (digital upconverters) and D/As accept the baseband real or complex data stream from

the FPGA and provide that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog outputs are through front-panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

CLOCKING AND SYNCHRONIZATION

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

MEMORY RESOURCES

The architecture of these models supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI EXPRESS INTERFACE

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

GATEXPRESS FOR FPGA CONFIGURATION

The Onyx architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting. Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image:

- The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

- The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

- The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without a host computer reset to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

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READYFLOW

Mercury provides ReadyFlow® BSPs (Board Support Packages) for all Cobalt, Onyx, and Flexor products. Available for both Linux and Windows, these packages:

- Provide a path for quick start-up through application completion
- Allow programming at high, intermediate and low levels to meet various needs
- Are illustrated with numerous examples
- Include complete documentation and definitions of all functions
- Include library and example source code.

ReadyFlow BSPs contain C-language examples that can be used to demonstrate the capabilities of Cobalt, Onyx, and Flexor products. These programming examples will help you get an immediate start on writing your own application. They provide sample code that is known to work, giving you a means of verifying that your board set is operational.

COMMAND LINE INTERFACE

The Command Line Interface provides access to pre-compiled executable examples that operate the hardware right out of the box, without the need to write any code. Board-specific hardware

operating arguments can be entered in the command line to control parameters: number of channels to enable, sample clock frequency, data transfer size, reference clock frequency, reference clock source, etc.

The Command Line Interface can be used to call an example application from within a larger user application to control the hardware, and parameter arguments are passed to the application for execution. Functions that control data acquisition automatically save captured data to a pre-named host file or are routed to the Signal Analyzer example function for display.

SIGNAL ANALYZER

When used with the Command Line Interface, the Signal Analyzer allows users to immediately start acquiring and displaying A/D data. A full-featured analysis tool, the Signal Analyzer displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD, and SINAD. Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals.

GATEFLOW

The GateFlow® FPGA Design Kit (FDK) allows the user to modify, replace and extend the standard installed functions in the FPGA to incorporate special modes of operation, new control structures, and specialized signal-processing algorithms.

The Cobalt (Virtex-6), Onyx (Virtex-7), and Flexor (Virtex-7) architectures configure the FPGA with standard factory-supplied interfaces including memory controllers, DMA engines, A/D and D/A interfaces, timing and synchronization structures, triggering and gating logic, time stamping and header tagging, data formatting engines, and the PCIe interface. These resources are connected to the User Application Container using well-defined ports that present easy-to-use data and control signals, effectively abstracting the lower-level details of the hardware.

The User Application Container

Shown below is the FPGA block diagram of a typical Cobalt, Onyx or Flexor module. The User Application Container holds a collection of different installed IP modules connected to the various interfaces through the standard ports surrounding the container. The specific IP modules for each product are described in further detail in the datasheet of that product.

The GateFlow FDK provides a complete Xilinx's ISE or Vivado project folder containing all the files necessary for the FPGA developer to recompile the entire project with or without any required changes. VHDL source code for each IP module provides excellent examples of how the IP modules work, how they might be modified, and how they might be replaced with custom IP to implement a specific function.
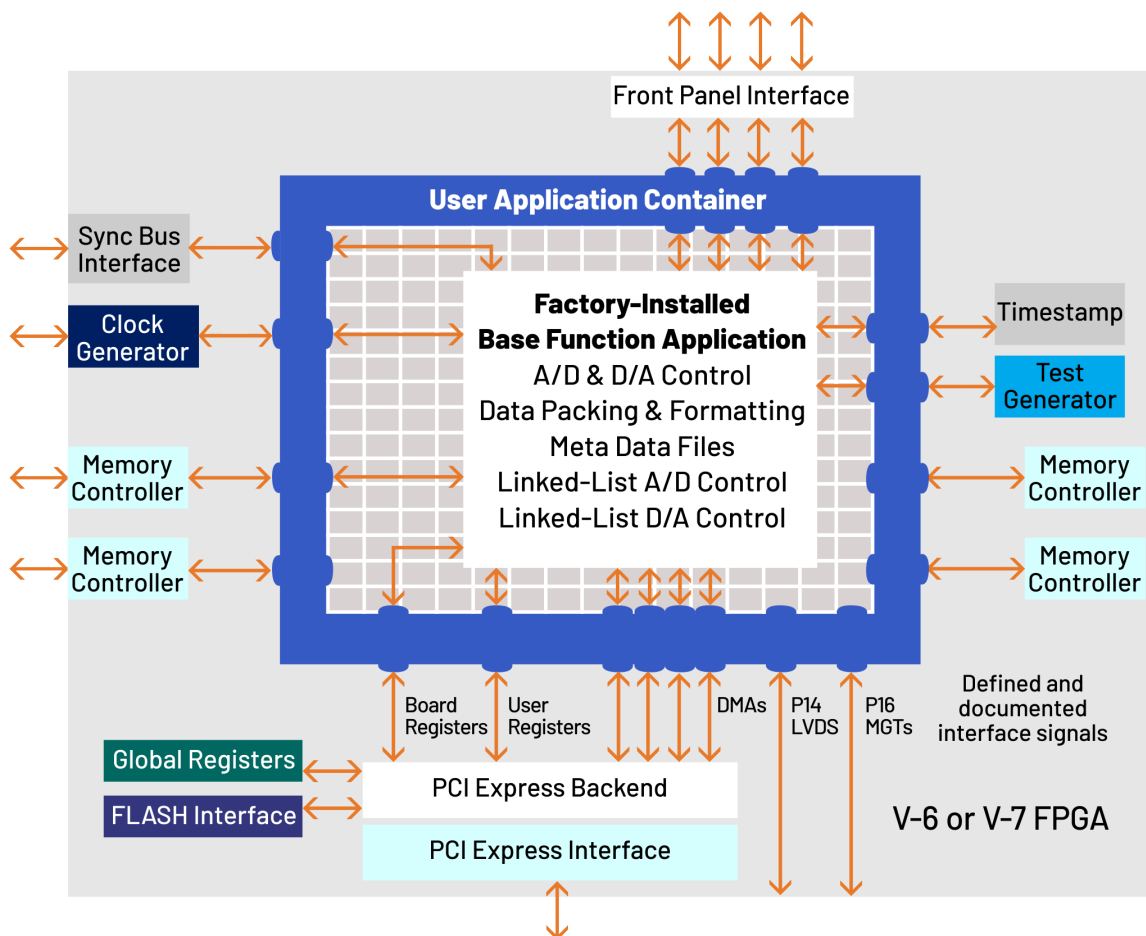
FRONT PANEL CONNECTIONS

The XMC front panel includes six SSMC coaxial connectors and a 26-pin Sync Bus connector for input/output of timing and analog signals. The front panel also includes nine LEDs.
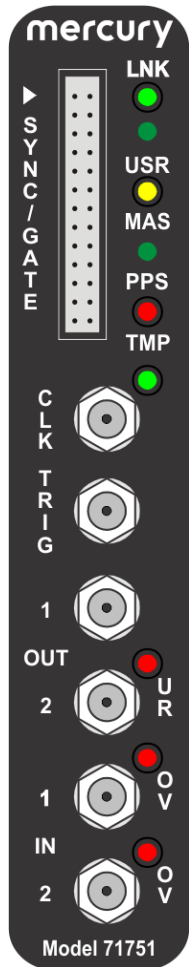
- **Sync Bus Connector:** The 19-pin Sync Bus front panel connector, labeled **SYNC/GATE**, provides clock, sync, and gate input/output pins for the Sync Bus.

- **Link LED:** The green **LNK** LED blinks when a valid link has been established over the PCIe interface.

- **User LED:** The green **USR** LED is for user applications.

- **MAS LED:** The yellow **MAS** LED illuminates when this model is the Sync Bus Master.

- **PPS LED:** The green **PPS** LED illuminates when a valid PPS signal is detected. The LED will blink at the rate of the PPS signal.

- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the Model PCB.

- **Clock Input Connector:** One SSMC coaxial connector, labeled **CLK**, for input of an external sample clock.

- **Trigger Input Connector:** The SSMC coaxial connector labeled **TRIG** is for input of an external trigger. The signal must be a LVTTL signal.

- **Analog Output Connectors:** Two SSMC coaxial connectors for analog signal outputs are labeled **OUT 1** and **2** for each DAC5688 output.

- **DAC Underrun LED:** The red **UR** underrun LED illuminates when the DAC5688 FIFO is out of data.

- **Analog Input Connectors:** Two SSMC coaxial connectors, labeled **IN 1** and **IN 2** are for each ADC12D1800 input channel.

- **ADC Overload LED:** Two red **OV** (overload) LEDs for each A/D input.

SPECIFICATIONS

57751: 2 A/Ds, 2 DDCs, 1 DUC, 2 D/As

58751: 4 A/Ds, 4 DDCs, 2 DUCs, 4 D/As

Front Panel Analog Signal Inputs (2 or 4)

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +5 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard) (2 or 4)

Type: Texas Instruments ADS5463

Sampling Rate: 20 MHz to 500 MHz

Resolution: 12 bits

A/D Converters (option –014) (2 or 4)

Type: Texas Instruments ADS5474

Sampling Rate: 20 MHz to 400 MHz

Resolution: 14 bits

Digital Downconverters (2 or 4)

Decimation Range: 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage

LO Tuning Freq. Resolution: 32 bits, 0 to f_s

LO SFDR: >120 dB

Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters (2 or 4)

Type: Texas Instruments DAC5688

Input Data Rate: 250 MHz max.

Output IF: DC to 400 MHz max.

Output Signal: 2-channel real or 1-channel with frequency translation

Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation

Resolution: 16 bits

Digital Interpolators (1 or 2)

Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Total Interpolator Range (D/A and Digital Combined)

2x to 524,288x

Front Panel Analog Signal Outputs (2 or 4)

Output Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources (2 or 4)

On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock (1 or 2)

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference

Timing Bus (1 or 2)

26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays

(1 or 2)

- Standard: Xilinx Virtex-7 XC7VX330T-2

- Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O

- Option -104: Installs the PMC P14 connector with 24 LVDS pairs to the FPGA

- Option -105: Provides one 8X or two 4X gigabit links between the FPGA and VPX P1 connector to support serial protocols.

Memory Banks (4 or 8)

Type: DDR3 SDRAM

Size: 1 GB each

Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C

- Storage Temp: -20° to 90° C

- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C

- Storage Temp: -40° to 100° C

- Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C

- Storage Temp: -50° to 100° C

- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions

- Depth: 170.6 mm (6.717 in.)

- Height: 100 mm (3.937 in.)

Weight: VPX Carrier: 110 grams (3.9 oz)

Model	Description
57751	2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA 6U VPX
58751	4-Channel 500 MHz A/D with DDCs, DUCs with 4-Channel 800 MHz D/A, and two Virtex-7 FPGAs 6U VPX

Options	Description
-014	400 MHz, 14-bit A/Ds
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O between the FPGA and P3 connector, 57751; P3 and P5 connectors, 58751
-105	Gigabit link between the FPGA and P2 connector, 57751; gigabit links from each FPGA to P2 connector, 78751
-702	Air-cooled, Level 2
-763	Conduction-cooled, Level 3

Contact Mercury for compatible option combinations.

ACCESSORY PRODUCTS

Model	Description
2171	Cable Kit: SSMC to SMA

FORM FACTORS

Onyx products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Onyx Model 71751 XMC (2-Channel 500 MHz A/D with DDC and 2-Channel 800 MHz D/A with DUC, Virtex-7 FPGA) has the following variants:

Model	
52751	3U VPX board (single XMC)
57751	6U VPX board (single XMC)
58751	6U VPX board (dual XMC)
71751	XMC module
78751	PCIe board (single XMC)

DEVELOPMENT SYSTEMS

Mercury offers development systems for Onyx products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Onyx boards. Please contact Mercury to configure a system that matches your requirements.

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