DATASHEET

Ensemble 6000 Series OpenVPX Intel 2nd Generation Core i7 Quad-Core LDS6522 Module

- **6U OpenVPX™-compliant VITA 65/46/48 (VPX-REDI) module**
- **High-performance Intel® 2nd Generation Core™ i7 (Sandy Bridge mobile-class) quad-core-processor**
- **Up to 2.1 GHz with 134 GFLOPS peak performance**
- **Serial RapidIO® and/or 10 Gigabit Ethernet fabric enabled**
- **Integrated 80-lane PCIe® switching infrastructure**
- **On-board and off-board co-processing expansion plane communications**
- **Mercury MultiCore Plus® software infrastructure support**

The Ensemble™ 6000 Series OpenVPX Intel Core i7 Quad-Core Next Generation LDS6522 Module from Mercury Computer Systems combines a powerful Sandy Bridge mobile-class quad-core Intel 2nd Generation Core i7 processor, a high-performance FPGA for both fabric bridging and user-application functions, and high-bandwidth on-board and off-board communication fabrics in a single 6U OpenVPX slot. The LDS6522 provides a next-generation architecture that balances the disruptive computational capa-bilities of the Intel 2nd Generation Core i7 processor with key high-bandwidth I/O interfaces, providing a powerful and scalable computing architecture that is well aligned with demanding high-end defense and commercial applications.

Intel 2nd Generation Core i7 Sandy Bridge Mobile-Class Processor

At the heart of the LDS6522 is the Intel 64-bit 2nd Generation Core i7 2715QE processor, running at up to 2.1 GHz. This processor is based on the Sandy Bridge processor architecture, which includes the revolution-ary Intel Advanced Vector Extensions (AVX) instruction set. The AVX instruction set doubles the width of the processor's SIMD engine from 128-bit to 256-bit, delivering a significant improvement in floating-point processing. Simultaneously, the 2715QE processor doubles the number of cores on-chip from 2 to 4. The combination of these two architectural advancements results in the LDS6522 delivering approximately 134 peak GFLOPS. The 2715QE includes a large 6 MB cache shared between the cores, allowing many high-performance calculations to remain cache resident. This accelerates processing by eliminating the potential latency required to access DRAM to fetch upcoming data. The Intel 2nd Generation Core i7 2715QE processor upports dual high-speed DDR3-1333 memory controllers, providing up to 21 GB/s of raw memory bandwidth. Up to 8 GB of DDR3 SDRAM with ECC support can be populated on the LDS6522. The LDS6522 makes use of the Cougar Point-M HM65 Platform Controller Hub (PCH) chipset, which provides integrated graphics capabilities along with I/O bridging between the Intel processor and external devices.

High-Speed Fabric Interfaces

The LDS6522 combines the processing power of the Core i7 family from Intel with a high-speed Serial RapidIO or 10 Gigabit Ethernet fabric interface. The on-board Altera Stratix IV FPGA can be configured with IP that provides a streaming bridge for high-bandwidth, low-latency data. The LDS6522 supports either Serial RapidIO (Gen1 or Gen2) or 10 Gigabit Ethernet bridging to the native PCIe interface on the Intel chipset. By linking the Intel 2nd Generation Core i7 processor with a high-performance OpenVPX data plane, the LDS6522 architecture ensures an optimal balance between I/O and processing capabilities. Unused resources within the FPGA are available to customers who wish to enhance the LDS6522 with additional FPGA-based capabilities.

PCI Express Architecture

The LDS6522 provides an 80-lane PCI Express® switch for both on-board switching and off-board expansion. This Gen2 switch provides a x8 PCIe interface to each of the two XMC sites as well as a x4 connection to the single PMC site via a PCI-X® to PCIe bridge. This allows mezzanines to operate at full bandwidth, optimizing the flow of I/O into the processing subsystem. Additional x4 interfaces are provided to the on-board FPGA, allowing bridging to the data plane. Externally, the LDS6522 implements

a full x16 PCIe connection to the OpenVPX expansion plane on the P2 VPX connector. This expansion plane interface enables the LDS6522's compatibility with Mercury's GPU or FPGA based co-processing modules.

The x16 PCIe® connection can be user configured as dual x8 connections. These configuration options let the module effectively act as an upstream/downstream PCIe switch, allowing "chaining" of PCIe devices. Finally, an additional x8 PCIe interface is routed to the VPX P5 connector.

Mezzanine Card Flexibility

The LDS6522 provides two mezzanine sites, one PMC/XMC site and one XMC only site. Each of the standard mezzanine sites on the LDS6522 module can be configured with off-the-shelf mezzanine cards to bring additional I/O into the system for processing or control. PMC cards are supported with a PCI®/PCI-X® interface at up to 133 MHz on the PMC/XMC site, with PMC user-defined I/O mapped to the backplane. XMCs are supported with x8, x4 and x1 PCIe (Gen1 or Gen2) supported on the J15/J25 connector per the VITA 42.3 standard. Twenty differential pairs of XMC user I/O is mapped to the backplane via the J16/J26 connector.

Multiple I/O Options

In addition to the flexibility offered via the on-board mezzanine sites, the LDS6522 offers a variety of additional built-in I/O options:

- One 10/100/1000BASE-T Gigabit Ethernet connection routed to the front panel on air-cooled configurations or to the backplane on conduction-cooled configurations
- One additional 10/100/1000BASE-T Gigabit Ethernet connection routed to the backplane
- Two 1000BASE-BX SERDES Ethernet connections routed to the backplane as per the OpenVPX™ control plane specification
- A DVI graphics interface is routed to the backplane, allowing the LDS6522 to provide a full graphical display if needed by the application
- One RS-232 serial port is routed to the front panel on air-cooled configurations, or to the backplane on conduction-cooled configurations. When routed to the backplane, the serial interface can be configured for either RS-232 or RS-422 signaling.
- One front panel USB 2.0 interface on air-cooled configurations only
- Two backplane USB 2.0 interfaces, available with both air-cooled and conduction-cooled configurations.
- Two SATA interfaces to the backplane are provided to easily interface with storage devices.
- Eight GPIO lines act as discrete I/O, usable as input, output, or to generate interrupts on the module.
- Several additional bused signals that enhance the functionality of the LDS6522 module.

System Management Plane

The LDS6522 module implements the advanced system management functionality architected in the OpenVPX specification to enable remote monitoring, alarm management, and hardware revision and health status.

Using the standard I2C bus and IPMI protocol, the on-board system-management block implements the Intelligent Platform Management Controller (IPMC), in accordance with the VITA 46.11 standard. This allows the LDS6522 module to:

- Read sensor values
- Read and write sensor thresholds, allowing an application to react to thermal, voltage or current variations that exceed those thresholds
- Reset the entire module
  Power up/down the entire module
  Retrieve module field replaceable unit (FRU) information
- Be managed remotely by a Chassis Management Controller at the system level, such as implemented Mercury's OpenVPX SFM family of switch modules

Additional Features

The LDS6522 module provides all the features typically found on a single-board computer. In addition to the sophisticated management subsystem and fabric interconnect, the LDS6522 module provides users with a toolkit enabling many different application use cases. Features include:

- Thermal and voltage sensors integrated on-board
- Real-time clock with granularity to 1 ms and time measurement of up
- to 30 years
- General-purpose timers for synchronization
- Watchdog timer to support processor interrupt or reset
- Multiple boot paths, include netboot, USB boot, boot from SATA, or from the on-board 4GB flash device

Open Software Environment

Mercury leverages over 25 years of multicomputer software expertise, including recent multicore processor expertise, across its many plat-forms. This strategy is fully applied to the LDS6522 module. Because the processor, memory and surrounding technologies are leveraged across product lines, software developed on the LDS6522 module can interface seamlessly with other Mercury products. The same development and run-time environment is implemented on the LDS6522 module as on other Mercury Intel®-based platforms across the Ensemble™ 3000, 5000 and 6000 series.

A key software package available for the LDS6522 module is the Scientific Algorithm Library (SAL). SAL offers the legacy SAL API interface, but is optimized for the APX capabilities of the multiple on-chip cores available with the Intel Core™ i7 quad-core processor.

Software support is available on the LDS6522 for the following products:

- Support for Mercury's standard numeric libraries, VSIPL and SAL (Scientific Algorithm Library), as well as their multi-core variants, is optimized for the Intel 2nd Generation Core i7 architecture of the LDS6522 module.
- Open Development Suite for Linux® is an Eclipse-based integrated development environment that includes a C/C++ optimizing compiler, a source-level debugger, a language-sensitive text editor, a performance profiler, a project builder, a version control system, a run-time error checker and a graphical source browser. Mercury provides extensions that allow multiprocessor-aware process launch and debug, as well as a System Dashboard view that allows graphical remote management.
- Support is provided for Wind River® Workbench integrated development environment when the module is running Wind River Linux® or VxWorks®.
- Interprocessor Communication System (ICS) support is carried forward from the RACE++®/MCOE™ software environment. ICS provides a low-level interprocessor communication API that lets users take advantage of the high-bandwidth, low-latency data plane fabric with an easy-to-use software interface.
- Trace Analysis Tool and Library (TATL™) is a "logic analyzer for software" that provides insight into the dynamic interaction of up to a few hundred processors.
  The MCP software environment lets applications use industry-standard middleware such as MPI, DRI, CORBA, or standard TCP/IP sockets ported to run seamlessly over the fabric. MCP also offers a software tool that can help to migrate legacy applications created with MCOE into the MCP domain.

Open Standards Mean Interoperability and Planning for the Future

The OpenVPX™ Industry Working Group is an industry initiative launched by defense prime contractors and COTS system developers, to take a proactive approach to solving the interoperability issues associated with the VITA 46 (VPX) family of specifications. This group has created an overarching System Specification defining VPX system architecture through pinout definitions to establish a limited set of application- specific reference solutions. These OpenVPX standard solutions provide clear design guidance to COTS suppliers and the user community, assur-ing interoperability across multi-vendor implementations. The OpenVPX System Specifications were ratified by the VSO in February 2010.

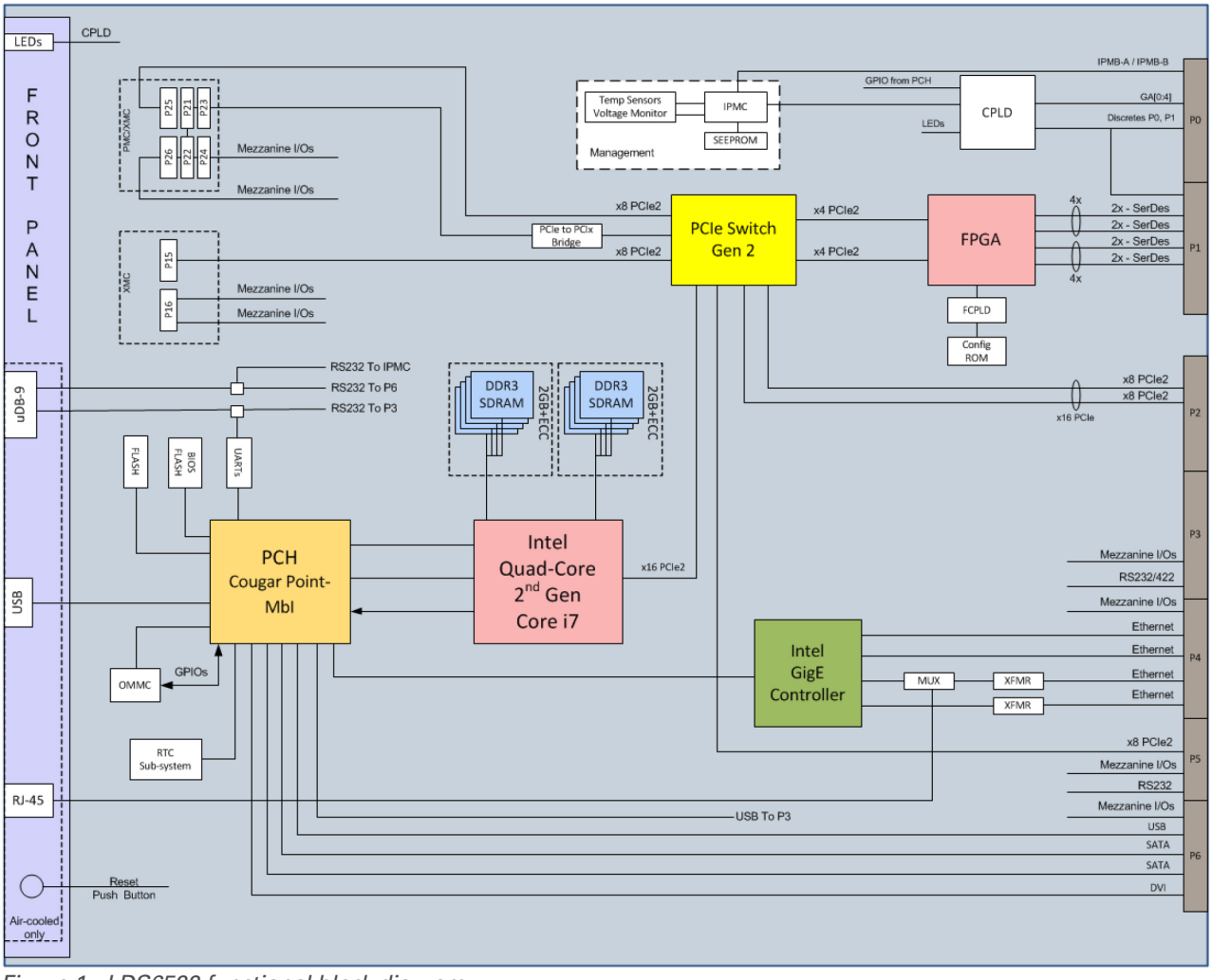

Figure 1 - LDS6522 functional block diagram

Specifications

Intel Sandy Bridge Mobile-Class 32-nm Processor

Dual-core	2.1 GHz
Peak performance	134 GFLOPS (peak theoretical)
Threads per core	
Intel® Virtualization Technology	2
DDR3-1333	4 GB with ECC (up to 8 GB future capability)
Raw memory bandwidth	21 GB/s
BIOS SPI flash	2 x 8 MB
NAND flash	4 GB

Altera Stratix® IV EP4SGX180 FPGA

Logic elements	175,000
Internal memory	11.7 Mb
18x18 multipliers	920
SerDes	16
Each Serdes	600 Mbp to 6.25 Gpbs
184 GMACs	200 MHz

Provides fabric bridging to data plane

Can act as co-processor to execute iFFT/FFT, image or signal processing

Configured from CPU or dedicated configuration ROM

IPMI (System Management)

On-board IPMI Controller
Voltage and temperature monitor

Geographical address monitor
Power/reset control

FRU and on-board EEPROM interfaces
FPGA, CPU and CPLD interfaces

OpenVPX Multi-Plane Architecture

System Management via IPMB-A and IPMB-B link on P0 management plane

Dual 4x serial RapidIO® or 10 Gigabit Ethernet interfaces on P1 data plane

Full x16 or dual x8 PCIe® expansion plane

Dual 1000BASE-BX Ethernet control plane

Power/reset contro

FRU and on-board EEPROM interfaces

FPGA, CPU and CPLD interfaces

Ethernet Connections

Two 1000BASE-BX Ethernet to P4 connector

OpenVPX™ Control Plane

One 10/100/1000BASE-T Ethernet to P4 connector

Accessible via OpenVPX RTM or external chassis interface

One 10/100/1000BASE-T Ethernet connection to front panel (air-cooled module) or backplane (conduction-cooled module

Ethernet functions supported by the chipset include:

UDP, TCP, SCTP, ARP, IPv4, IPv6, IEEE1588, flow control, 802.1P (priority) and 802.1Q (VLAN)

PMC-X/XMC Sites

Mezzanine sites	1 PMC/XMC, 1 XMC only
PCI-X™-to-PCIe bridge	Connects PMC site to on-board PCI Express® switch
PMC PCI™ support	33 and 66 MHz
PMC PCI-X® support	66, 100, and 133 MHz

PMC user-defined I/O from P4 to backplane

PCIe XMC sites per VITA 42.3 with XMC user-defined I/O from J6 to backplane

Additional I/O Capabilities

1 RS-232 serial interface to front panel (air-cooled) or backplane (conduction-cooled)

Configurable for RS-422 signaling when routed to backplane

One front-panel USB 2.0 interface (air-cooled configurations only)

Two USB 2.0 interfaces to backplane

Two SATA interfaces to backplane

8 single-ended GPIO interfaces to backplane

System signals to backplane

NVMRO, ChassisTest, Environmental Bypass, MemoryClear

Mechanical

6U VPX (air-cooled)

1.0" slot pitch

OpenVPX and VPX REDI

Environmental Specs (Air-Cooled Version)

Operating Temp	-0°C to +40°C
Storage Temp	-40°C to +85°C
Operating Humidity	10-90%, non-condensing
Vibration	0.003 g2/Hz; 20 to 2000 Hz, 1 hr/axis
Shock	20g, z-axis; 32g, x-, y-axes; 11 ms half-sine
Operating Altitude	0-10,000 ft*

*Customer must maintain required cfm level.

Compliance

OpenVPX™ System Specification encompasses VITA 46.0, 46.3, 46.4, 46.6, 46.11

Compatible with VITA 65

VITA 46/48.1/48.2 (REDI)

Serial RapidIO®, PCI Express®, 10 Gigabit Ethernet

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