DATASHEET

Ensemble® IOM-141 Streaming I/O XMC

Quad Channel Fiber-Optic Serial Front Panel Data Port (SFPDP)

- **Full-duplex 247 MB/s peak I/O per channel**
- **Fiber connections distances up to 150 meters**
- **Real-time latency as low as 4 µs**
- **Supports all four Front Panel Data Port (FPDP) data modes**
- **Ideal for streaming data input**
- **Two DMA engines per channel (send and receive)**

Mercury Systems brings enhanced performance and flexibility to external I/O with the Ensemble IOM-141 Streaming I/O XMC (Switched Mezzanine Card, VITA 42.2-2006). Providing 2.5 Gbaud of full-duplex bandwidth per channel and four channels per card, the IOM-141 XMC offers high levels of speed and connection density. With fiber connection distances of up to 150 meters and with a latency as low as 4 µs, it is ideally suited as the real-time digital interface for sensor input or data output in a high-performance embedded system.

Compatibility

The IOM-141 XMC implements the Serial Front Panel Data Port (SFPDP) protocol, as specified by VITA 17.1-2003. It supports all four SFPDP framing modes. This implementation of the standard makes the IOM-141 XMC compatible with products supporting any subset of the VITA 17.1-2003 protocol.

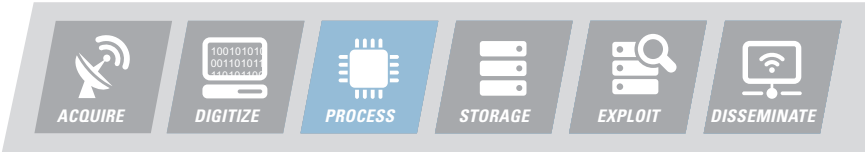
The IOM-141 XMC is software compatible with RACE++ Series RINOJ-F and the IOM-140 XMC products, easing migration from the legacy I/O daughter cards while offering significant improvements in speed as well as configuration flexibility. The IOM-141 is compatible with Mercury's Intel®-based OpenVPX™ products, interacting with Intel module's on-board Protocol Offload Engine Technology (POET™) technology (when configured to bridge to Serial RapidIO®) to stream I/O directly to and from the XMC to any fabric-attached endpoint in the system. functions.

I/O Intelligence

The IOM-141 XMC is more than an ordinary digital interface: each channel can be programmed for data distribution without processor intervention. Although the data destination is typically a PCIe® targeted memory, with Mercury's system focused approach and drivers, destinations may be anywhere where fabric based connectivity exists, even when mode changes are called for (e.g. at a Serial RapidIO destination via a POET enabled PCIe bridge).

The IOM-141 can inspect the input data stream that indicate sensor mode changes and route data appropriately for each different mode. Each mode can be made to correspond with an application-defined Direct Memory Access (DMA) Command Packet (CP) chain. These command packets cause the channel's DMA controller to route the data to a predefined destination anywhere within the system's switch fabric. This data-driven distribution takes advantage of information available at the source. DMA command packets can be chained together to automatically distribute sequential data packets to different processors or endpoints.

Mercury Systems is a best-of-breed provider of commercially developed, open sensor and Big Data processing systems, software and services for critical commercial, defense and intelligence applications.



Synchronization between the Sensor I/O XMC and the application program can be accomplished by queuing a transfer request that includes status information at the desired synchronization point in the DMA chain. This block of status information is written to the local memory of the synchronizing processor. The processor can then poll on the receiving memory location for block of status information. The Sensor I/O XMC also can be synchronized with a processor via mailbox interrupts.

Serial FPDP Interface

Serial FPDP supports a mapping of the FPDP protocol onto the Fibre Channel physical layers (FC-0 and FC-1). Serial data is trans-mitted at 2.5 Gbaud over the fiber. The IOM-141 XMC achieves a sustained data rate of 247 MB/s per channel when the data packets are kept large on both the fiber side and the XMC con-nector side of the interface.

The serial protocol provides optional error checking and flow control. The optional error checking is accomplished with a Cyclic Redundancy Check (CRC-32) included in each packet sent over the serial line. The optional flow control feature enables the receiving end of the fiber interface to send flow control commands through its output port back to the data transmitter. If flow control is not used, only a single fiber per data channel is required.

The IOM-141 XMC converts four channels of full-duplex serial FPDP data into a single PCIe channel, which is then routed through the host module's on-board POET™ interface to the system's Serial RapidIO data plane. This device is implemented as a switched mezzanine card (XMC) and occupies an XMC compatible site on any modules supporting PCIe over the Jn5 connector.

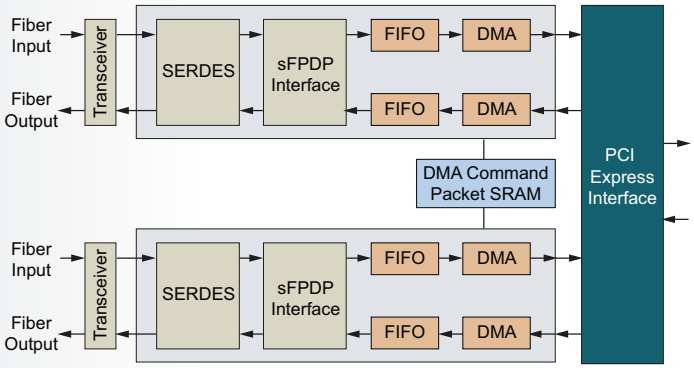


Figure 1. *XMC Channel block diagram*

Linked-List DMA Controller

The IOM-141 XMC daughter card includes a linked-list DMA controller for intelligent control of data distribution. Lists of DMA command packets control the linked-list DMA controller. Since they are constructed once at setup time and can be initiated multiple times within the time-critical portion of the application, such chains of transfer requests are very valuable for repetitive, high-speed transfers. In many applications, once the DMA controller is set up it can run autonomously, scattering or gathering data among a large number of processing nodes with no processor intervention.

I/O Management Software

Mercury provides a data transfer facility layered on top of the standard Mercury Interprocessor Communication System (ICS). This facility consists of a set of user-callable I/O control functions. These functions are used to define I/O transfer requests (DMA command packets) and to link such requests into a chain that is then automatically executed by the designated I/O device.

Although the IOM-141 is a PCIe XMC, it interfaces directly with the Intel module's POET interface to Serial RapidIO directly. Each CP specifies the target's Serial RapidIO ID, address and maximum word count for the transfer as well as some control information. The route in each CP can specify either a single Serial RapidIO endpoint or, in the case of an input stream, multiple Serial RapidIO endpoints. By chaining command packets together into a linked list, an incoming stream can be parceled out among a large number of endpoints. Transfers of up to 4 GB in length may be implemented.

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Data Frame Management

The IOM-141 XMC allows the sensor to frame the data into "epochs." Any sensor can define its own epoch boundary based on what makes sense for that type of sensor and on how the data will be used by the processing system. In the case of radar data, these epochs are likely to be coherent processing intervals. In the case of images, an epoch is likely to be a line or a frame of an image. The IOM-141 XMC supports the four SFPDP framing options: Unframed, Single-Frame Data, Dynamic-Size Repeating Frame Data and Fixed-Size Repeating Frame Data.

Data-Driven Frame Processing

Many modern sensors change modes during operation. When a sensor changes modes, the processing system must make the corresponding mode change at the correct time. The sensor can also use the first word of each epoch to indicate its current mode. The IOM-141 XMC in "cable header" mode may use this word to index to a particular DMA command packet chain, then initiate the chain without processor intervention (see Figure 2). This allows each configuration of the sensor to have a dedicated DMA chain and a completely different data distribution from other modes.

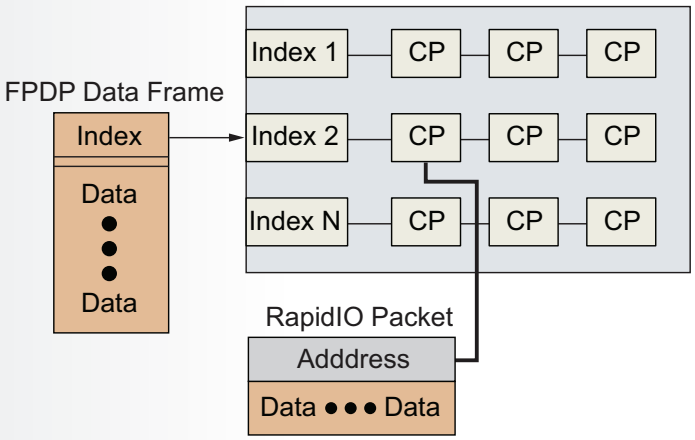

Figure 2. *XMC DMA CP Chain*

When the sensor mode changes are known in advance, the IOM-141 XMC can be programmed to switch DMA chains for the next mode through the use of branching at the end of an SFPDP frame or epoch. This branching capability can also be used for error handling when the end of the SFPDP frame occurs before it is expected.

Recovering From Input Stream Faults

With some input interfaces, missing or extra data can cause the interface to lose sync with an input data stream until a processor intervenes. The IOM-141 XMC minimizes the system upset by localizing the effects of anomalies in the input stream. To do this, the XMC can re-synchronize its DMA controller to the incoming data at each data frame (epoch boundary). This re-synchronization is done by the hardware, with no processor intervention.

In the event that an end-of-epoch marker is lost due to a media error, the maximum word count in the DMA CP will prevent data from being written past the end of the buffer.

Conquering Latency

The IOM-141 XMC can be configured to give a latency of less than 4 µs from when data arrives at the interface to when it is on a processing node ready to be processed. The main feature that enables this low latency is the linked-list DMA CP processing of the XMC's DMA controller. By cycling through lists of DMA commands created during initialization, the IOM-141 XMC can autonomously distribute the data without any processor intervention.

Two additional features ensure that low-latency operation is maintained. First, a programmable threshold is used to tell the DMA controller when it should start emptying its input FIFO. If the FIFO has more than the specified amount of data, the DMA controller will start emptying the FIFO. Second, the Sensor I/O XMC includes a programmable timer that will cause any remaining data to be emptied from the input FIFO if no input data arrives for the specified length of time.

Sensor I/O XMC Full-Duplex Operation

Each interface can operate in full-duplex mode. In addition, there are separate DMA controllers for transmit and receive on each channel — 2 DMA controllers per channel (8 per card). On each channel, transmit and receive can be synchronized, if desired.

Sensor I/O XMC Copy Mode

The IOM-141 XMC can also loop any data arriving through its receive fibers directly onto its corresponding transmit fiber. Copy mode is useful for systems in which it is desirable to record the incoming data. When copy mode is enabled, the data can be both distributed to nodes by the Sensor I/O XMC as well as passed on to another device or chassis for recording.

Specifications

Configuration

4 channels

PCIe (Gen 1) x8 interface to XMC Jn5 connector

Media	62.5/125 or 50/125 micron
Wavelength	850 nm
Connector type	LC
Distance	Up to 150 meters, depending on configuration

Configuration Requirements

Ensemble 6000 Series Intel-based Hardware

Software Support

MultiCore Plus for Ensemble 6000 Intel-based Systems

IOM-141 XMC daughter cards include a driver software package for MCP, and require the ICS package.

Electrical

FIFO/channel

Input	16K x 35 bits
Output	2K x 34 bits

DMA command packets SRAM	128K x 32 bits per channel
Data rate	2.500 Gbaud or 1.0625 Gbaud
Power dissipation	12W-14W for 4-channel (typical)

Mechanical

XMC style daughter card 6.5" x 2.9"

Compliance

OpenVPX System Specification encompasses

VITA 46.0, 46.3, 46.4, 46.6, 46.7, 46.9, 46.11

Compatible with VITA 65

VITA 48/48.1/48.2 (REDI)

PCIe

Environmental

See Environmental Protections for Operation at the Tactical Edge for specific ruggedness levels and cooling options.

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