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Cobalt 57624/58624

2-or 4-channel, 34- or 68-signal adaptive IF relay 6U VPX boards with Virtex-6 FPGA

Supports many functions for commercial and military communications

- Signal drop/add/replace
- Frequency shifting and hopping
- Amplitude equalization
- Bandwidth consolidation
- Applications include signal monitoring, signal jamming, channel security, countermeasures, beamforming, and radar

Models 57624 and 58624 consist of one or two Model 71624 XMC modules mounted on a VPX carrier board. Model 57624 is a 6U board with one Model 71624 module while the Model 58624 is a 6U board with two XMC modules rather than one.

As IF relays, they accept two or four IF analog input channels, modify up to 34 or 68 signals, and then deliver them to two or four analog IF outputs. Any signal within each IF band can be independently enabled or disabled, and changed in both frequency and amplitude as it passes through the board These models support many useful functions for both commercial and military communications systems including signal drop/add/replace, frequency shifting and hopping, amplitude equalization, and bandwidth consolidation. Applications include countermeasures, active tracking and monitoring, channel security, interception, adaptive spectral management, jamming, and encryption.

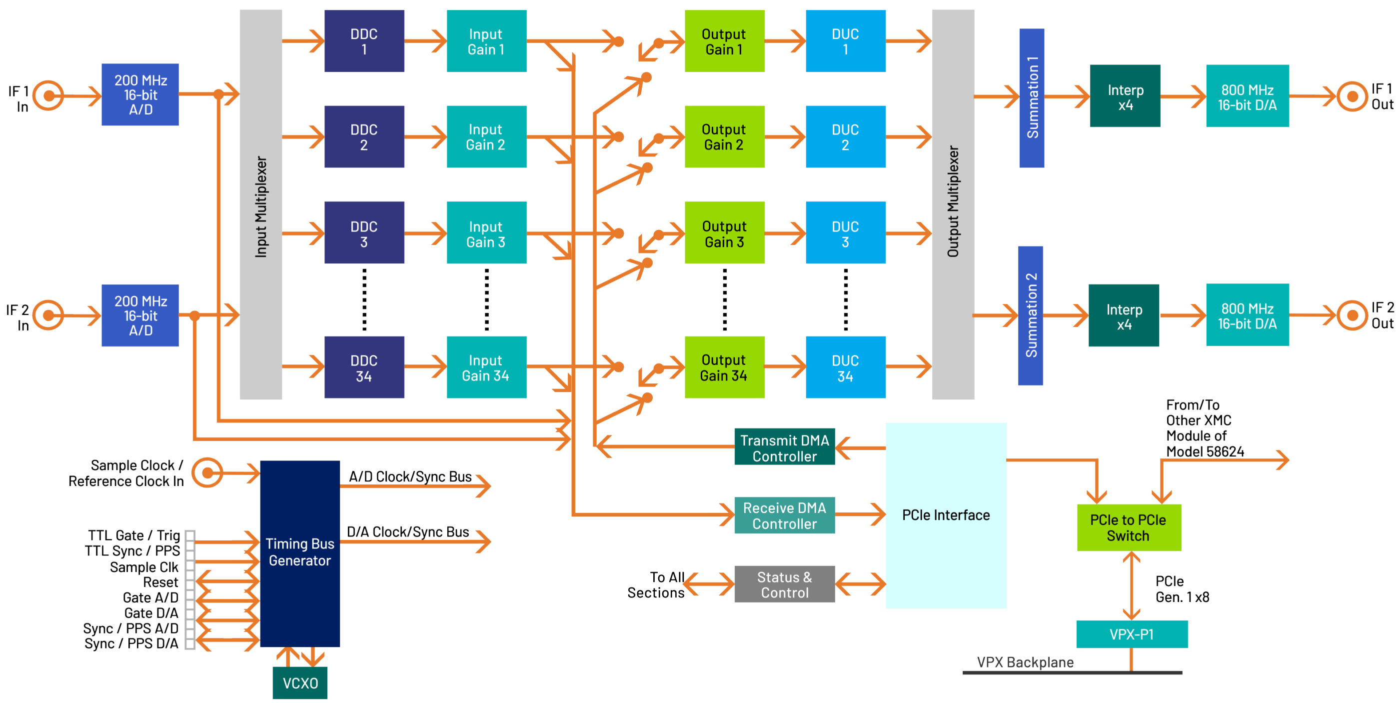
FEATURES

- Modifies 34 or 68 IF signals between input and output
- Up to 80 MHz IF bandwidth
- Two/four 200 MHz 16-bit A/Ds
- Two/four 800 MHz 16-bit D/As
- 34/68 DDCs and 34/68 DUCs (digital downconverters and digital upconverters)
- Signal drop/add/replace
- Frequency shifting and hopping
- Amplitude boost and attenuation
- PCI Express Gen. 1: x4 or x8

57624 BLOCK DIAGRAM

Click on a block for more information.

Block diagram 57624 shows half of the 58624. All resources are actually double of what is shown except for the PCIe-to-PCIe Switch.



THE COBALT ARCHITECTURE

The 57624 and 58824 consist of one or two 71624 XMC modules mounted on a VPX carrier board. The 57624 is a 6U board with one 71624 module while the 58624 is a 6U board with two XMC modules rather than one.

As IF relays, they accept two or four IF analog input channels, modify up to 34 or 68 signals, and then deliver them to two or four analog IF outputs. Any signal within each IF band can be independently enabled or disabled, and changed in both frequency and amplitude as it passes through the board.

EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. The GateFlow FPGA Design Kits include all of the factory-installed modules as document source code. Developers can integrate their own IP with the factory-installed functions or use the GateFlow kit to completely replace the IP with their own.

XILINX VIRTEX-6 FPGA

The SX315T Virtex-6 FPGA with 1344 DSP48E engines is well suited for the demanding signal processing tasks required by the 71620 adaptive relay. Because of the complexity and proprietary nature of these functions, the FPGA cannot be extended or modified by the user.

ADAPTIVE RELAY INPUT OVERVIEW

These models digitize two or four analog IF inputs using 200 MHz 16-bit A/D converters. The bandwidth of each IF signal can be up to 80 MHz, and may contain multiple signals, each centered at a different frequency. An array of 34 or 68 DDCs (digital down converters) can be independently programmed to translate any signal to baseband and then band limit the signal as required. DDC tuning frequency is programmable from 0 Hz to the A/D sample rate. Output bandwidth is programmable from around 20 kHz to 312 kHz for a sample rate of 200 MHz. Each DDC can independently source IF data from either of the two A/Ds.

Baseband I+Q DDC outputs are scaled in a programmable gain/attenuation block before being delivered across the PCIe system interface to target memory, typically associated with a system processor. Here, the signals can be analyzed, classified, demodulated, decrypted or decoded, depending on the application.

Samples from each A/D converter can also be delivered across PCIe to system memory so that the processor can access wideband IF data. By performing an FFT, the processor can identify signals and then tune the DDCs accordingly.

ADAPTIVE RELAY OUTPUT OVERVIEW

The output stage of these models consists of 34 or 68 DUCs (digital upconverters) and two or four 800 MHz 16-bit D/A converters. Each DUC accepts baseband I+Q signals from either the local DDCs or from system memory.

DUC inputs are scaled in programmable gain/attenuation blocks similar to those in the input stages. Each DUC is independently programmable for data source selection (DDC or memory), upconvert tuning frequency and bandwidth (interpolation).

The translated DUC outputs are directed to either of two or four summation blocks, each associated with one of the two or four D/A converters using a final interpolation factor of x4. After conversion, the IF analog outputs of each D/A can contain signals from any combination of the 34 or 68 DUCs.

A/D CONVERTERS

The front-end accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two or four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into one or two Virtex-6 FPGAs for the data capture and all of the remaining adaptive relay signal processing operations.

DIGITAL DOWNCONVERTERS

Each of the FPGA-based DDCs has an independent mixer and local oscillator with a 32-bit tuning frequency setting that ranges from DC to f_S, where f_S is the A/D sampling frequency, nominally 200 MHz. An IF input signal can be downconverted to a complex (I+Q) signal centered at 0 Hz by setting the DDC tuning frequency to its center frequency.

The DDC output bandwidth is determined by its decimation setting, which is programmable from 512 to 8192 in steps of 8. Each DDC can have a different decimation, thereby supporting up to 34 different signal bandwidths.

The fixed 80% decimating output filters deliver an output bandwidth equal to 0.8*fs/N, where N is the decimation setting and fs is the A/D sample rate. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_S/N.

D/A CONVERTERS

One or two Texas Instruments DAC5688 dual-channel D/As accept the summed upconverted data streams, one from each summation block, and operates in its non-translating dual, real baseband mode. Its built-in interpolation filter is typically set to x4 mode, boosting the summation output sample rate from a nominal 200 MHz to 800 MHz. This simplifies the output low pass reconstruction filtering requirements.

Two or four transformer-coupled analog IF outputs are delivered through one or two pairs of front panel SSMC connectors.

DIGITAL UPCONVERTERS

The interpolation filter increases the base-band input sample rate by an interpolation factor typically equal to the decimation factor of the corresponding DDC. This interpolation factor is programmable from 512 to 8192 in steps of 8. Using this strategy, the interpolation sample rate equals the A/D sample rate, nominally 200 MHz.

A complex digital mixer upconverts the interpolated baseband signal to the desired IF output center frequency. This frequency is determined by a local oscillator programmable with a 32-bit integer from DC to f_S, where f_S is the interpolator output frequency, nominally 200 MHz.

Each of the DUCs can have an independent interpolation factor and tuning frequency. However, all DUC outputs sharing a common summation block must have the same sample rate.

CLOCKING AND SYNCHRONIZATION

Two or four internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks.

In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

One or two front panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

PCI EXPRESS INTERFACE

These models include an industry-standard interface fully compliant with PCIe Gen. 1 x8 bus specifications. The interface automatically adjusts to accommodate fewer lanes, and includes dual DMA controllers for efficient transfers to and from the board.

INPUT GAIN BLOCKS

Each DDC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated. Each input gain block, which is a complex digital multiplier, accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately+48 dB to -48 dB.

RECEIVE DMA CONTROLLERS

Two or four output DMA engines deliver data across the PCIe interface into user-specified memory locations in PCIe target memory. DMA engine #1 can deliver either raw samples from A/D Ch 1 or channel-inter-leaved 24-bit I and Q baseband samples from the 34 DDCs. Data samples from each DDC can be independently enabled/disabled for output. DMA engine #2 can deliver raw samples from A/D Ch 2. This sequence repeats for the second XMC module of the 58624.

When a target memory buffer is filled, these models issue an interrupt to the system processor and then begins filling an alternate buffer. In this way, the processor is always informed when and where data is available for retrieval. Packet headers identify the DDC and show the number of subsequent data samples.

TRANSMIT DMA CONTROLLERS

Each of the FPGA-based 34 or 68 DUCs interpolates complex (I+Q) baseband signals and translates them to the desired IF output center frequency.

The data source for each DUC can be independently selected from its corresponding DDC output, or from PCIe target memory buffers fetched by the transmit DMA controller, where header information steers the memory data to the appropriate DUC channel.

Like the receive DMA controllers, once a data buffer is emptied, these models signal the processor with an interrupt and move to the next assigned buffer to continue fetching data.

OUTPUT GAIN BLOCKS

The complex baseband input for each DUC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated.

Each of the output gain blocks accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to -48 dB.

SUMMATION BLOCKS

Two or four summation blocks accept any combination of the upconverted DUC signals by setting an enable bit for each DUC's contribution. Each DUC output can be enabled for none, one or both of the summation blocks.

The summation blocks deliver only real output samples to the subsequent D/A converter stage.

READYFLOW

Mercury provides ReadyFlow® BSPs (Board Support Packages) for all Cobalt, Onyx, and Flexor products. Available for both Linux and Windows, these packages:

- Provide a path for quick start-up through application completion
- Allow programming at high, intermediate and low levels to meet various needs
- Are illustrated with numerous examples
- Include complete documentation and definitions of all functions
- Include library and example source code.

ReadyFlow BSPs contain C-language examples that can be used to demonstrate the capabilities of Cobalt, Onyx, and Flexor products. These programming examples will help you get an immediate start on writing your own application. They provide sample code that is known to work, giving you a means of verifying that your board set is operational.

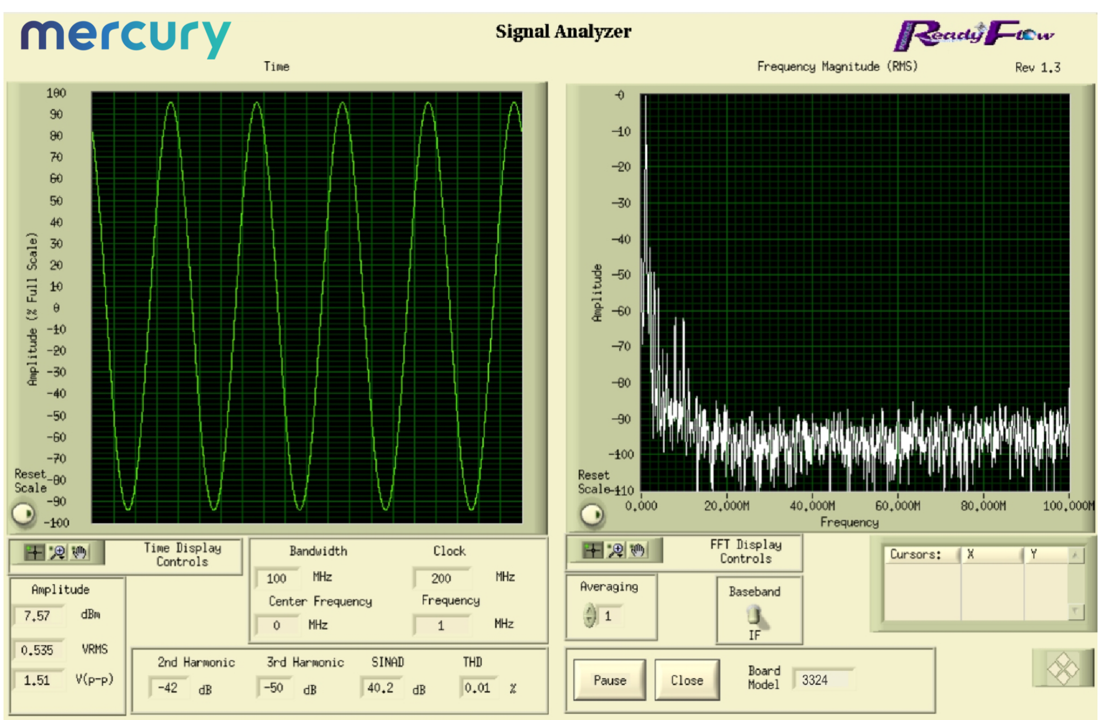
COMMAND LINE INTERFACE

The Command Line Interface provides access to pre-compiled executable examples that operate the hardware right out of the box, without the need to write any code. Board-specific hardware operating arguments can be entered in the command line to control parameters: number of channels to enable, sample clock frequency, data transfer size, reference clock frequency, reference clock source, etc.

The Command Line Interface can be used to call an example application from within a larger user application to control the hardware, and parameter arguments are passed to the application for execution. Functions that control data acquisition automatically save captured data to a pre-named host file or are routed to the Signal Analyzer example function for display.

SIGNAL ANALYZER

When used with the Command Line Interface, the Signal Analyzer allows users to immediately start acquiring and displaying A/D data. A full-featured analysis tool, the Signal Analyzer displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD, and SINAD. Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals.



GATEFLOW

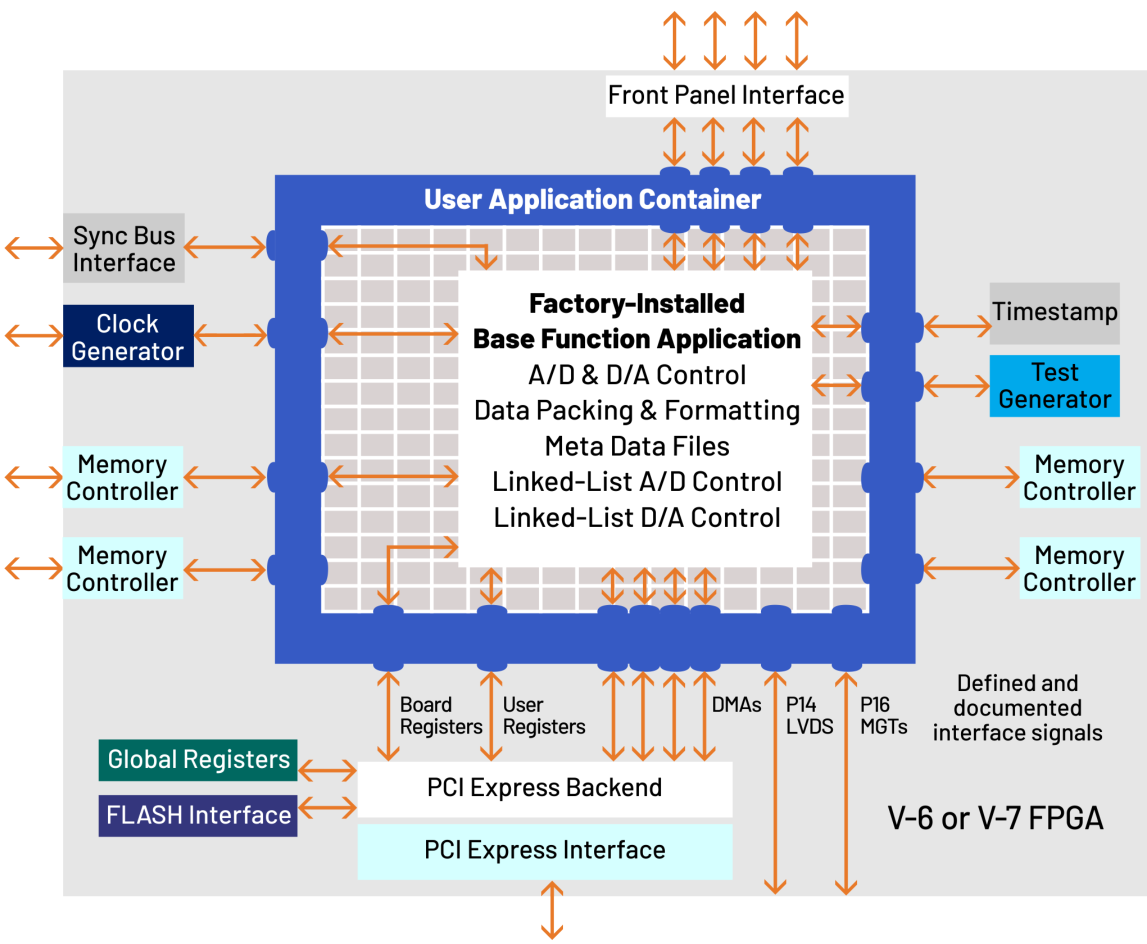
The GateFlow® FPGA Design Kit (FDK) allows the user to modify, replace and extend the standard installed functions in the FPGA to incorporate special modes of operation, new control structures, and specialized signal-processing algorithms.

The Cobalt (Virtex-6), Onyx (Virtex-7), and Flexor (Virtex-7) architectures configure the FPGA with standard factory-supplied interfaces including memory controllers, DMA engines, A/D and D/A interfaces, timing and synchronization structures, triggering and gating logic, time stamping and header tagging, data formatting engines, and the PCIe interface. These resources are connected to the User Application Container using well-defined ports that present easy-to-use data and control signals, effectively abstracting the lower-level details of the hardware.

The User Application Container

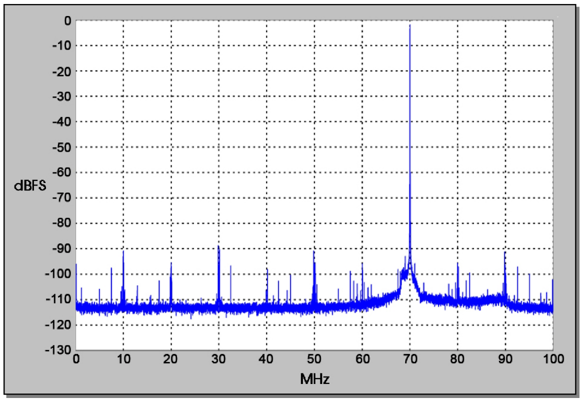
Shown below is the FPGA block diagram of a typical Cobalt, Onyx or Flexor module. The User Application Container holds a collection of different installed IP modules connected to the various interfaces through the standard ports surrounding the container. The specific IP modules for each product are described in further detail in the datasheet of that product.

The GateFlow FDK provides a complete Xilinx's ISE or Vivado project folder containing all the files necessary for the FPGA developer to recompile the entire project with or without any required changes. VHDL source code for each IP module provides excellent examples of how the IP modules work, how they might be modified, and how they might be replaced with custom IP to implement a specific function.



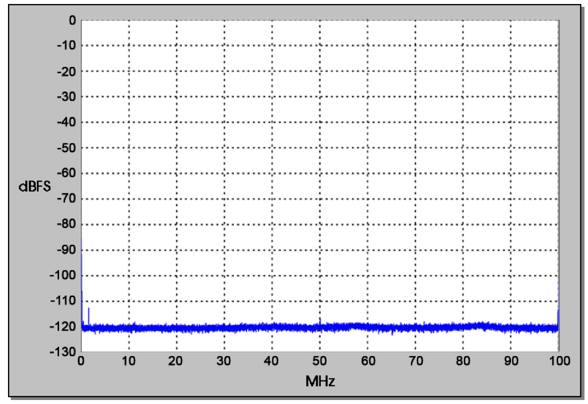
A/D PERFORMANCE

Spurious Free Dynamic Range



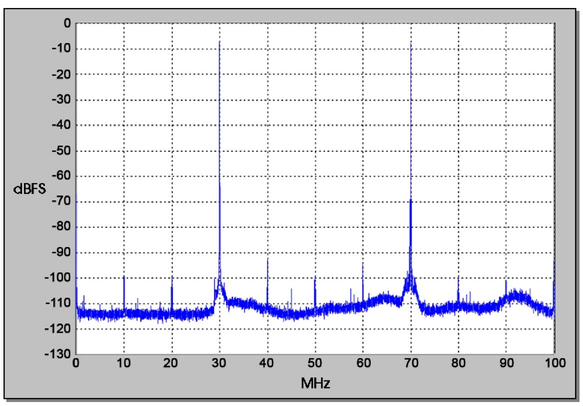
f_{in} = 70 MHz, f_s = 200 MHz, Internal Clock

Spurious Pick-up



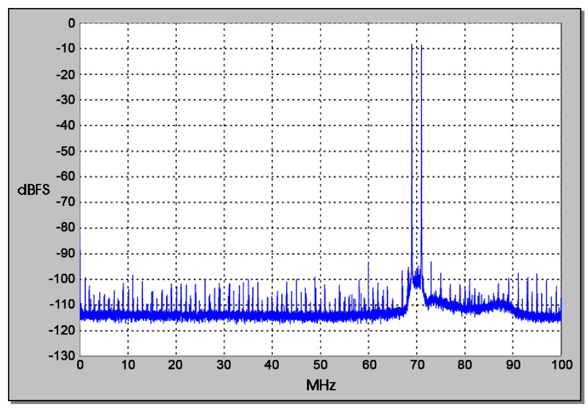
f_s = 200 MHz, Internal Clock

Two-Tone SFDR



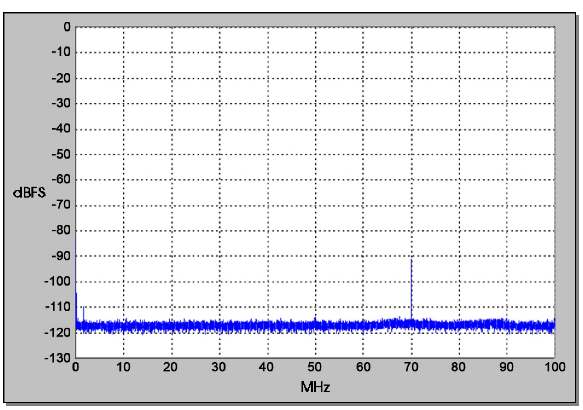
f_1 = 30 MHz, f_2 = 70 MHz, f_s = 200 MHz

Two-Tone SFDR



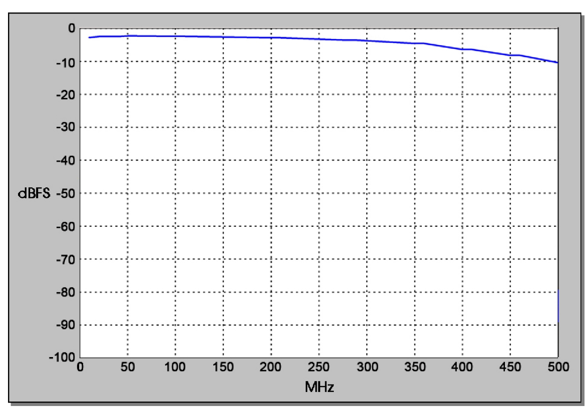
f_1 = 69 MHz, f_2 = 71 MHz, f_s = 200 MHz

Adjacent Channel Crosstalk



f_{in} Ch2 = 70 MHz, f_s = 200 MHz, Ch 1 shown

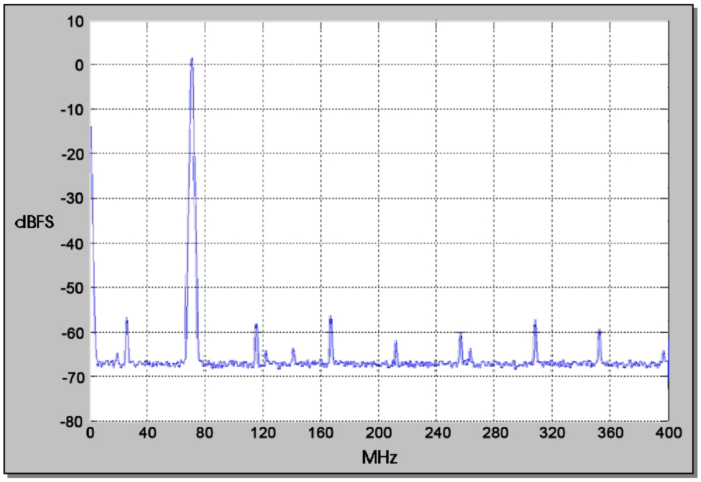
Input Frequency Response



f_s = 200 MHz, Internal Clock

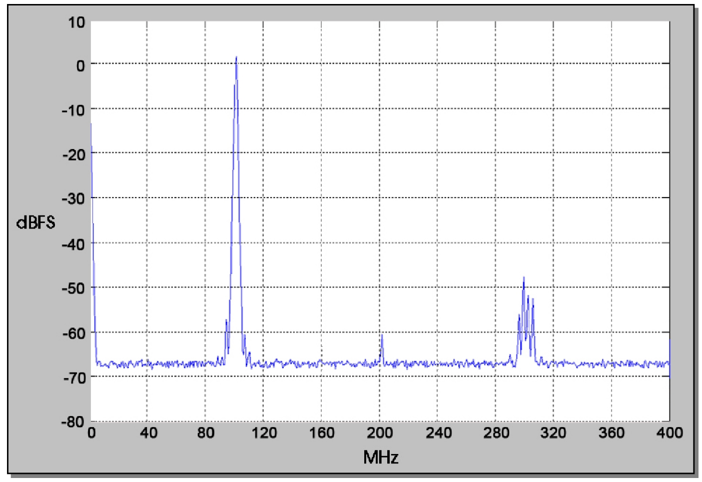
D/A PERFORMANCE

Spurious Free Dynamic Range



f_{out} = 70 MHz, f_s = 800 MHz, Interpolation = 4,
Internal Clock

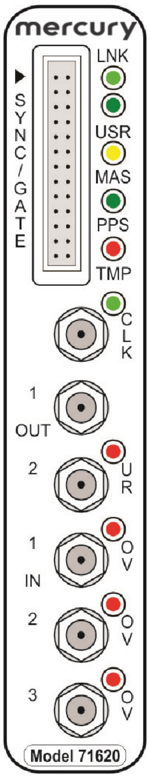
Spurious Free Dynamic Range



f_{out} = 100 MHz, f_s = 800 MHz, Interpolation = 4,
Internal Clock

FRONT PANEL CONNECTIONS

The XMC front panel includes six SSMC coaxial connectors and a 26-pin Sync Bus connector for input/output of timing and analog signals. The front panel also includes ten LEDs.



- **Sync Bus Connector:** The 26-pin Sync Bus front panel connector, labeled **SYNC/ GATE**, provides clock, sync, and gate input/output pins for the LVPECL Sync Bus.
- **Link LED:** The green **LNK** LED blinks when a valid link has been established over the PCIe interface.
- **User LED:** The green **USR** LED is for user applications.
- **Master LED:** The yellow **MAS** LED illuminates when the 71621 is the Sync Bus Master. When only a single 71621 is used, it must be a Master.
- **PPS LED:** The green **PPS** LED illuminates when a valid PPS signal is detected. The LED will blink at the rate of the PPS signal.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the PCB.
- **Clock LED:** The green **CLK** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.
- **Clock Input Connector:** One SSMC coaxial connector, labeled **CLK**, for input of an external sample clock.
- **Analog Output Connectors:** Two SSMC coaxial connectors, labeled **OUT 1** and **2**: one for each DAC5688 output.
- **D/A Underrun LED:** There is one red **UR** (underrun) LED for the D/A output. This LED illuminates when the DAC5688 FIFO is out of data.
- **Analog Input Connectors:** Three SSMC coaxial connectors, labeled **IN 1**, **IN 2**, and **IN 3**: one for each ADS5485 input channel.
- **A/D Overload LEDs:** There are three red **OV** (overload) LEDs: one for each A/D input. Each LED indicates either an analog input overload in the associated ADS5485, or an A/D FIFO overrun.

SPECIFICATIONS

57624: 2 A/Ds, 34 DDCs, 34 DUCs, 2 D/As; 58624: 4 A/Ds, 68 DDCs, 68 DUCs, 4 D/As

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Quantity: 2 or 4

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

Digital Downconverters

Quantity: 34 or 68

Decimation Range: 512 to 8192, in steps of 8

LO Tuning Freq. Resolution: 32 bits, 0 to f_s

LO SFDR: >100 dB

Phase Offset: 1 bit, 0 or 180 degrees

FIR Filter: 18-bit coefficients

Output: Complex, 16-bit I + 16-bit Q

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Input Gain Block

Quantity: 34 or 68

Data: Complex, 16-bit I + 16-bit Q

Gain Range: 16-bit Q8.8 format, approximately +/- 48 dB

Output Gain Blocks

Quantity: 34 or 68

Data: Complex, 16-bit I + 16-bit Q

Gain Range: 16-bit Q8.8 format, approximately +/- 48 dB

Digital Upconverters

Quantity: 34 or 68

Interpolation Range: 512 to 8192, insteps of 8

LO Tuning Freq. Resolution: 32 bits, 0 to f_s

LO SFDR: >120 dB

FIR Filter: 18-bit coefficients, 16-bit output

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters

Analog Output Channels: 2 or 4

Type: Texas Instruments DAC5688

Input Data Rate: 200 MHz max.

Output Signal: Real

Output Sampling Rate: 800 MHz max. with 4x interpolation

Resolution: 16 bits

Front Panel Analog Signal Outputs (2 or 4)

Output Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources (1 or 2)

On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer (1 or 2)

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)

Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accept 10 to 800 MHz sample clock or PLL system reference

Timing Bus

26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/ trigger and sync/PPS inputs

Field Programmable Gate Arrays (1 or 2)

Required: Xilinx Virtex-6 XC6VSX315T

PCI Express Interface

PCI Express Bus: Gen. 1 x4 or x8

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions:

- Depth: 171 mm (6.717 in.)
- Height: 100 mm (3.937 in.)

Weight: VPX Carrier: 110 grams (3.9 oz)

ORDERING INFORMATION

Model	Description
57624	Dual-Channel 34-Signal Adaptive IF Relay - 6U VPX
58624	Quad-Channel 68-Signal Adaptive IF Relay - 6U VPX

Options	Description
-064	XC6VSX315T FPGA (required)
-702	Air-cooled, Level 2
-763	Conduction-cooled, Level 3

Contact Mercury for compatible option combinations.

ACCESSORY PRODUCTS

Model	Description
2171	Cable Kit: SSMC to SMA

FORM FACTORS

Cobalt products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Cobalt Model 71624 XMC (Adaptive Relay, Virtex-6 FPGA) has the following variants:

Model	
52624	3U VPX board (single XMC)
57624	6U VPX board (single XMC)
58624	6U VPX board (dual XMC)
71624	XMC module
78624	PCIe board (single XMC)

DEVELOPMENT SYSTEMS

Mercury offers development systems for Cobalt products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Cobalt boards. Please contact Mercury to configure a system that matches your requirements.

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