

Flexor 5973 3U VPX Virtex-7 Processor and FMC Carrier

FMC carrier offers optical interface

- Incorporates the VITA 66.4 standard for half-size MT optical interconnect
- Provides 12 optical duplex lanes to the backplane
- Robust solution for high data rate demands
- VITA-57.1 FMC site offers access to a wide range of possible I/O



The Flexor™ 5973 is a high-performance 3U OpenVPX board based on the Xilinx Virtex-7 FPGA. As a stand-alone processor board, it provides an ideal development and deployment platform for demanding signal-processing applications.

The 5973 includes a VITA-57.1 FMC site providing access to a wide range of I/O options. When combined with any of Mercury's analog interface FMCs, it becomes a complete multichannel data conversion and processing subsystem suitable for connection to IF, HF or RF ports of a communications or radar system.

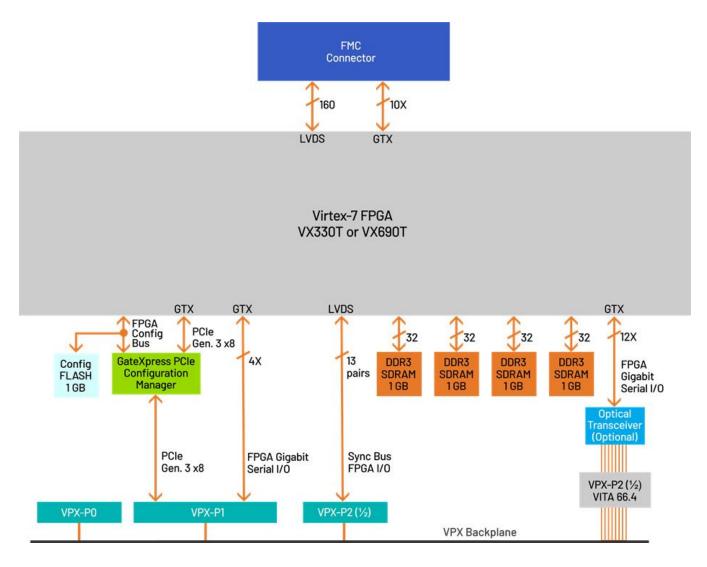
When used with Mercury's gigabit serial copper or optical interface FMCs, the 5973 becomes a high speed data streaming and processing interface. Its built-in data capture and playback features and Gen. 3 x8 PCIe interface make it a turnkey solution.

FEATURES

- VITA-57.1 FMC site offers access to a wide range of possible I/O
- Supports Xilinx® Virtex®-7 VXT FPGA
- GateXpress[®] supports dynamic FPGA reconfiguration across PCle
- 4 GB of DDR3 SDRAM
- PCI Express (Gen. 1, 2 and 3) interface up to x8
- Optional optical Interface for backplane gigabit serial interboard communication
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)



5973 BLOCK DIAGRAM





BOARD ARCHITECTURE

Based on the proven design of the Mercury Onyx family of Virtex-7 products, the 5973 retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the main board and the FMC, enabling factory-installed functions That Include data multiplexing, channel selection, data packing, gating, triggering and memory control.

The architecture organizes the FPGA as a container for dataprocessing applications where each function exists as an intellectual property (IP) module.

When integrated with a Mercury FMC, the 5973 is delivered with factory-installed applications ideally matched to the board's analog or digital interfaces. These can include A/D acquisition and D/A waveform playback engines for simplifying data capture and playback.

Data tagging and metadata packet generation, in conjunction with powerful linked list DMA engines, provide a streamlined interface for moving data on and off the board and identifying data packets with channel, timing and sample count information.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCle interface complete the factory-installed functions and enable the 5973 and its installed FMC to operate as a complete turnkey solution without the need to develop any FPGA IP.

EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. The GateFlow FPGA Design Kits include all of the factory-installed modules as document source code. Developers can integrate their own IP with the factory-installed functions or use the GateFlow kit to completely replace the IP with their own.

XILINX VIRTEX-7 FPGA

The Xilinx Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

GATEXPRESS FOR FPGA CONFIGURATION

The Onyx architecture includes GateXpress®, a sophisticated FPGA-PCle configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCle target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCle discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCle interface. At power up the user can choose which image will load based on a hardware switch setting. Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image:

- The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.
- The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.
- The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCle configuration space allowing dynamic FPGA reconfiguration without a host computer reset to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.



FRONT PANEL CONNECTIONS

The 5973 3U VPX carrier front panel houses the front panel of the FMC module installed on the carrier. The VPX carrier front panel includes three LED indicators below the FMC panel.

Standard Option 729 mercury mercury + Model 5973 + Model 5973 **FMC FMC** front front panel panel A G LNK O LNK O TMP ● TMP USR @ USR O 4 HP 5 HP

JTAG Connector:

The VPX carrier front panel provides a 12-pin JTAG connector to download programs and to perform boundaryscan tests on 5973 devices.

- Link LED: The green LNK LED illuminates when a valid PCIe link has been established over the VPX P1 interface.
- Over Temperature
 LED: The red TEMP
 LED illuminates when
 an over-temperature
 or over-voltage
 condition is indicated
 by the
 temperature/voltage
 sensors on the Model
 5973.
- User LED: The yellow USR LED is available for user applications.

Note: If your 5973 is ordered with Option 763 for mounting in a conduction-cooled VPX chassis, it would have a conduction-cooled VPX Carrier Front Panel.

SPECIFICATIONS

I/O Module Interface

VITA-57.1 FMC site

Field Programmable Gate Array

Standard: Xilinx Virtex-7 XC7VX330T-2
 Optional: Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O

Parallel: 13 pairs of LVDS connections between the FPGA and

the VPX P2 connector for custom I/O

Serial: 4X gigabit links between the FPGA and the VPX P1 $\,$

connector to support serial protocols.

Optical: VITA-66.4, 12X duplex lanes Memory

Type: DDR3 SDRAM

Size: Four banks, 1 GB each Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air-cooled)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

Operating Temp: -20° to 65° C

Storage Temp: -40° to 100° C

Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

Operating Temp: -40° to 70° C

Storage Temp: -50° to 100° C

Relative Humidity: 0 to 95%, noncondensing

Physical

Dimensions: 3U VPX

Depth: 100 mm (3.937 in)Height: 170.6 mm (6.717 in)



FLEXORSET MODELS

This chart shows all available FlexorSets. Click on model numbers for more information.

Form Factor	Software/FPGA Tools	Carrier Model	FMC Model	FlexorSet Model	Description
3U VPX	Virtex-7 ReadyFlow BSP GateFlow FDK Vivado	5973	3312	5973-312	4-Channel 250 MHz A/D & 2-Channel 800 MHz D/A
				5973-313	4-Channel 250 MHz A/D & 2-Channel 800 MHz D/A with 4 multiband DDCs & interpolation filters
			3316	5973-316	8-Channel 250 MHz 16-bit A/D
				5973-317	8-Channel 250 MHz 16-bit A/D with 8 multiband DDCs
			3320	5973-320	2-Channel 3 GHz A/D & 2-Channel 2.8 GHz D/A
			3324	5973-324	4-Channel 500 MHz A/D & 4-Channel 2 GHz D/A
	KintexUltraScale Navigator BSP Navigator FDK Vivado	5983*	3312	5983-313*	4-Channel 250 MHz A/D & 2-Channel 800 MHz D/A with 4 multiband DDCs & interpolation filters
			3316	5983-317*	8-Channel 250 MHz 16-bit A/D with 8 multiband DDCs
			3320	5983-320*	2-Channel 3 GHz A/D & 2-Channel 2.8 GHz D/A
			3324	5983-324*	4-Channel 500 MHz A/D & 4-Channel 2 GHz D/A
PCle	Virtex-7	7070	3312	7070-312	4-Channel 250 MHz A/D & 2-Channel 800 MHz D/A
	ReadyFlow BSP GateFlow FDK Vivado			7070-313	4-Channel 250 MHz A/D & 2-Channel 800 MHz D/A with 4 multiband DDCs & interpolation filters
			3316	7070-316	8-Channel 250 MHz 16-bit A/D
				7070-317	8-Channel 250 MHz 16-bit A/D with 8 multiband DDCs
			3320	7070-320	2-Channel 3 GHz A/D & 2-Channel 2.8 GHz D/A
			3324	7070-324	4-Channel 500 MHz A/D & 4-Channel 2 GHz D/A

 $^{^*}$ Consult with Mercury about the availability of a 5983A version of this product. For differences, see below.

Model 5983	Model 5983A
Flash Memory - 1 Gbit of FLASH Memory	Flash Memory -2 Gbit of BPI FLASH Memory
Optical I/O (Option 110) - VITA 66.4 - Up to 12 duplex optical lanes are available on a VITA 66.4 connector. With the installation of a serial protocol, the VITA 66.4 interface enables a high-bandwidth connection between 5983s mounted in the same chassis or over extended distances.	Optical I/O (Option 110) - VITA 67.3D - Provides 12 duplex lanes @ 10 Gb/sec through the lower half of VPX P2 (VPX P2B). With the installation of a serial protocol, the VITA 67.3D interface enables gigabit communications between boards and chassis, independent of the PCIe interface. Consult with Mercury before ordering Option 110 (optical).
	Custom Analog I/O (Option 113) - VITA 67.3 - VITA 67.3 provides 10 coax connections through the lower half of VPX P2.



ORDERING INFORMATION

Model	Description	
5973	3U OpenVPX Virtex-7 Processor and FMC Carrier	

Options:							
-073	XC7VX330T-2 FPGA						
-076	XC7VX690T-2 FPGA						
-702	Air-cooled, Level 2						
-763	Conduction-cooled, Level 3						

Contact Mercury for compatible option combinations and complete specifications of rugged and conduction-cooled versions. Options may change, so be sure to contact Mercury for the latest information.

DEVELOPMENT SYSTEMS

Mercury offers development systems for Flexor products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Flexor boards. Please contact Mercury to configure a system that matches your requirements.

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