Jade 57865/58865

2 or 4-channel 200 MHz 16-bit A/D channelizer, 762 or 1524 narrowband DDCs, 4 or 8 wideband DDCs 6U VPX boards with Kintex UltraScale FPGA

Complete radar and software radio interface solution

- Radar and software radio receiver
- Communications receiver
- Analog signal interface for data recording
- Wideband data acquisition
- Remote monitoring
- Sensor interfaces

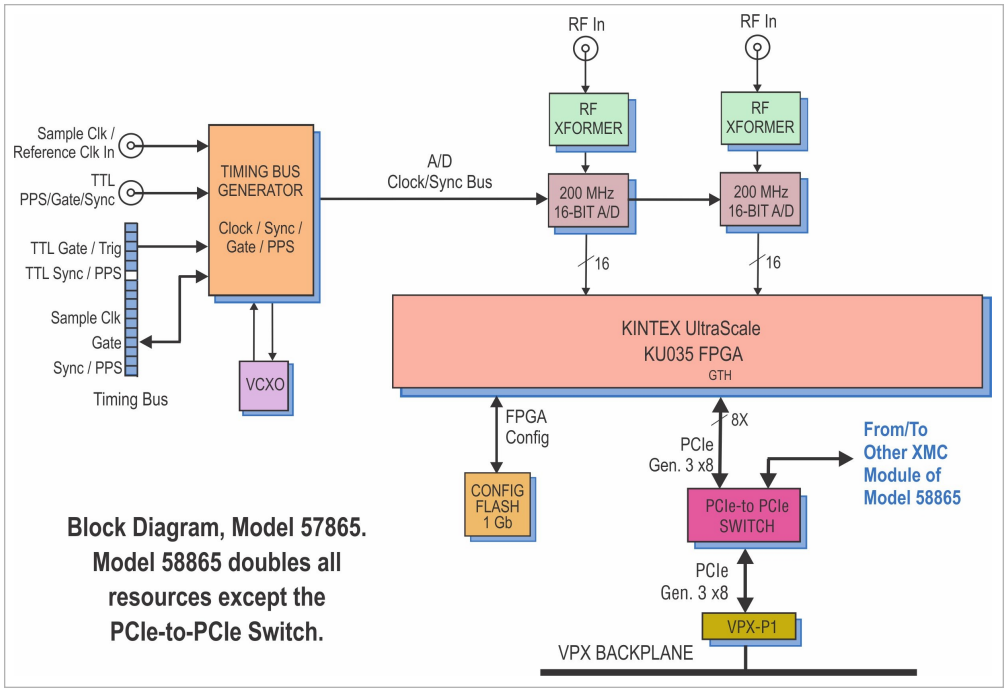
Jade® 57865 and 58865 consist of one or two 71865 XMC modules mounted on a 6U VPX carrier board. The 57865 is equipped with one 71865 while the 78865 is equipped with two XMC modules rather than one.

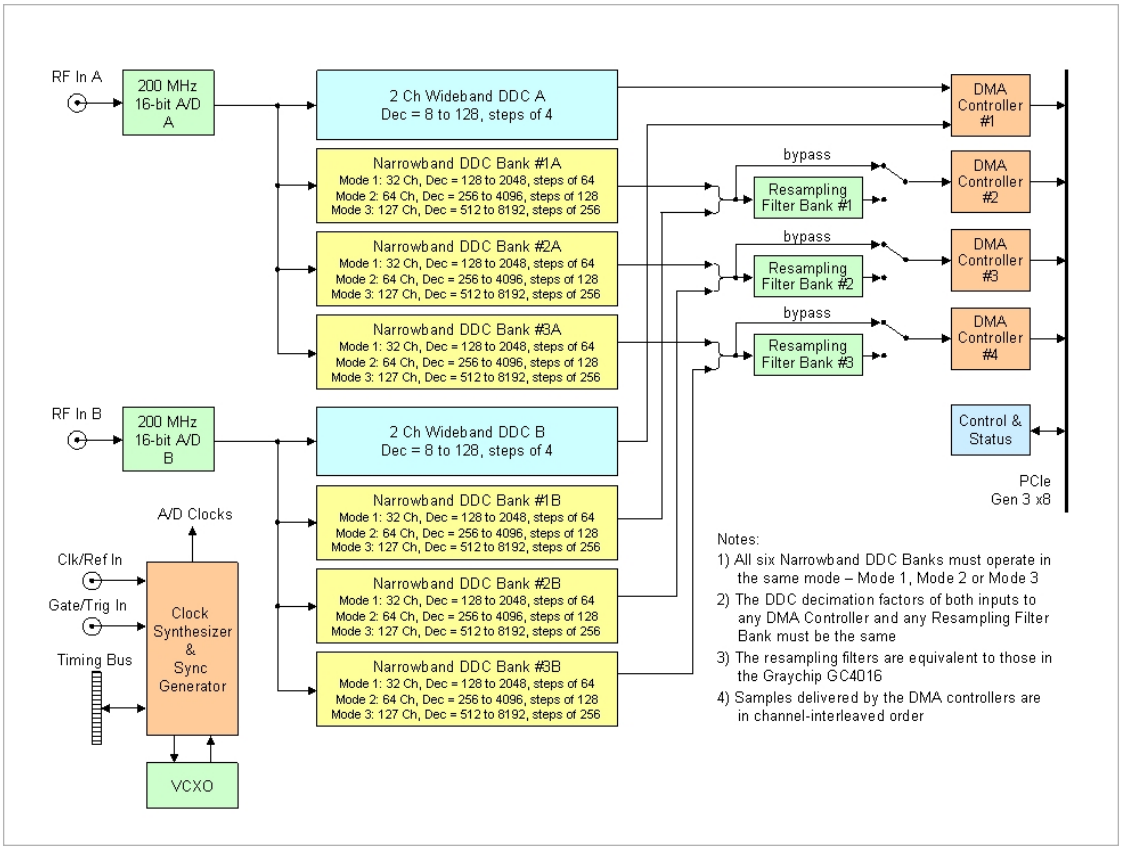
They include two or four A/Ds, complete multiboard clock and sync section, eight or 16 banks of channelizer-based DDCs and resampling filters.

FEATURES

- Complete software radio receiver solution for extremely high-channel-count applications
- Xilinx® Kintex® UltraScale™ KU035 FPGA
- Two or four 200 MHz 16-bit A/Ds
- Four or eight wideband DDCs (digital downconverters)
- Up to 762 or 1524 narrowband DDCs
- Sample clock generation and synchronization to an external system reference
- Ruggedized and conduction-cooled versions
- Navigator Design Suite for software and custom IP development

57865 BLOCK DIAGRAM





THE JADE ARCHITECTURE

Evolved from the proven designs of the Mercury Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions in these models include two or four A/D acquisition IP modules for simplifying data capture and transfer.

Each acquisition IP module contains a powerful, programmable DDC IP core and a controller for all data clocking, triggering, and synchronization functions. From each of the acquisition modules, A/D sample data flows into identical IP modules consisting of banks of wideband and narrowband DDCs. Finally, data is delivered to four or eight DMA controllers and then to the PCIe x8 interface.

These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

XILINX KINTEX ULTRASCALE FPGAS

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs: KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

A/D CONVERTERS

The board's analog interface accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two or four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Kintex UltraScale FPGAs for signal-processing or routing to other board resources.

A/D ACQUISITION IP MODULES

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data.

Each IP module has an associated DMA engine for easily moving DDC data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC RESOURCES

Samples from the two A/D converters flow into two identical blocks, each containing one bank of two wideband DDCs and three banks of narrowband DDCs, as shown in the block diagram below.

Wideband DDCs

The four wideband DDCs can be set for decimation values between 8 and 128 in steps of 4, providing usable output bandwidths from 1.25 MHz to 20 MHz for a sample rate, f_S, of 200 MHz. Because all four wideband DDCs within the 71865 feed the same DMA controller #1, all wideband DDCs must use the same decimation factor.

Each DDC delivers an output stream consisting of 16-bit I + 16-bit Q complex samples at a rate of f_S/N. Four samples, one from each of the wideband DDCs, are interleaved in the output stream. All four wideband DDCs can be independently tuned across the range from 0 Hz to f_S with 32 bits of resolution.

Narrowband DDCs

Each of the six narrowband DDC banks can be configured to operate in three different modes, where each mode provides a different quantity of DDC channels and range of decimations.

These modes are summarized in the following table:

Mode	Channels	Dec Range	Steps
1	32	128 - 2048	64
2	64	256 - 4096	128
3	127	512 - 8192	256

All six narrowband DDC banks must operate in the same mode.

The 80% default filters deliver an output bandwidth of $0.8*f_S/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers an output stream at a rate of f_S/N, and is programmable for either 16-bit I + 16-bit Q, or 24-bit I + 24-bit Q complex samples.

Because each pair of narrowband DDC banks feed a common DMA controller, the decimation setting for each DDC must be the same. Nevertheless, each pair can have a different decimation setting from the other pairs.

RESAMPLING FILTERS

Three multiplexers allow outputs from each of the three narrowband DDC pairs to feed the associated DMA controller or feed the input of a resampling filter.

Each of the three resampling filters is an FIR low-pass filter that accepts DDC input samples at one sample rate and delivers output samples at another rate. Resampling filters are often used for better symbol recovery of signals using digital modulation schemes. The output rate is usually higher to create oversampling at a multiple of 2x, 4x, 8x, or 16x the symbol rate.

The resampling filter combines the operations of an FIR interpolation filter followed by a decimator. The overall resampling ratio is equal to the interpolation factor divided by the decimation factor, both of which are programmable parameters.

Note that each of the three resampling filters can be programmed independently. Some limitations on the DDC output data rates and subsequent resampling ratios may be imposed because of maximum PCIe transfer rates.

CLOCKING AND SYNCHRONIZATION

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front-panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

PCI EXPRESS INTERFACE

These models include industry-standard interfaces fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interfaces include multiple DMA controllers for efficient transfers to and from the boards.

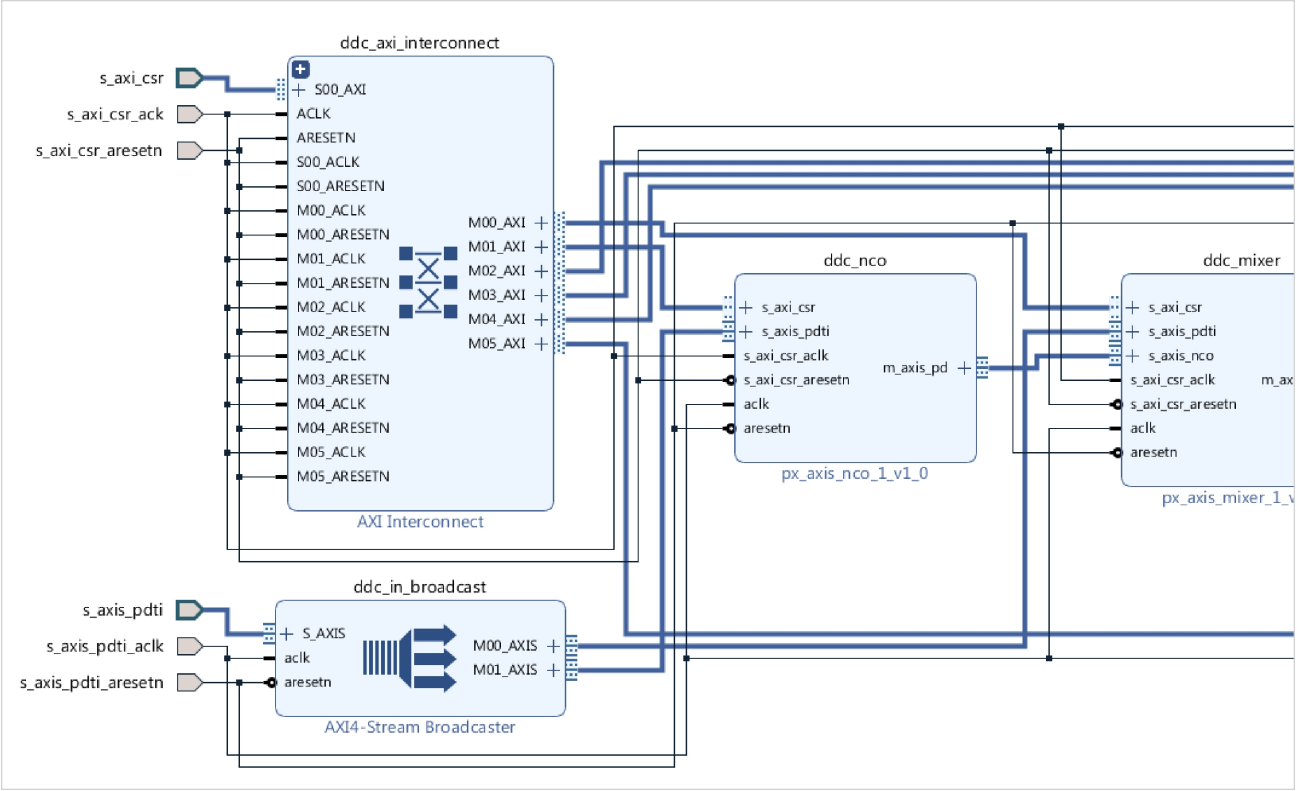
NAVIGATOR DESIGN SUITE

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into the factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

The **Navigator FPGA Design Kit (FDK)** for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Jade product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Jade design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations.

Navigator FDK includes an IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.

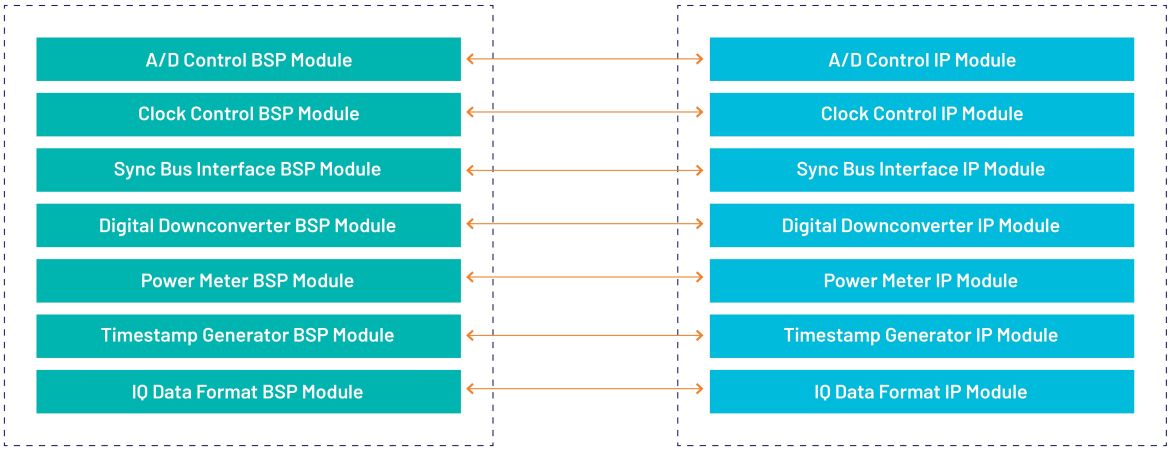
The **Navigator Board Support Package (BSP)** provides software support for Jade boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA. The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.



Navigator IP FPGA Design viewed in IP Integrator

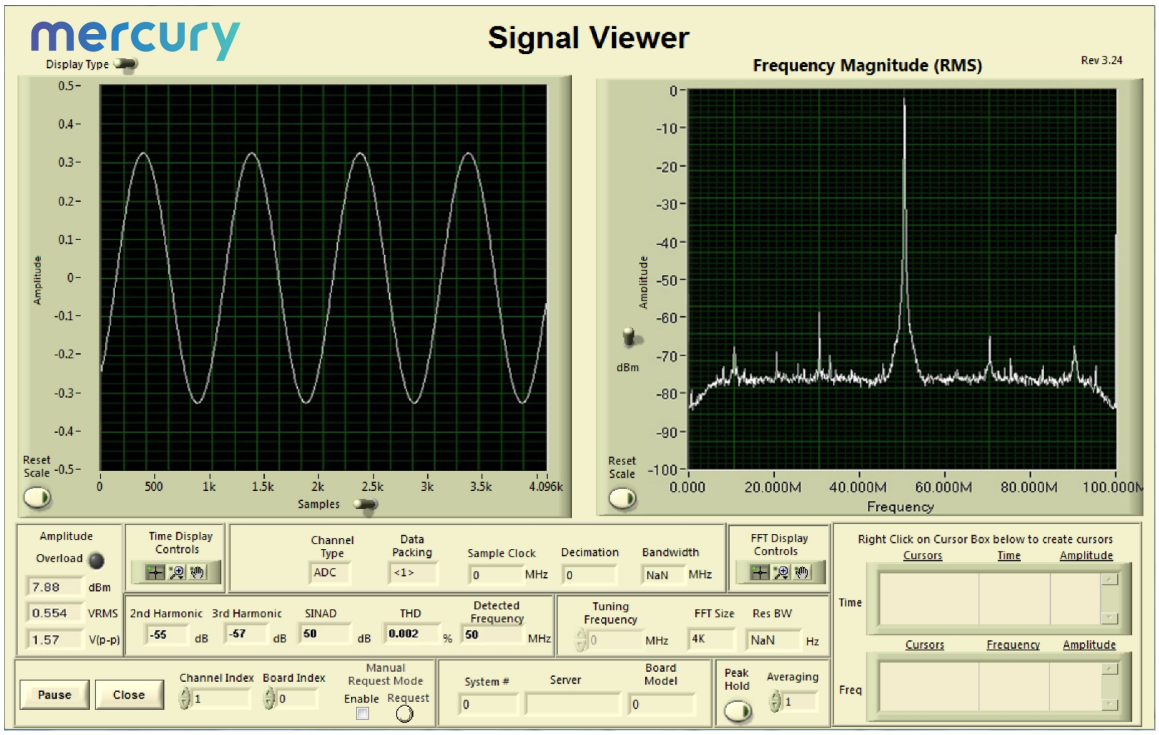
NAVIGATOR BOARD SUPPORT PACKAGE

NAVIGATOR FPGA DESIGN KIT



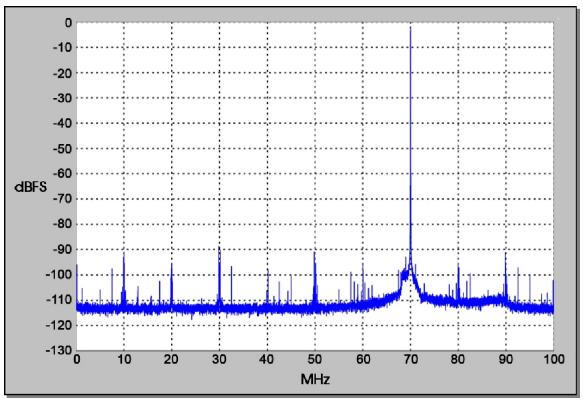
Because all Jade boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the **Signal Viewer**, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Jade board and Navigator BSP and start viewing analog signals immediately.



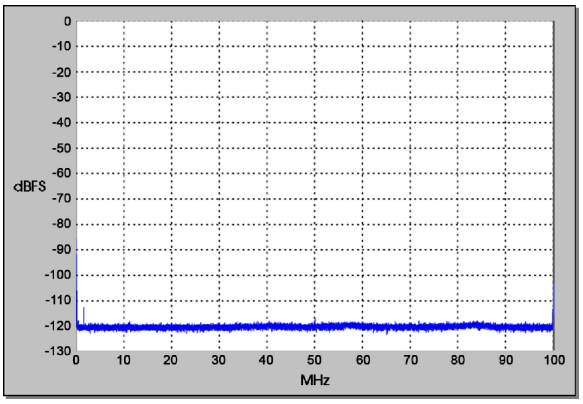
A/D PERFORMANCE

Spurious Free Dynamic Range



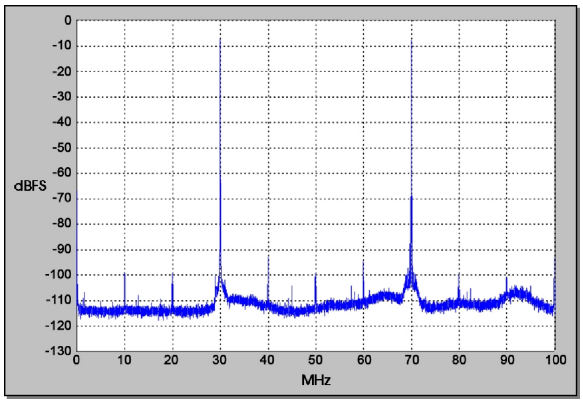
f_{in} = 70 MHz, f_s = 200 MHz, Internal Clock

Spurious Pick-up



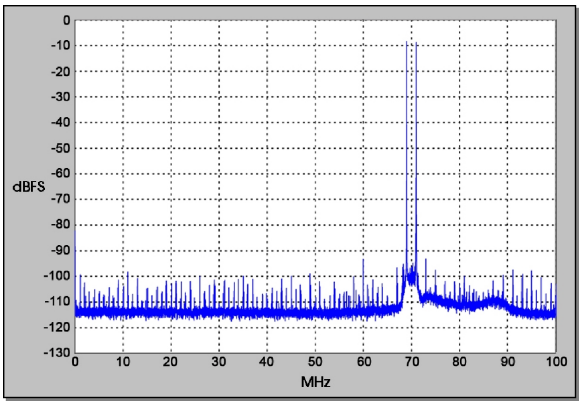
f_s = 200 MHz, Internal Clock

Two-Tone SFDR



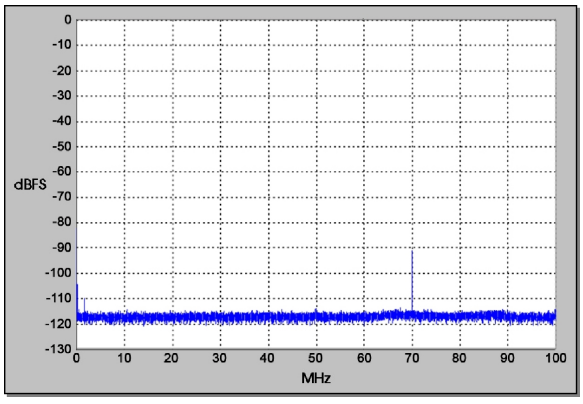
f_1 = 30 MHz, f_2 = 70 MHz, f_s = 200 MHz

Two-Tone SFDR



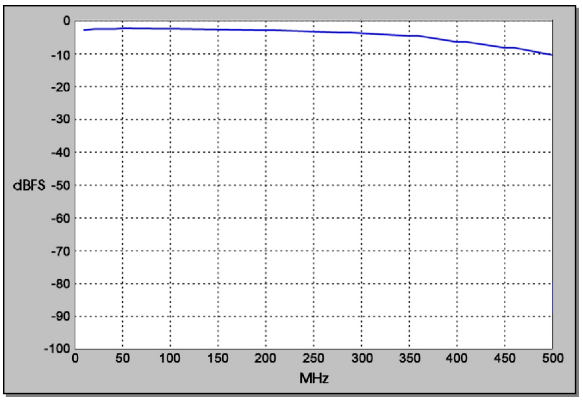
f_1 = 69 MHz, f_2 = 71 MHz, f_s = 200 MHz

Adjacent Channel Crosstalk



f_{in} Ch2 = 70 MHz, f_s = 200 MHz, Ch 1 shown

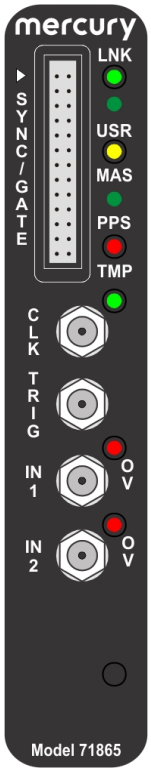
Input Frequency Response



f_s = 200 MHz, Internal Clock

FRONT PANEL CONNECTIONS

The front panel includes four SSMC coaxial connectors for clock, trigger, and analog input signals, and a 26-pin Sync Bus input/output connector. The front panel also includes eight LED indicators.



- **Sync Bus Connector:** The 26-pin µSync front panel connector, labeled **SYNC/GATE**, provides clock, sync, and gate input/output pins for the Low-Voltage Positive Emitter-Coupled Logic (LVPECL) Sync Bus.
- **Link LED:** The green **LNK** LED indicates the link speed when a valid link has been established over the PCIe interface, as follows: Gen 1 - LED blinks slowly (less than once per second); Gen 2 - LED blinks about once per second; Gen 3 - LED will be constantly on.
- **User LED:** The green **USR** LED is for user applications.
- **Master LED:** The yellow **MAS** LED illuminates when this 71865 is the Sync Bus Master. When only a single 71865 is used, it must be a Master.
- **PPS LED:** The green **PPS** LED illuminates when a valid PPS signal is detected. The LED will blink at the rate of the PPS signal.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the 71865 PCB.
- **Clock LED:** The green **CLK** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.
- **Clock Input Connector:** One SSMC coaxial connector, labeled **CLK**, for input of an external sample clock.
- **Trigger Input Connector:** One SSMC coaxial connector, labeled **TRIG**, for input of an external trigger.
- **Analog Input Connectors:** Two SSMC coaxial connectors, labeled **IN 1** and **IN 2**: one for each ADS5485 A/D converter.
- **DAC Underrun LED:** One red underrun **UR** LED for the D/A output. This LED illuminates when the DAC5688 FIFO is out of data.
- **ADC Overload LEDs:** There are two red **OV** (overload) LEDs: one for each A/D input. Each LED indicates either an overload in the associated ADS5485 or an ADC FIFO overrun.

SPECIFICATIONS

57865: 2 A/Ds; 58865: 4 A/Ds

Front Panel Analog Signal Inputs (2 or 4)

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type:
Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters (2 or 4)

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 GHz

Resolution: 16 bits

Wideband Digital Downconverters (4 or 8)

Decimation Range: 8 to 128 in steps of 4, common to all four DDCs

LO Tuning Freq. Resolution: 32 bits, 0 to f_s

LO SFDR: >120 dB

Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: 24-bit coefficients, 24-bit output

FIR Filter Performance: 80% bandwidth <0.3 dB passband ripple, >100 dB stopband attenuation

Narrowband Digital Downconverters

Quantity: Six or 12 banks

DDC Bank Modes:

Mode 1: 32 DDCs, Dec = 128 to 2048, in steps of 64

Mode 2: 64 DDCs, Dec = 256 to 4096, steps of 128

Mode 3: 127 DDCs, Dec = 512 to 8192, steps of 256

LO Tuning Freq. Resolution: 32 bits, 0 to f_s, with independent tuning for each channel

LO SFDR: >120 dB

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources (1 or 2)

On-board clock synthesizer

Clock Synthesizer (1 or 2)

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 3, 4, 6, 8, or 16 for the A/D clock

External Clock (1 or 2)

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2)

26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input (1 or 2)

Type: Front panel female SSMC connector, LVTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)

Standard: Xilinx Kintex UltraScale XCKU035-2

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: VPX board

- Depth: 233.35 mm (9.187 in)
- Height: 170.60 mm (6.717 in)

Weight: Approximately 14 oz (400 grams)

ORDERING INFORMATION

Model	Description
57865	2-channel 200 MHz A/D with 4 WB DDCs, 762 NB DDCs, Kintex UltraScale FPGA - 6U VPX
58865	4-channel 200 MHz A/D with DDCs and Kintex UltraScale FPGAs - 6U VPX

Options:	
-702	Air-cooled, Level 2
-763	Conduction-cooled, Level 3

Contact Mercury for compatible option combinations and complete specifications of rugged and conduction-cooled versions. Options may change, so be sure to contact Mercury for the latest information.

ACCESSORY PRODUCTS

Model	Description
2171	Cable Kit: SSMC to SMA

DEVELOPMENT SYSTEMS

Mercury offers development systems for Jade products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Jade boards. Please contact Mercury to configure a system that matches your requirements.

FORM FACTORS

Jade products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Jade Model 71865 XMC (4-Channel 200 MHz A/D with 766 DDCs, Kintex UltraScale FPGA) has the following variants:

Model	
52865	3U VPX board (single XMC)
57865	6U VPX board (single XMC)
58865	6U VPX board (dual XMC)
71865	XMC module
78865	PCIe board (single XMC)

LIFETIME SUPPORT FOR JADE PRODUCTS

Mercury offers worldwide customers shorter development time, reliable, rugged solutions for a variety of environments, reduced costs, and mature software development tools. We offer free lifetime support from our engineering staff, which customers can depend on through phone and email, as well as software updates. Take advantage of our 40 years of experience in delivering high-performance radar, communications, SIGINT, EW, and data acquisition MIL-Aero solutions worldwide.

Corporate Headquarters
50 Minuteman Road
Andover, MA 01810 USA
+1 978.967.1401 tel
+1 866.627.6951 tel
+1 978.256.3599 fax

International Headquarters
Mercury International
Avenue Eugène-Lance, 38
PO Box 584
CH-1212 Grand-Lancy 1
Geneva, Switzerland
+41 22 884 5100 tel

Learn more

Visit: mrcy.com/go/MP57865

For technical details, contact:
mrcy.com/go/CF57865

MADE IN USA