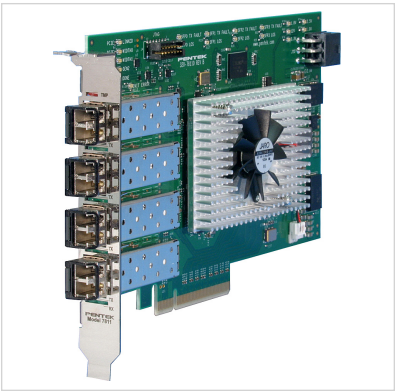
Cobalt 7811

Quad serial FPDP interface PCIe board with Virtex-6 FPGA

Complete serial FPDP solution

- Fully compliant with VITA 17.1 specification
- Fibre optic or copper serial interfaces
- PCI Express interface up to x8
- Virtex-6 FPGAs: LX130T, LX240T, or SX315T
- Extendable IP design



The 7811 is a multichannel, gigabit serial interface, ideal for interfacing to Serial FPDP data converter boards or as a chassis-to-chassis data link. The 7811 is fully compatible with the VITA 17.1 Serial FPDP specification.

Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 7811 serves as a flexible platform for developing and deploying custom FPGA processing IP.

THE COBALT ARCHITECTURE

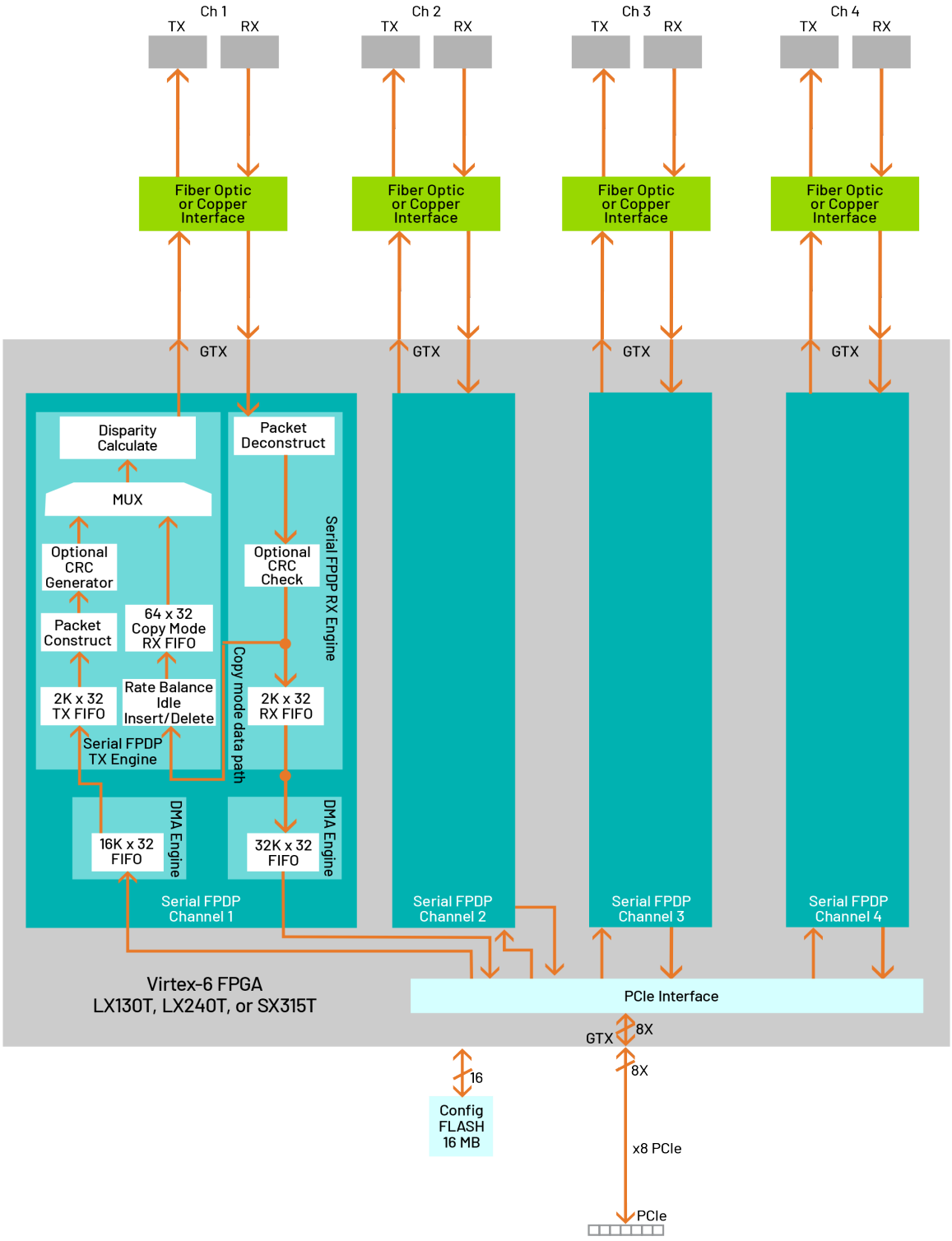
The Cobalt® Architecture features a Xilinx Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable the 7811 to operate as a complete turnkey solution without the need to develop any FPGA IP.

EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. The GateFlow FPGA Design Kits include all of the factory-installed modules as document source code. Developers can integrate their own IP with the factory-installed functions or use the GateFlow kit to completely replace the IP with their own.

7811 BLOCK DIAGRAM



XILINX VIRTEX-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

PCI EXPRESS INTERFACE

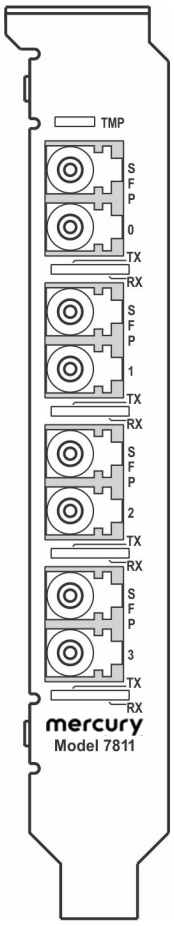
The 7811 includes an industry-standard interface fully compliant with PCI Express bus specifications. Supporting PCIe links up to x8, the interface includes eight DMA controllers. Each of the four Serial FPDP channels includes dedicated DMA engines for transmit and receive for efficient transfers to and from the board.

SERIAL FPDP INTERFACE

The 7811 is fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5,3.125, and 4.25 Gbaud link rates and the option for multimode and single-mode optical interfaces or copper interfaces, the board can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop modes.

FRONT PANEL CONNECTIONS

The 7811 PCIe front panel provides four duplex input/output connectors. The front panel also includes nine LEDs.



- **SFPDP I/O Connectors:** Four duplex Serial FPDP (SFPDP) fiber-optic transceivers, labeled **SFP 0** and **SFP 3** (Small Form-factor Pluggable) for SFPDP Ports 0 to 3 respectively, provide one input and one output connection.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by the temperature/voltage sensors on the 7811 PCB.
- **Transmit LEDs:** The four green LEDs labeled **TX** indicate a transmit in progress on the respective SFP channel's output.
- **Receive LEDs:** The four yellow LEDs labeled **RX** indicate a receive in progress on the respective SFP channel's input.

SPECIFICATIONS

Front Panel Serial FPDP Inputs/Outputs

Number of Connectors: 4

Fiber Optic Connector Type: LC

Laser: 850 nm (standard, other options available)

Copper Connector Type: SFP+

Fiber Optic or Copper Link Rates: 1.0625, 2.125, 2.5, 3.125 or 4.25 Gbaud (copper rate depends on cable length)

Fiber Optic or Copper Data Transfer Rates: 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port

Field Programmable Gate Array

- Standard: Xilinx Virtex-6 XC6VLX130T
- Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

PCI Express Interface

PCI Express Bus: Gen. 1 x4 or x8

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: Half-length PCIe card, 4.38 in. x 7.13 in.

- Depth: 181.0 mm (7.13 in.)
- Height: 111 mm (4.38 in.)

ORDERING INFORMATION

Model	Description
7811	Quad Serial FPDP Interface with Virtex-6 FPGA - PCIe

Options	Description
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-280	Copper serial interfaces
-281	Multimode optical serial interfaces
-702	Air-cooled, Level 2

Contact Mercury for compatible option combinations.

FORM FACTORS

Cobalt products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Cobalt Model 71611 XMC (Quad Serial FPDP Interface with Virtex-6 FPGA) has the following variants:

Model	
52611	3U VPX board (single XMC)
57611	6U VPX board (single XMC)
58611	6U VPX board (dual XMC)
71611	XMC module
78611	PCIe board (single XMC)
7811	PCIe board (single XMC)

DEVELOPMENT SYSTEMS

Mercury offers development systems for Cobalt products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Cobalt boards. Please contact Mercury to configure a system that matches your requirements.

Corporate Headquarters
50 Minuteman Road
Andover, MA 01810 USA
+1 978.967.1401 tel
+1 866.627.6951 tel
+1 978.256.3599 fax

International Headquarters
Mercury International
Avenue Eugène-Lance, 38
PO Box 584
CH-1212 Grand-Lancy 1
Geneva, Switzerland
+41 22 884 5100 tel

Learn more

Visit: mrcy.com/go/MP7811

For technical details, contact:
mrcy.com/go/CF7811

SERIAL FPDP VITA 17.1 COMPLIANCE

Mercury's Serial FPDP products fully comply with the VITA 17.1 specification as follows:

1. What Link Rate does the interface support?

✓ 1.0625 Gbaud ✓ 2.125 Gbaud ✓ 2.5 Gbaud ✓ 3.125 Gbaud ✓ 4.25 Gbaud

2. What Serial FPDP function does the interface support?

__Transmitter only __Receiver only ✓ Transmitter & Receiver

3. Does the Receiver support Flow Control (setting the STOP signal)?

__Always active __Not supported ✓ Optional (selectable)

4. Does the Transmitter support Flow Control (data transmission stops after a STOP signal)?

__Always active __Not supported ✓ Optional (selectable)

5. If the Transmitter supports Flow Control, after transmitting a STOP signal, how many 32-bit words can be received before a Receive FIFO overflow occurs?

✓ Programmable

6. Does the interface support CRC?

__Always active __Not supported ✓ Optional (selectable)

7. Does the Transmitter support Copy Master Mode (insertion of additional IDLE ordered sets)?

__Always active __Not supported ✓ Optional (selectable)

8. Does the Receiver support Copy Mode (re-transmission of data)?

✓ Yes __No

9. If Copy Mode is supported, what method is implemented (see VITA 17.1 Observation 6.1.4.4)?

__Method 1 ✓ Method 2

10. Does the Receiver support Copy/Loop Mode (re-transmit data and set Flow Control)?

✓ Yes __No

11. What type of media is supported?

✓ Short Wave Laser ✓ Long Wave Laser ✓ Copper

12. What type of media connectors are supported?

✓ LC __SC __ST ✓ Micro Twinax

13. Which fiber transmit data frames are supported in addition to Normal Data Fiber Frames (see VITA 17.1 Permission 7.3.3.1)?

✓ Sync without Data Fiber Frames ✓ Sync with Data Fiber Frames

14. Does the Serial FPDP Transmitter stop in response to the Serial FPDP Receiver sending NRDY True (see VITA 17.1 Observation 7.3.2.2)?

__Always __Never ✓ Optional (selectable)

15. Are status bits kept up to date when there is no data to transmit by sending empty Serial FPDP Normal Data Fiber (see VITA 17.1 Rule 7.3.3.8, Recommendation 7.3.3.2 and Suggestion 7.3.3.1)?

✓ Yes, empty frames transmitted __No, status is not updated when no data is transmitted