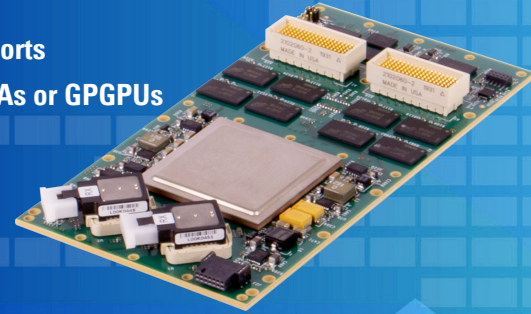


## EnsembleSeries™ IOM-400 Mezzanine High-speed FPGA-based Programmable I/O Module

FPGA supported XMC I/O mezzanine bridging sensor data to PCIe-attached processors and accelerators

- Twenty-four channel, front-panel access fiber I/O or eight channel copper I/O ports
- Bridging/processing incoming sensor data to PCIe-connected processors, FPGAs or GPGPUs
- Xilinx Kintex Ultrascale+ FPGA with multiple population options for scalability
- Fast, rugged open system XMC mezzanine for wideband streaming I/O
- Optional embedded BuiltSECURE systems security engineering



The EnsembleSeries® IOM-400 is a robust and versatile embedded streaming I/O module that conforms to the open standard XMC form-factor. IOM-400 mezzanines are ideally suited to bridge incoming sensor data streams to PCIe connected processors including Intel CPUs and GPGPU and FPGA accelerators.

Built on Xilinx's Kintex Ultrascale+ FPGA baseline, each EnsembleSeries IOM-400 mezzanine is highly configurable, supporting various data stream protocols. A typical use case is to receive I/O in a custom format (e.g. Ethernet frames), perform front-end processing and then send data to a CPU or GPGPU accelerator via PCIe.

The IOM-400's primary processing resource is Xilinx's latest Ultrascale+ Kintex FPGA device. With supporting DDR4 DRAM and local flash storage, the IOM-400 is a key building block for any subsystem managing incoming digital I/O streams.

### Optional BuiltSECURE

For deployment at the tactical edge and export to allies, the EnsembleSeries IOM-400 family of mezzanines optionally embeds BuiltSECURE technology to counter nation-state reverse engineering with system security engineering (SSE). BuiltSECURE is built-in SSE that enables turnkey or private and personalized security solutions to be quickly configured. The extensible nature of Mercury's SSE

**BuiltSECURE™**

delivers system-wide security that evolves over time, building in future proofing. As countermeasures are developed to offset emerging threats, Mercury's security framework keeps pace, maintaining system-wide integrity. Please contact Mercury directly for BuiltSECURE configurations.

### FPGA Configurable Processing

The EnsembleSeries IOM-400 utilizes the Kintex Ultrascale+ KU11P FPGA as its default populated I/O managing device. This FPGA represents the latest in configurable signal processing, I/O management and distribution within an open standards based processing subsystem. Each mezzanine's default FPGA option can be swapped for a larger and more capable KU15P FPGA, should additional resources be needed to meet specific requirements.

### Fiber Optics

IOM-400 mezzanines may be configured with front-panel fiber optics as the physical medium for sensor I/O to be delivered to the FPGA. By default, the IOM-400 is configured with 24 high-speed optical receivers that are capable of operating up to 10.3125 Gbaud. The optics are 50/125  $\mu\text{m}$  multi-mode fiber terminated with MT ferrule connectors that are ideally suited to either external or more commonly interfaced via VITA 66 backplane interfaces. The optics are qualified over the full temperature range to allow the deployment of the IOM-400 in the most rugged of environments and wide temperature ranges. The optics can be configured as 24 receive, 24 transmit, or 12 receive/12 transmit.

*Mercury Systems is a leading commercial provider of secure sensor and safety-critical processing subsystems. Optimized for customer and mission success, Mercury's solutions power a wide variety of critical defense and intelligence programs.*



ACQUIRE



DIGITIZE



PROCESS



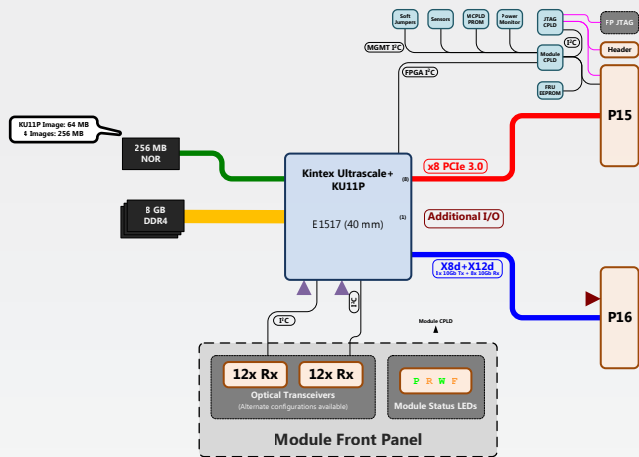
STORAGE



EXPLOIT



DISSEMINATE



### Ensemble Series IOM-400 functional block diagram

The unique 45° rotated position of the fiber optics on the IOM-400 support VITA 66 routing of optical cable that does not protrude beyond the open standards-driven front-panel area when integrated onto a carrier such as the EnsembleSeries SFM6126 PCIe switch. This enables the IOM-400 to be easily deployed across the widest range of rugged subsystem configurations with ease.

For applications where optics are not preferred, eight channels of high-speed copper I/O are available on the P16 XMC user I/O connector.

### Subsystem Scalability

FPGAs within the PCIe environment become part of a scalable system that can expand to provide a fully connected and composable architecture for maximum flexibility. As sensor data planes become more common, a fully connected PCIe fabric can link IOM-400 streaming I/O sources directly to GPGPU co-processors for direct data streams without the added latency of buffering via a general purpose CPU. Mercury's server-class processing modules are designed and tuned to enumerate and manage large PCIe logical trees to facilitate this use case. Artificial intelligence and machine learning application are well suited to the use of the IOM-400 to host the incoming sensor I/O.

### Data-rate Scalable Interconnects

EnsembleSeries IOM-400 mezzanines are configured with VITA 61 XMC connectors by default. The VITA 61 connector offers superior signal integrity characteristics and is a more rugged design, appropriate for high-end XMC modules utilizing Gen3 PCIe interfaces in environmentally challenging applications.

### VPX-REDI

The VPX (VITA 46) standard defines 6U and 3U board formats with high performance interconnects capable of supporting today's high-speed fabric interfaces. VPX may be paired with the ruggedized enhanced design implementation standard — REDI (VITA 48). IOM-400 mezzanines when packaged in conduction-cooled or Air Flow-By modules are VPX-REDI compatible. Air-cooled equivalents conform to the same

OpenVPX form-factor and are suitable for less challenging environments. Targeted for harsh embedded environments, VPX-REDI supports higher functional density and two-level maintenance (2LM). 2LM allowing relatively easily replacement a failed modules.

### Packaging options

EnsembleSeries IOM-400 XMC mezzanines are air-cooled or conduction-cooled and may be integrated in to conduction-cooled, Air Flow-By, Air Flow-Through and Liquid Flow Through OpenVPX modules.

### Specifications

#### Main user FPGA and memory

Xilinx Ultrascale+ KU11P (default) or KU15P (Industrial Grade)  
8 GB of DDR4 SDRAM

#### Flash memory

Capacity 256 MB (able to hold 2 images)

#### PCIe ports to host processor

Gen3 x8 via P15 XMC connector

#### Fiber links (front-panel, optional)

Up to 24 transmit, 24 receive, or 12 transmit/12 receive channels at 10 Gb/s each, full-duplex 850 nm (50/125 μm) multi-mode fiber (~range 150m)  
Also configurable as 3.125 Gb/s (reduced cost build)

#### XMC P16 ports

8 SERDES at up to 10Gb/s – allows for rear transition or remote fiber use (and other uses)

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