Jade 71813

SOSA aligned LVDS with optical I/O XMC module with Kintex UltraScale FPGA

SOSA aligned high-performance offload co-processor

- Customizable I/O signal status and control interface
- Optional front panel optical interface with four 12 Gbps lanes to the FPGA
- Can be used as an optical interface for 10GigE, 40GigE, Aurora or custom protocols

The 71813 is a member of the Jade® family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA based boards, simplifying the design to reduce power and cost, while still providing some of the highest performance FPGA resources available today.

Designed to work with Mercury's Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data processing IP.

In addition to supporting PCI Express Gen. 3 as a native interface, the 71813 includes optional high-bandwidth optical and parallel connections to the Kintex UltraScale FPGA for custom digital I/O.

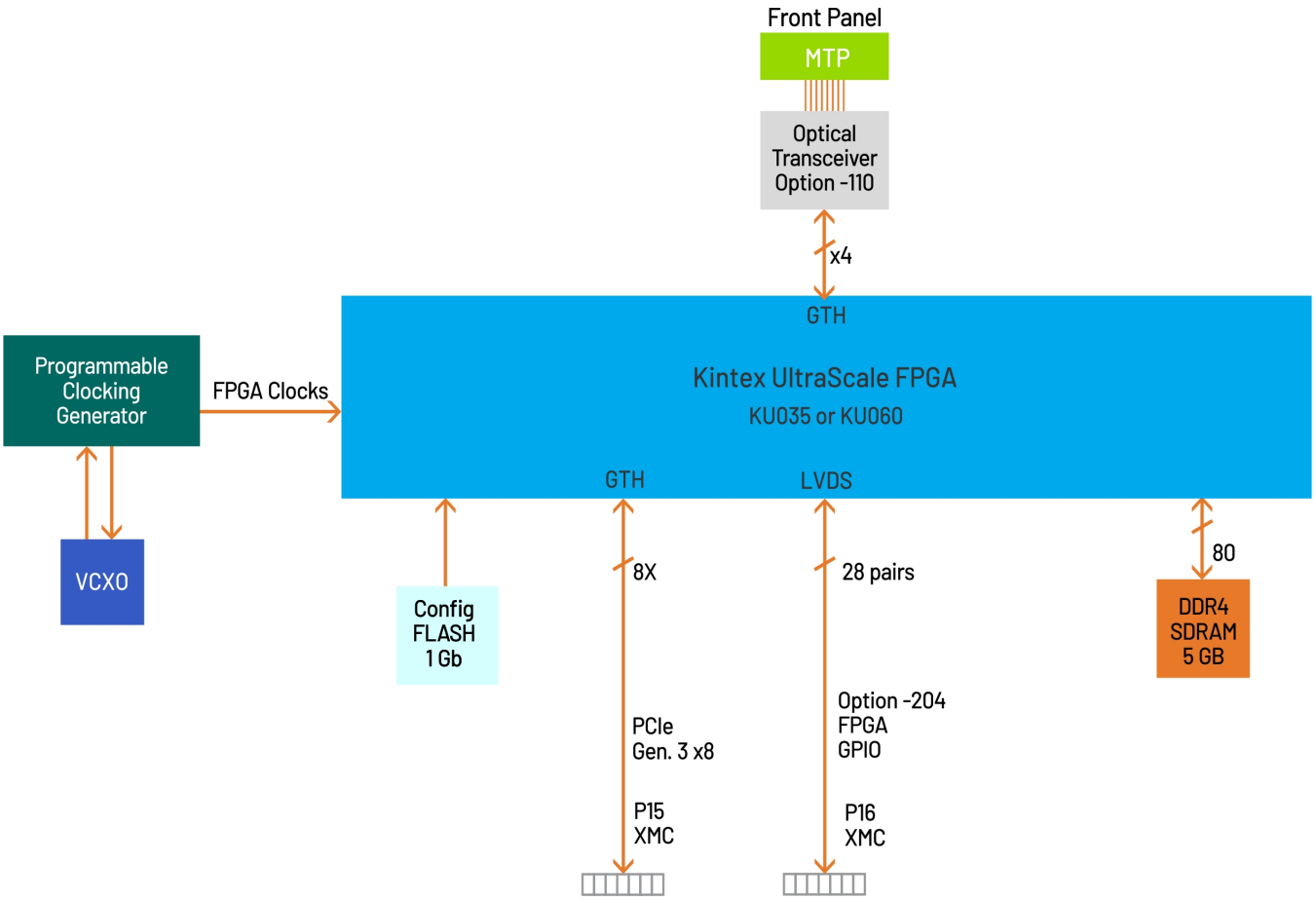
FEATURES

- Supports Xilinx® Kintex® UltraScale™ FPGA
- Developed in alignment with the SOSA™ Technical Standard
- PCI Express interface (Gen. 1, 2 & 3) up to x8
- VITA 42.0 XMC compatible with switched-fabric interfaces
- Optional front panel optical interface
- Ruggedized and conduction-cooled versions
- Navigator Design Suite for software and custom IP development

SOSA™ Sensor Open Systems Architecture

71813 BLOCK DIAGRAM

Click on a block for more information.



THE JADE ARCHITECTURE

Evolved from the proven designs of Mercury's Cobalt® and Onyx® families, Jade® raises the processing performance while lowering the overall power requirements by building on the Xilinx family of Kintex UltraScale FPGAs. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions as well as providing an ideal platform for user-created intellectual property (IP).

EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. The Navigator® FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the wide range of IP functions contained in the Navigator® IP library, or use the Navigator® kit to completely replace the IP with their own.

XILINX KINTEX ULTRASCALE FPGAS

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU060. The KU060 features 2760 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

SUPPORT FOR THE SOSA TECHNICAL SPECIFICATION

Option -204 installs the P16 XMC connector with 28 pairs of LVDS connections to the FPGA for custom I/O. When mounted on a compatible single board computer, the 71813 provides a customizable I/O signal status and control interface to support the emerging Sensor Open Systems Architecture (SOSA™) Technical Standard.

FRONT PANEL OPTICAL INTERFACE

The 71813 can be optionally configured with a front panel MPO optical connector for supporting four 12Gbps lanes to the FPGA. With user-installed FPGA IP, the 71813 can be used as an optical interface for 10 GigE, 40GigE, Aurora, as well as custom protocols.

MEMORY RESOURCES

The 71813 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Mercury-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI EXPRESS INTERFACE

The 71813 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

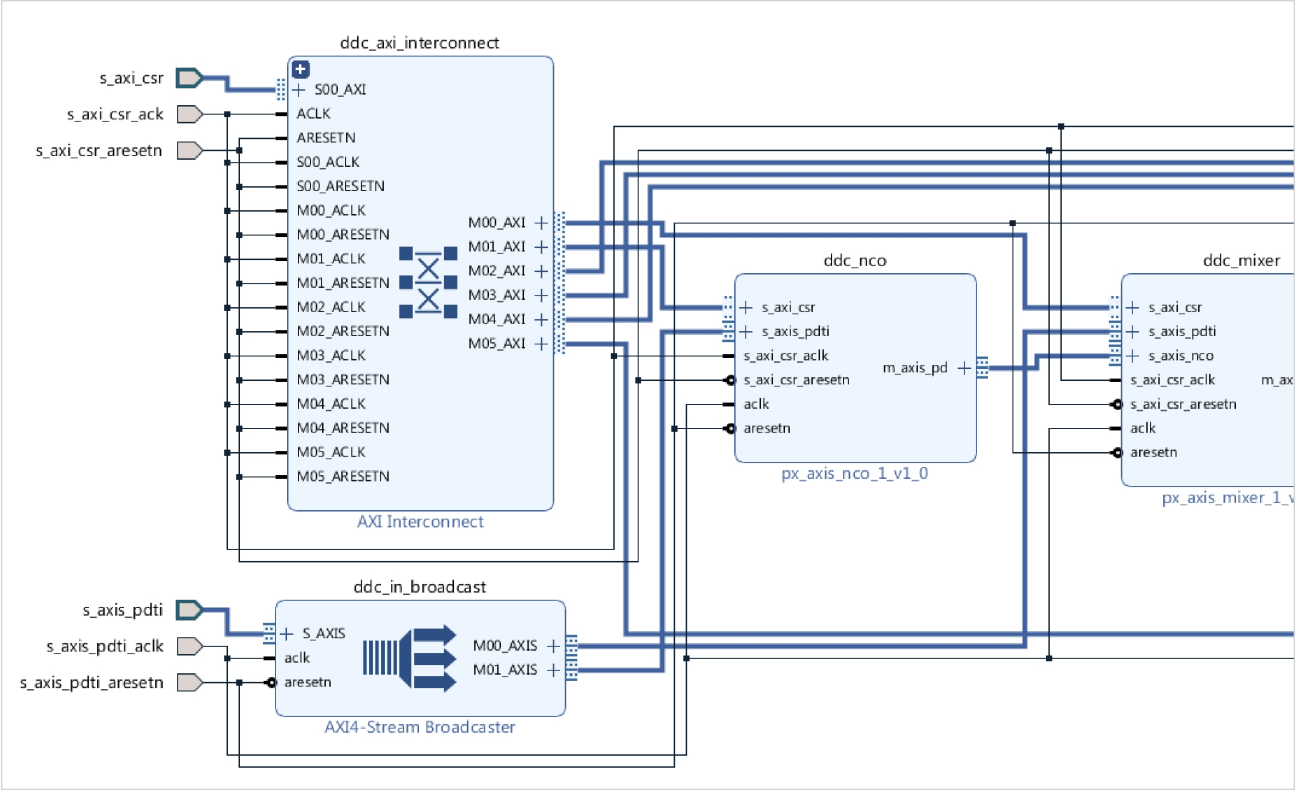
NAVIGATOR DESIGN SUITE

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into the factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

The **Navigator FPGA Design Kit (FDK)** for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Jade product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Jade design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations.

Navigator FDK includes an IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.

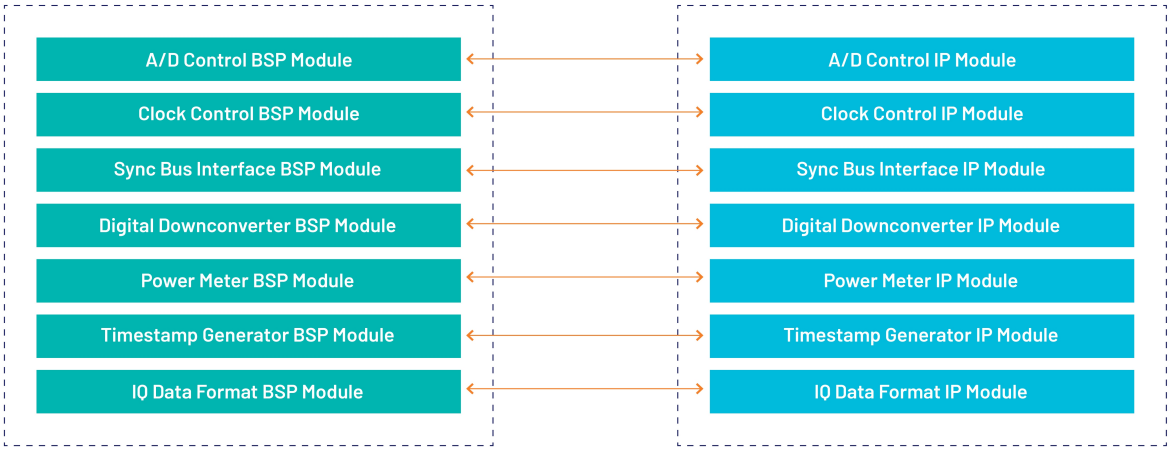
The **Navigator Board Support Package (BSP)** provides software support for Jade boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA. The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.



Navigator IP FPGA Design viewed in IP Integrator

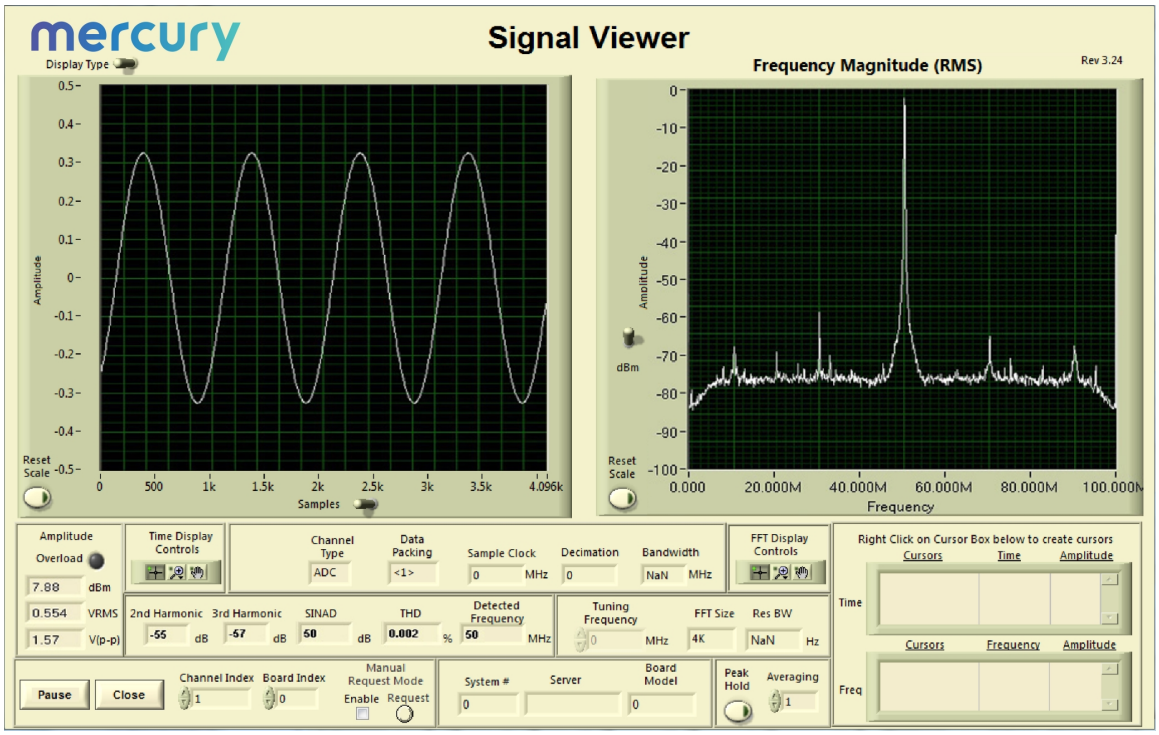
NAVIGATOR BOARD SUPPORT PACKAGE

NAVIGATOR FPGA DESIGN KIT



Because all Jade boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the **Signal Viewer**, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Jade board and Navigator BSP and start viewing analog signals immediately.



SPECIFICATIONS

Field Programmable Gate Array

Standard: Xilinx Kintex UltraScale XCKU035-2

Option -084: Xilinx Kintex UltraScale XCKU060-2

Custom I/O

Option -204: Installs the XMC P16 connector with 28 LVDS pairs to the FPGA

Option -110: Installs a front panel optical MPO connector with an 4X gigabit serial link to the FPGA

Memory

Type: DDR4 SDRAM

Size: 5 GB

Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -713: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: Single XMC module

- Depth: 149.0 mm (5.87 in)
- Height: 74 mm (2.91 in)

Weight: Approximately 14 oz (400 grams)

ORDERING INFORMATION

Model	Description
71813	SOSA Aligned LVDS with Optical I/O and Kintex UltraScale FPGA - XMC

Options:	
-084	XCKU060-2 FPGA
-204	LVDS FPGA I/O through P16 connector
-702	Air-cooled, Level 2
-713	Conduction-cooled, Level 3
-730	2-slot heat sink

Contact Mercury for compatible option combinations and complete specifications of rugged and conduction-cooled versions. Options may change, so be sure to contact Mercury for the latest information.

DEVELOPMENT SYSTEMS

Mercury offers development systems for Jade products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Jade boards. Please contact Mercury to configure a system that matches your requirements.

SOSA ALIGNED JADE PRODUCTS

In addition to the Jade 71813, the following Jade products also are SOSA aligned:

Model	
5585	8-Channel 250 MHz A/D with Virtex UltraScale+ HBM FPGA - SOSA Aligned 3U VPX
5586	Virtex UltraScale+ HBM FPGA Processor - SOSA Aligned 3U VPX

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