

MPS1101 Sensor Processor

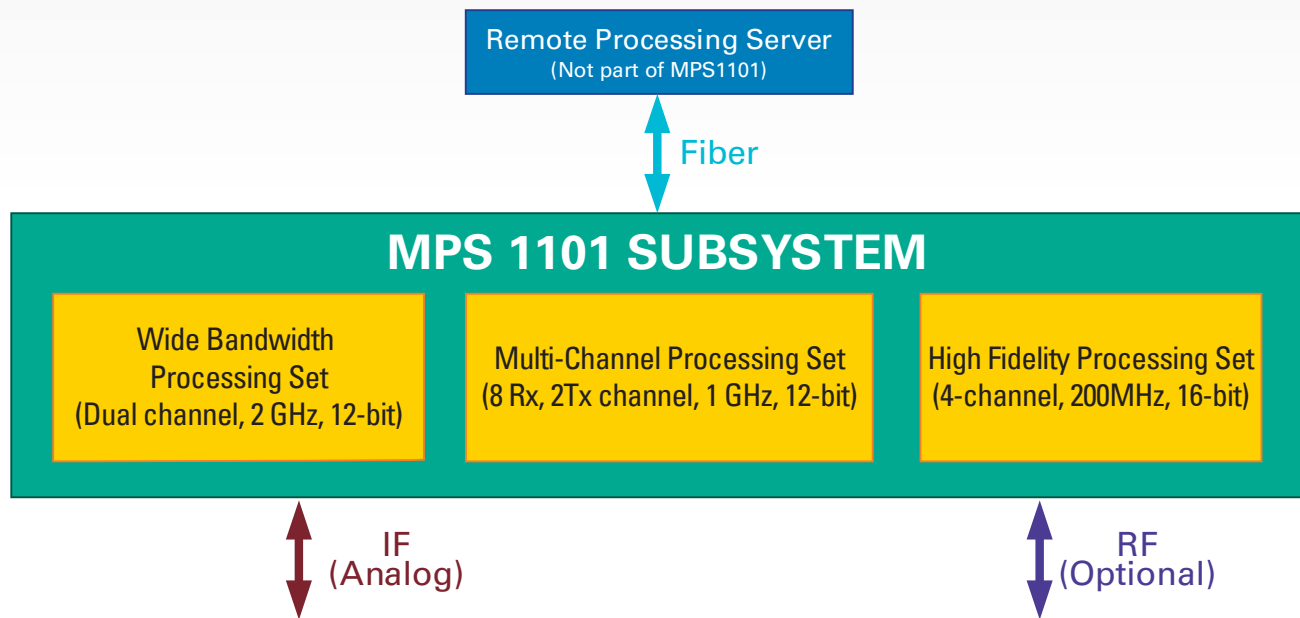
Open Architecture Development Subsystem for Mission-to-Mission Flexibility

- **Wide-bandwidth processing set:** 2Rx and 2Tx channels, 2 GHz, 12-bit
- **Multichannel processing set:** 8Rx and 2Tx channels, 1 GHz, 12-bit
- **High-fidelity processing set:** 4Rx and 4Tx channels, 200 MHz, 16-bit



As adversaries bring new electronic warfare capabilities to the spectrum, it's critical to have the necessary technology in place to discover and respond quickly to effectively counter threats. To achieve this, subsystems need to have a modular and reconfigurable architecture to offer a more rapid, yet secure, way of deploying new systems.

To support this need, Mercury Systems has developed the MPS1101 product family that offers an open architecture, application-ready development subsystem for hardware, software and firmware. With the design flexibility built in, users can leverage a wide range of hardware sets, plus turnkey firmware and software, to easily prototype and develop subsystems that meets their mission-specific needs.



Application ready

Users can leverage the MPS1101 subsystem's multiple processing sets and flexible design to build exactly what is needed for a mission-to-mission solution without the long timelines historically required for subsystem builds with similar capabilities.

Multiple processing components

- Rapid prototyping
- Tactical application demonstrator
- Radar/EW (wideband, low latency)
- Communications (multichannel, wideband)
 - Communication protocols
 - COMINT
 - SDR
- ELINT processor
 - High fidelity, multichannel
- AI/cognitive/machine learning
- Remote sensor
 - High-power, intelligent processing
 - Off-subsystem data transmission over high-speed fiber

Multiple software execution loops for multiple applications

- Real-time execution loop
 - FPGA processing resources of the hardware
- Near real-time loop
 - FPGA capabilities of the hardware and embedded real-time processing from the Intel-based microprocessors
- Processed Signal loop
 - Leverages the signal reduction capabilities of the processing hardware to refine waveforms for large data set processing (AI, PDW, Machine Learning)
- Operator initiated loop
 - Main-in-the-loop commands

A customizable subsystem with open hardware, software and firmware allows for the creation of a product that not only has the ability to test systems prior to deployment, but also the security features necessary for reliable and expedited deployment. The MPS1101 helps ensure effectiveness of the subsystem from design phase to operation in the field.

Real Time (nsec)

```

            graph LR
            In[Input Signal] --> AD[ADC/DAC/FPGA]
            AD --> Out[Output Signal]
            
```

Used For:

- DRFM
- Coherent EA
- Fire on Energy
- Pulse on Pulse

Near Real Time (µsec)

```

            graph LR
            In[Input Signal] --> AD[ADC/DAC/FPGA]
            AD --> Out[Output Signal]
            AD -- Digital RF --> SBC[SBC]
            SBC -- Response --> AD
            
```

Used For:

- Reactive EW
- Minimal Processing
- AoA with Response
- Complex EW/IO

Processed Signal (msec/sec)

```

            graph LR
            In[Input Signal] --> AD[ADC/DAC/FPGA]
            AD --> Out[Output Signal]
            AD -- Digital RF --> SBC[SBC]
            SBC -- Response --> AD
            SBC -- Response --> Ser[Server]
            Ser -- Response --> SBC
            
```

Used For:

- Demod/Remod
- Complex modulation
- AI/ML Functions
- Scripted EW/IO

Operator Initiated Request (As requested)

```

            graph LR
            Op[Operator] -- Digital RF --> Ser[Server]
            Ser -- Digital RF --> SBC[SBC]
            SBC -- Digital RF --> AD[ADC/DAC/FPGA]
            AD --> Out[Output Signal]
            
```

Used For:

- Push button jam (Spectrum/Audio)
- Large streamed digital files
- Microphone
- Record/Playback of files

MPS1101 Module List

Module Description	Processing Set	Processor Type
Single Board Computer (LDS3517)	Dual Channel, Wideband, Low Latency	CPU
Digital Transceiver (DCM3220)	Dual Channel, Wideband, Low Latency	FPGA
Optical I/O Module (IOM400)	Dual Channel, Wideband, Low Latency	Fiber Interface
RFSoc Module (WB3XBM 26)	Multi-Channel (Eight receive, two transmit)	FPGA
CPU (1064 2464)	Multi-Channel	CPU
FPGA Module (5983 w/ 324)	High-Fidelity (Four channel receive/transmit)	FPGA
Single Board Computer (SBC347D)	High-Fidelity (Four channel receive/transmit)	CPU
Critical I/O Storpack	Common Modules	Storage (3TB)
PCIe gen3 Switch (qty2 in subsystem)	Common Modules	Switch
Ethernet Switch	Common Modules	Switch

Need more Help? Need a variant of this product?

For further information, please contact Mercury Systems at electronicwarfare@mercy.com

Innovation That Matters, and Mercury Systems are registered trademarks of Mercury Systems, Inc. Other product and company names mentioned may be trademarks and/or registered trademarks of their respective holders. Mercury Systems, Inc. believes this information is accurate as of its publication date and is not responsible for any inadvertent errors. The information contained herein is subject to change without notice.

Copyright © 2020 Mercury Systems, Inc.

5099.00E 1220 ds MPS1101 Product Family



CORPORATE HEADQUARTERS

50 Minuteman Road
Andover, MA 01810 USA
(978) 967-1401
(866) 627-6951
Fax (978) 256-3599

