Jade 5586

3U VPX SOSA aligned co-processor board with Virtex UltraScale+ HBM FPGA

Co-processor for distributed FPGA processing tasks

- High-Bandwidth Memory (HBM) delivers 20x more memory bandwidth than traditional DDR4 solutions
- Board interfaces: 1 GigE, 10 GigE, 40 GigE, dual 100 GigE and PCIe
- High-bandwidth memory, FPGA logic and DSP density make this board a single-slot 3U VPX processing powerhouse

The 5586 is a high-performance, SOSA aligned 3U OpenVPX co-processor board based on the Xilinx Virtex UltraScale+ HBM FPGA. It serves as an ideal stand-alone processor or as a co-processor for distributed FPGA processing tasks.

Ample data transfer bandwidth and flexibility are provided by a range of board interfaces including 1 GigE, 10 GigE, 40 GigE, dual 100 GigE and PCIe with installation of Mercury or user-supplied IP. The Virtex UltraScale+ HBM's on-chip high-bandwidth memory coupled with the FPGA's logic and DSP density enable the 5586 to be a single-slot 3U VPX processing powerhouse.

FEATURES

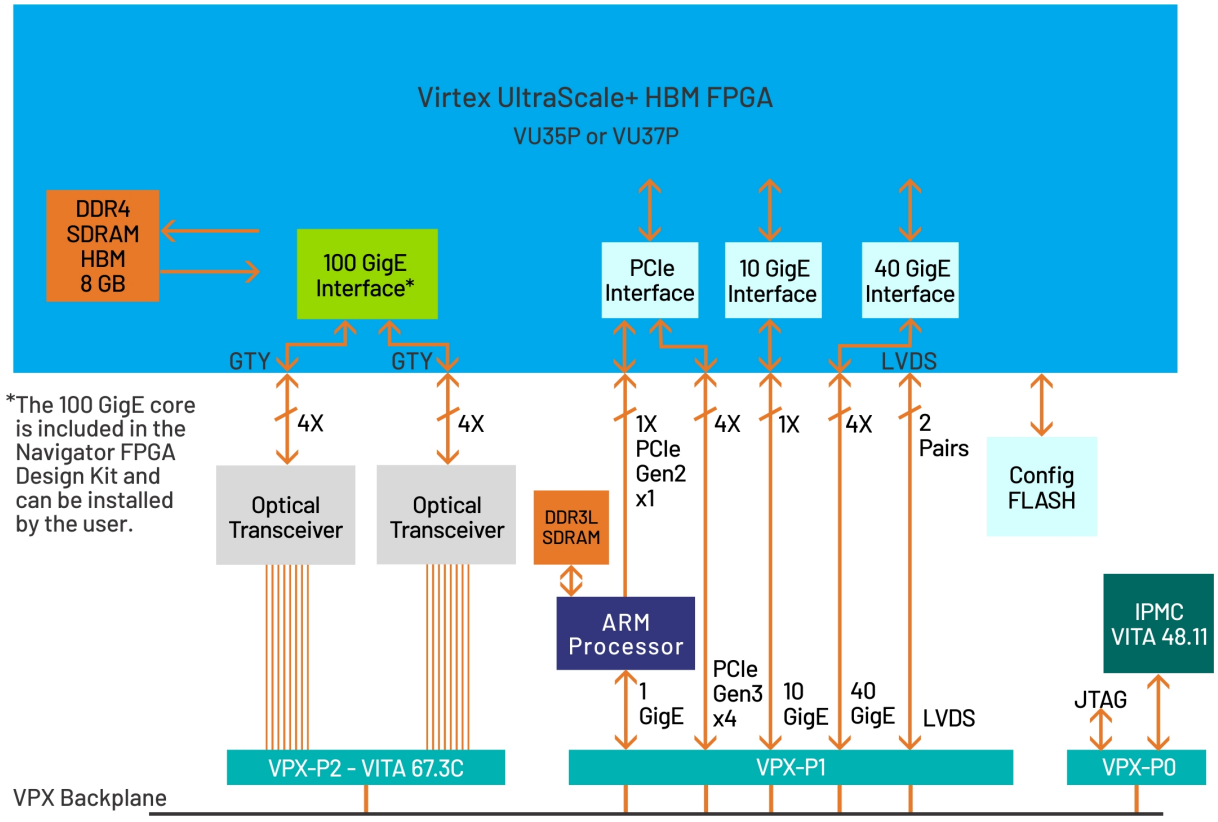
- Features Xilinx Virtex UltraScale+ HBM FPGAs
- 10 GigE Interface and 40 GigE Interface
- Optional VITA 67.3C optical interface for backplane gigabit serial communication
- Dual 100 GigE UDP interface
- Compatible with several VITA standards including: VITA 46, VITA 48.11, VITA 67.3C and VITA 65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled
- Navigator Design Suite for software and custom IP development

BOARD ARCHITECTURE

The 5586 board design places the Virtex UltraScale+ FPGA as the cornerstone of the architecture. All control and data paths are accessible by the FPGA. IP and software are provided to access all board interfaces including PCIe, 10 and 40 GigE. An optional 8-lane optical interface is also available and provides a dual 100 GigE interface with an IP core included with the Navigator FPGA Design Kit and installed by the user.

SOSA™ Sensor Open Systems Architecture

5586 BLOCK DIAGRAM



EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. Mercury's Navigator FPGA Design Kits (FDKs) include the board's FPGA design as a block diagram that can be edited in Xilinx's Vivado IP Integrator. In addition to the IP Integrator block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Mercury factory-installed functions or use the Navigator kit to completely replace the Mercury IP with their own.

The Navigator Board Support Package (BSP), the companion product to the Navigator FDK, provides a complete C-callable library for control of the 5586's hardware and IP. The Navigator FDK and BSP libraries mirror each other where each IP function is controlled by a matching software function, simplifying the job of keeping IP and software development synchronized.

XILINX VIRTEX ULTRASCALE+ HBM FPGA

The 5586 features the VU37P Virtex UltraScale+ HBM. The FPGA's 8 GB of on-chip HBM SDRAM supports memory bandwidth of up to 460 GB/s. This represents better than a 20X throughput increase over traditional, external DDR4 SDRAM. This increased performance addresses the ever-accelerating memory requirements of high bandwidth, high computation applications. Additional resources include 9024 DSP slices, 2.8 million system logic cells and 32.7 Gb/s GTY gigabit serial transceivers.

INTEGRATED PLATFORM MANAGEMENT CONTROLLER

The 5586 uses an Integrated Platform Management Controller (IPMC) to provide a fully compliant and flexible management solution for Field Replaceable Units (FRU) that support the VITA 46.11 standard required by HOST and SOSA architectures. The IPMC provides a standardized implementation of FRU management interfaces, control signals and sensor monitoring.

The IPMC provides the Chassis Manager and higher-level System Management Software (SMS) access to FRU information, FRU control signals and sensor monitoring functions so that they can identify, activate/de-activate, reset and monitor the health of the card and take appropriate system control actions.

The IPMC also provides a low-level path for configuration management and FRU maintenance through both IPMI messages and a Maintenance Port (MP) serial interface. The maintenance port provides a terminal mode command-line interface and supports monitoring, data uploads and FRU-level troubleshooting.

SPECIFICATIONS

ARM Processor

Type: 64-bit Cortex-A53 core

Speed: 800 MHz

Memory: 4 Gb DDR3L SDRAM

Ethernet: 1 GigE on VPX-P1

Field Programmable Gate Array

Type: Xilinx Virtex UltraScale+ HBM XCVU37P

Speed: (standard) -1 speed grade

- Option -002: -2 speed grade

System Logic Cells: 2,852k

HBM DRAM: 8 GBytes

Total Block RAM: 70.9 Mb

UltraRAM: 270.0 Mb

DSP Slices: 9,024

FPGA I/O

Interface: GPIO

- Quantity: 2 pairs
- Type: LVDS
- Location: VPX-P1

Interface: 10 GigE

- Location: VPX-P1

Interface: 40 GigE

- Location: VPX-P1

Interface: Optical (Option -108)

- Quantity: 8 full duplex lanes
- Speed: 26 Gb/sec
- Laser: 850 nm
- Location: VITA 67.3C (VPX-P2)

Interface: PCI-Express

- Type: Gen 1, 2, or 3: x4
- Location: VPX-P1

FPGA Configuration FLASH:
2x 1 Gbit QSPI

Environmental

Option -763: L3 (conduction-cooled)

- Operating Temp: 0° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: VPX board

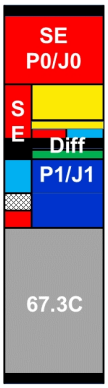
- Depth: 170.61 mm (6.717 in)
- Height: 100 mm (3.937 in)

Weight: TBD

OpenVPX Compatibility

The 5586 is compatible with the following module profile, as defined by the VITA 65 OpenVPX Specification:

SLT3-PAY-1F1U1S1S1U2F1H-14.6.11-12



ORDERING INFORMATION

Model	Description
5586	SOSA aligned 3U VPX co-processor, Virtex UltraScale+ HBM FPGA

Options:	
-002	-2 FPGA speed grade, -1 standard
-108	VITA 67.3C 8X optical interface

Contact Mercury for compatible option combinations and complete specifications of rugged and conduction-cooled versions.

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