DATASHEET

Ensemble® 6000 Series OpenVPX 2nd Generation Intel Core i7 Quad-Core LDS6521 Module

New Low-Density Server Delivers Next-Generation Processing and Fabric Capabilities

(Air-Cooled Version)

- **6U OpenVPX™-compliant VITA 65/46/48 (VPX-REDI) module**
- **Intel® 2nd Generation Core i7 (Sandy Bridge mobile-class) quad-core processor at up to 2.1 GHz with 134 GFLOPS peak performance**
- **POET™-enabled for Gen 2 Serial RapidIO® and/or 10 Gigabit Ethernet fabric**
- **Integrated Gen 2 80-lane PCIe switching infrastructure for on-board and off-board co-processing expansion-plane communications**
- **Mercury MultiCore Plus® software infrastructure support**

The Ensemble® 6000 Series OpenVPX™ 2nd Generation Intel Core i7 Quad-Core LDS6521 Module from Mercury Systems combines a powerful Sandy Bridge mobile-class 2nd Generation Intel Core i7 processor, a high-performance FPGA for both fabric bridging and user-application functions, and high-bandwidth on-board and off-board communication fabrics in a single 6U OpenVPX slot. The LDS6521, as Mercury's next low-density server, provides a next-generation architecture that balances the disruptive computational capabilities of the 2nd Generation Intel Core i7 processor with key high-bandwidth I/O interfaces, providing a powerful and scalable commercial architecture that is well aligned with demanding commercial image processing and data processing applications.

2nd Generation Intel Core i7 Sandy Bridge Mobile-Class Processor

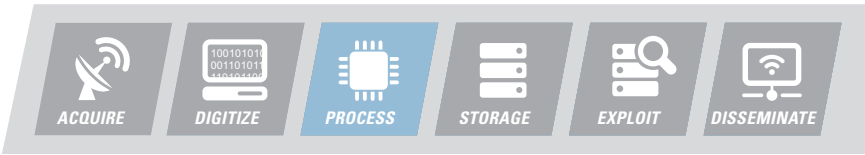
At the heart of the LDS6521 is the Intel 64-bit 2nd Generation Core i7 2715QE processor, running at up to 2.1 GHz. This processor is based on the Sandy Bridge processor architecture, which includes the revolutionary Intel Advanced Vector Extensions (AVX) instruction set. The AVX instruction set doubles the width of the processor's SIMD engine from 128-bit to 256-bit, delivering a significant improvement in floating-point processing. Simultaneously, the 2715QE processor doubles the number of cores on-chip from 2 to 4. The combination of these two architectural advancements results in the LDS6521 delivering approximately 134 peak GFLOPS. The 2715QE includes a large 6-MB cache shared between the cores, allowing many high-performance calculations to remain cache resident. This accelerates processing by eliminating the potential latency required to access DRAM to fetch upcoming data.

The 2nd Generation Intel Core i7 2715QE processor supports dual high-speed DDR3-1333 memory controllers, providing up to 21 GB/s of raw memory bandwidth. Up to 8 GB of DDR3 SDRAM with ECC support can be populated on the LDS6521. The LDS6521 makes use of the Cougar Point-M HM65 Platform Controller Hub (PCH) chipset, which provides integrated graphics capabilities along with I/O bridging between the Intel processor and external devices.

POET Fabric Interconnect Technology

The LDS6521 continues Mercury's fabric innovations by delivering upgraded Protocol Offload Engine Technology (POET™) fabric interconnect capabilities. POET brings the high-bandwidth, low-latency performance of switch fabrics to the LDS6521, providing the bandwidth necessary to eliminate data starvation and to fully utilize the upgraded processing power of Intel 2nd Generation Core i7 technology. The LDS6521

Mercury Systems is a best-of-breed provider of commercially developed, open sensor and Big Data processing systems, software and services for critical commercial, defense and intelligence applications.



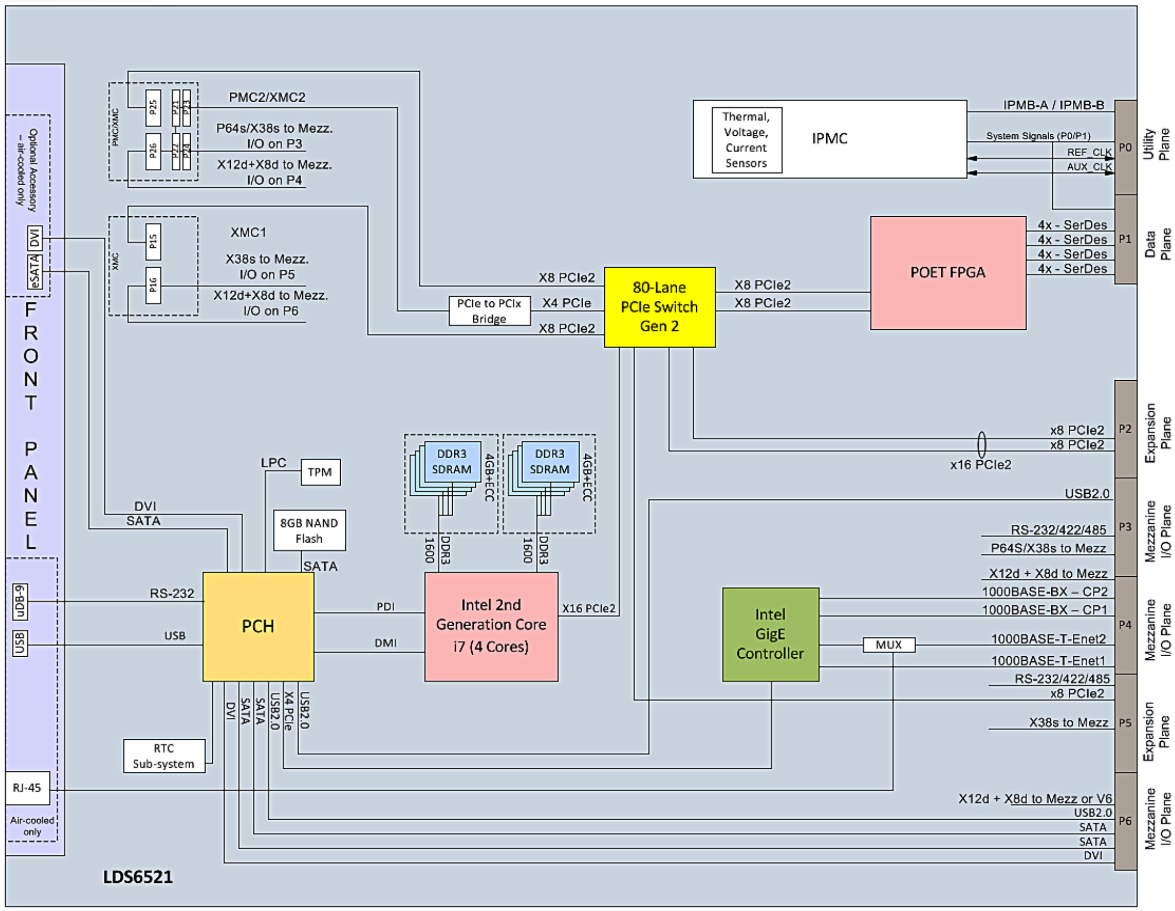


Figure 21 *LDS6521 functional block diagram*

provides four fat-pipe interfaces to the backplane via the POET interface, doubling the available data-plane bandwidth over that available in the prior LDS6520 design. The LDS6521 POET instantiation supports both the high-bandwidth, low-latency, Serial RapidIO® switch fabric (Generation 2), as well as the highly successful 10 Gigabit Ethernet protocol. Changing the Data Plane protocol is as simple as loading a new POET image into the local FPGA.

The LDS6521 POET interface can also provide local switching among multiple fabric ports, allowing scalable mesh-based subsystem designs. The open and downloadable nature of POET allows users of the LDS6521 to implement these different protocols on the OpenVPX data plane without hardware changes. Users can also integrate their custom IP with POET to enhance the value of their subsystems.

The LDS6521 module is compliant to the VITA 65 module profile MOD6-PAY-4F1Q2U2T-12.2.1-n, where n can vary based on POET instantiation. The LDS6521 is supported in chassis slots compliant with VITA 65 slot profile SLT6-PAY-4F1Q2U2T-10.2.1.

PCI Express Architecture

The LDS6521 provides an 80-lane PCIe® switch for both on-board switching and off-board expansion. This Gen2 switch provides a x8 PCIe interface to each of the two XMC sites, as well as an x4 connection to a PCIe to PCI-X bridge for the single PMC site. This allows mezzanines to operate at full bandwidth, optimizing the flow of I/O into the processing subsystem. Additional x8 interfaces are provided to the on-board FPGA, allowing bridging to the data plane without bottlenecking. Externally, the LDS6521 implements a full x16 PCIe connection to the OpenVPX expansion plane on the P2 VPX connector. This expansion-plane interface enables the LDS6521's compatibility with Mercury's GPU or FPGA based co-processing modules. The x16 PCIe connection can be user-configured as dual x8 connections. These configuration options let the module effectively act as an upstream/downstream PCIe switch to allow "chaining" of PCIe devices. An additional x8 PCIe interface is routed to the VPX P5 connector.

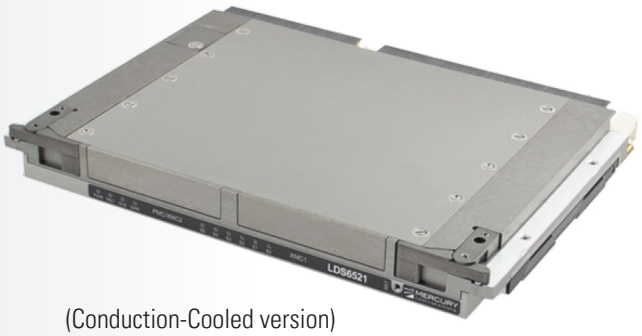
Mezzanine Card Flexibility

The LDS6521 provides two mezzanine sites, one PMC/XMC and one XMC-only. Each of the standard mezzanine sites on the LDS6521 module can be configured with off-the-shelf mezzanine cards to bring additional I/O into the system for processing or control. PMC cards are supported with a 32-bit or 64-bit PCI/PCI-X interface at up to 133 MHz on the PMC/XMC site, with PMC user-defined I/O mapped to the backplane. XMCs are supported with x8 PCIe (Gen1 or Gen2) supported on the J15/J25 connector per the VITA 42.3 standard. There are 20 differential pairs and 38 single-ended signals of XMC user I/O mapped to the backplane via the J16/J26 connector.

Multiple I/O Options

In addition to the flexibility offered via the on-board mezzanine sites, the LDS6521 has a variety of additional built-in I/O options:

- One 10/100/1000BASE-T Gigabit Ethernet connection can be routed to the front panel on air-cooled configurations or to the backplane on conduction-cooled configurations.
- One additional 10/100/1000BASE-T Gigabit Ethernet connection is routed to the backplane.
- Two 1000BASE-BX SERDES Ethernet connections are routed to the backplane per the OpenVPX control-plane specification.
- Two DVI graphics interfaces are provided. One is routed to the front panel on air-cooled configurations only via an optional I/O adaptor. The other is routed to the backplane, allowing the LDS6521 to provide a full graphical display in any configuration, if needed by the application.
- One TIA-232 serial port is routed to the front panel on air-cooled configurations, or to the backplane on conduction-cooled configurations. When routed to the backplane, the serial interface can be configured for either TIA-232 or TIA-422/TIA-485 signaling.
- One front panel USB 2.0 interface is available on air-cooled configurations.
- Two backplane USB 2.0 interfaces are available with both air-cooled and conduction-cooled configurations.
- One front-panel eSATA interface is provided on air-cooled configurations via an optional I/O adaptor.
- Two SATA interfaces to the backplane are provided to easily interface with storage devices.
- Eight GPIO lines act as discrete I/O usable as input, output, or to generate interrupts on the module.
- Several additional bused signals enhance the functionality of the LDS6521 module.



(Conduction-Cooled version)

System Management

The LDS6521 module implements the advanced system management functionality architected in the OpenVPX Specification to enable remote monitoring, alarm management, and hardware revision and health status.

Using the standard I2C bus and IPMI protocol, the on-board system-management block implements the Intelligent Platform Management Controller (IPMC), in accordance with the VITA 46.11 draft standard. This allows the LDS6521 module to:

- Read sensor values
- Read and write sensor thresholds, allowing an application to react to thermal, voltage, or current variations that exceed those thresholds
- Reset the entire module
- Power up/down the entire module
- Retrieve module Field Replaceable Unit (FRU) information
- Be managed remotely by a Chassis Management Controller at the system level, such as implemented on Mercury's 6U OpenVPX switch fabric modules

VPX-REDI

The VPX (VITA 46) standard defines 6U and 3U board formats with a modern high-performance connector set capable of supporting today's high-speed fabric interfaces. VPX is most attractive when paired with the Ruggedized Enhanced Design Implementation standard – REDI (VITA 48). The LDS6521 module is implemented as a 6U conduction-cooled implementation of VPX-REDI, with air-cooled variants in the same VPX form factor available for less rugged environments.

Targeted primarily for harsh-environment embedded applications, VPX-REDI offers extended mechanical configurations supporting higher functional density, such as Two-Level Maintenance (2LM). 2LM allows relatively unskilled maintenance personnel to replace a failed module and restore the system to an operational state in a limited time period, and also minimizes potential damage to the module.

Additional Features

The LDS6521 module provides all the features typically found on a single-board computer. In addition to the sophisticated management subsystem and fabric interconnect, the LDS6521 module provides users with a toolkit enabling many different application use cases.

Features include:

- • Real-time clock with granularity to 1 ms and time measurement of up to 30 years
- • General-purpose timers for synchronization
- • Watchdog timer to support processor interrupt or reset
- • Multiple boot paths, include netboot, USB boot, and boot from SATA or the on-board 8 GB flash device

Open Software Environment

Mercury leverages over 25 years of multicomputer software expertise, including recent multicore processor expertise, across its many platforms. This strategy is fully applied to the LDS6521 module. Because the processor, memory and surrounding technologies are leveraged across product lines, software developed on the LDS6521 module can interface seamlessly with other Mercury products. The same Linux®or VxWorks® development and run-time environment is implemented on the LDS6521 module as on other Intel-based Mercury platforms across the Ensemble™ 3000, 5000, and 6000 Series.The MultiCore Plus® (MCP) open software environment gives the LDS6521 module access to a wide ecosystem of stacks, middleware, libraries and tools. A key software package available for the LDS6521 module is MultiCore SAL (MCSAL). MCSAL offers the familiar SAL API interface, but is optimized for the multiple on-chip cores available with the Intel Core™ i7 quad-core processor.

The MultiCore Plus (MCP) software environment lets applications use industry-standard middleware such as uDAPL, DRI, CORBA or standard TCP/IP sockets ported to run seamlessly over the fabric. MCP also offers a software tool that can help to migrate legacy applications created with MCOE™ on RACE++® systems into the MCP domain.

Specifications

2nd Generation Intel Core i7 Sandy Bridge Processor

Quad-core with Advanced Vector Extensions (AVX)

2.1 GHz 2715QE

Peak performance	134 GFLOPS (estimate)
Threads per core	2
Intel Virtualization Technology	
DDR3-1333	Up to 8 GB with ECC
Raw memory bandwidth	21 GB/s (total)
Local SATA flash	8 GB
BIOS SPI flash	

Xilinx® Virtex™-6 HX250T or HX380T FPGA

Provides fabric bridging to data plane

Can act as co-processor to execute iFFT/FFT, image or signal processing

Configured from CPU or dedicated configuration ROM

IPMI (System Management)

On-board IPMI Controller

Voltage and temperature monitor

Geographical address monitor

Power/reset control

On-board FRU EEPROM interface

FPGA, CPU and CPLD interfaces

Ethernet Connections

1000BASE-BX Ethernet to P4 connector	2
OpenVPX control plane	
10/100/1000BASE-T Ethernet to P4 connector	1
Accessible via OpenVPX RTM or external chassis interface	
10/100/1000BASE-T Ethernet connection	1
To front panel (air-cooled module) or backplane P4 connector (conduction-cooled module)	

Ethernet functions supported by the chipset include:

UDP, TCP, SCTP, ARP, IPv4, IPv6, IEEE1588, flow control, 802.1P (priority) and 802.1Q (VLAN)

OpenVPX Multi-Plane Architecture

System management via IPMB-A and IPMB-B link on P0 management plane

Quad 4x Serial RapidIO or 10 Gigabit Ethernet interfaces on P1 data plane

Full x16 or dual x8 PCIe expansion plane to P2 connector x8 PCIe expansion plane to P5 connector

Dual 1000BASE-BX Ethernet control plane

PMC-X/XMC Sites

Mezzanine sites	1 PMC/XMC, 1 XMC only
PCI-X-to-PCIe bridge	Connects PMC site to on-board PCIe switch
PMC PCI support	33 and 66 MHz
PMC PCI-X support	66, 100, and 133 MHz

PMC user-defined I/O from J14 to backplane

PCIe XMC sites per VITA 42.3 with XMC user-defined I/O from Jn6 to backplane

Mechanical

6U VPX (air-cooled and conduction-cooled)

1.0" slot pitch

OpenVPX and VPX-REDI

Additional I/O Capabilities

One RS-232 serial interface to front panel (air-cooled) or to the backplane (conduction-cooled)

Configurable for RS-422 or RS-485 signaling when routed to backplane

One front-panel USB 2.0 interface (air-cooled configurations only)

Two USB 2.0 interfaces (air-cooled configurations only)

One front-panel DVI interface (with optional I/O adaptor)

One DVI interface to backplane

One front-panel eSATA interface (with optional I/O adaptor)

Two SATA interfaces to backplane

Eight single-ended GPIO interfaces to backplane

System signals to backplane

NVMRO, ChassisTest, Environmental Bypass, MemoryClear

Compliance

OpenVPX System Specification encompasses VITA 46.0, 46.3, 46.4, 46.6, 46.7, 46.9, 46.11

Compatible with VITA 65

VITA 46/48.1/48.2 (REDI)

Serial RapidIO, PCIe, 10 Gigabit Ethernet

Please refer to Mercury publication "Environmental Protections for Operation at the Tactical Edge" for specific ruggedness levels and cooling options.

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