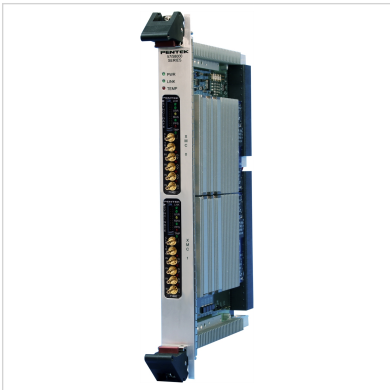


# Jade 57862/58862

4- or 8-channel 200 MHz A/D with multiband DDCs  
6U VPX board with Kintex UltraScale FPGA

## Complete radar and software radio interface solution

- Radar and software radio receiver
- Communications receiver
- Analog signal interface for data recording
- Wideband data acquisition
- Remote monitoring
- Sensor interfaces



### The 57862 and 58862 are members of Jade® family of high-performance 6U VPX boards.

These models consist of one or two 71862 XMC modules mounted on a VPX carrier board. The 57862 is a 6U board with one 71862 module while the 58862 is a 6U board with two XMC modules rather than one.

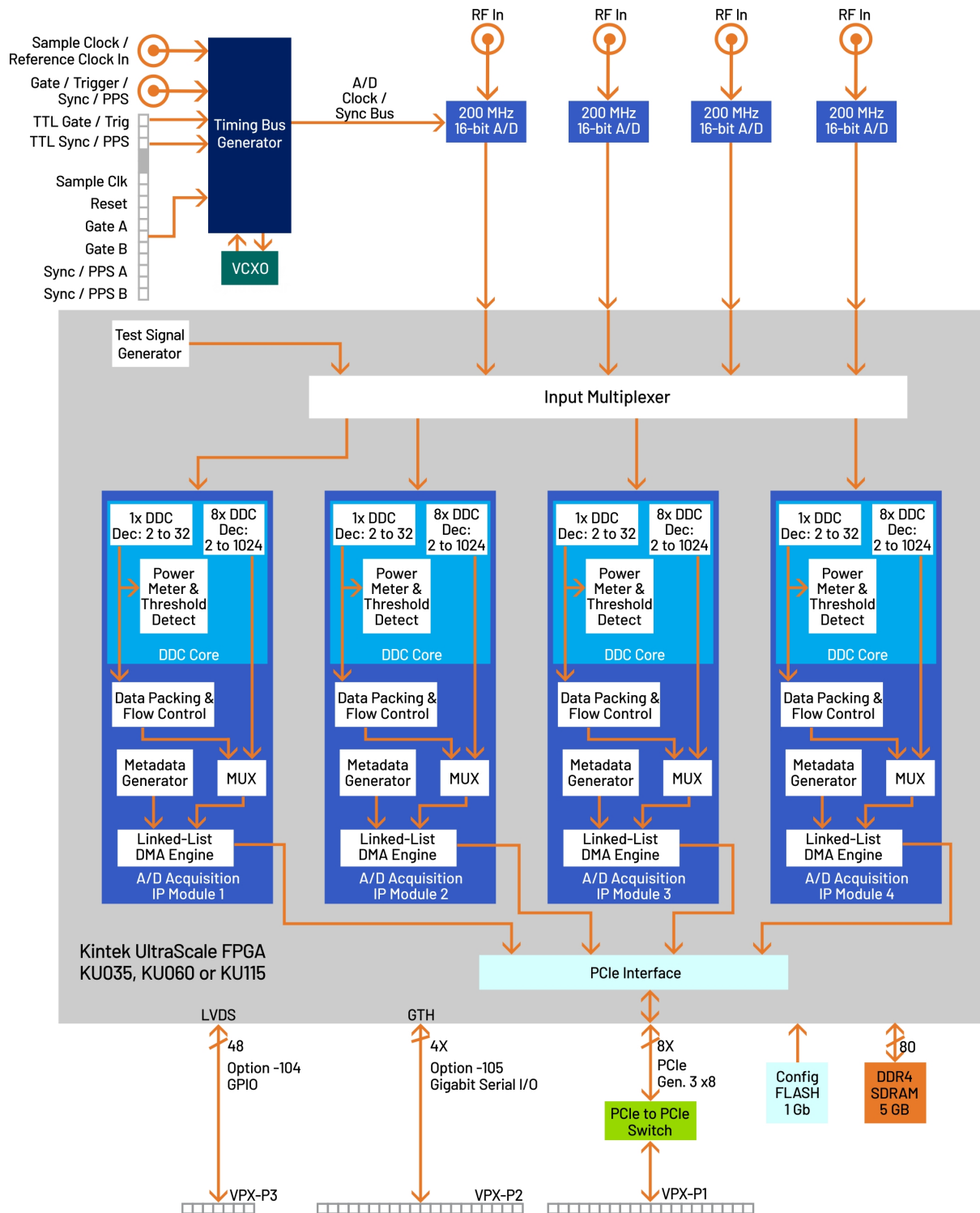
They include four or eight A/Ds, complete multiboard clock and sync sections, and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

### FEATURES

- Xilinx® Kintex® UltraScale™ FPGA
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight wideband multiband DDCs
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express interface (Gen. 1, 2 & 3) up to x8
- Optional LVDS port and gigabit serial connections for custom FPGA I/O
- Ruggedized and conduction-cooled versions
- Navigator Design Suite for software and custom IP development

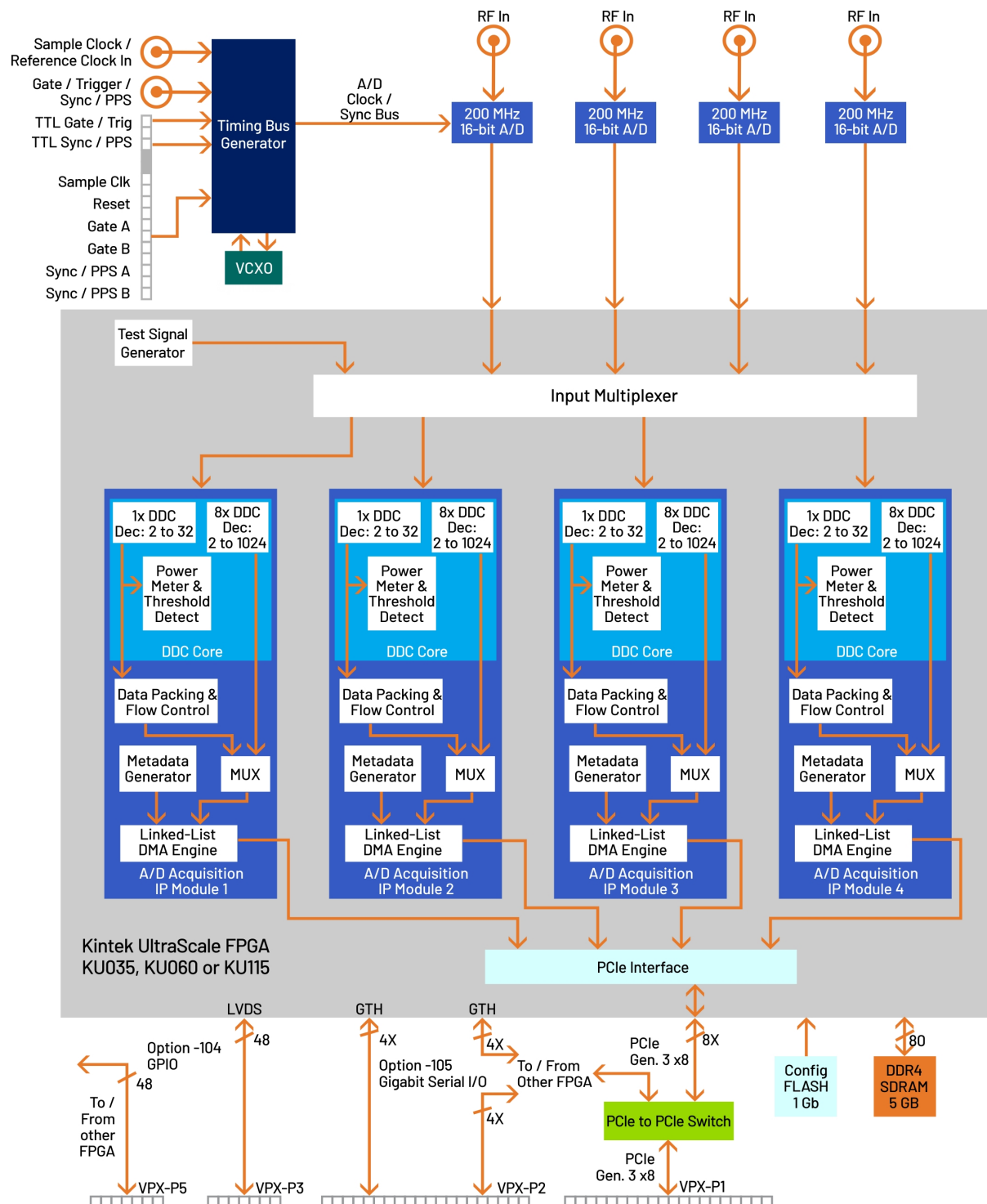
## 57862 BLOCK DIAGRAM

Click on a block for more information.



## 58862 BLOCK DIAGRAM

Block diagram shows half of the 58862. All resources are actually double of what is shown except for the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5.



## THE JADE ARCHITECTURE

Evolved from the proven designs of Mercury's Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions include four or eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the acquisition IP modules contains a powerful, programmable DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

## XILINX KINTEX ULTRASCALE FPGAS

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs: KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

## A/D CONVERTER STAGE

The board's analog interface accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Kintex UltraScale FPGAs for signal processing or routing to other board resources.

## A/D ACQUISITION IP MODULES

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the A/Ds or test signal generators.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

## DDC IP CORES

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each Acquisition Module can choose between the two cores allowing for a very flexible downconversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to  $f_s$ , where  $f_s$  is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to  $f_s$  where  $f_s$  is the A/D sampling frequency. Decimations can be programmed from 2 to 1024.

The decimating filter for all DDCs accepts a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of  $0.8 \cdot f_s / N$ , where  $N$  is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of  $f_s / N$ .

## CLOCKING AND SYNCHRONIZATION

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

Front -panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

## MEMORY RESOURCES

The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Mercury-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

## PCI EXPRESS INTERFACE

These models include industry-standard interfaces fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interfaces include multiple DMA controllers for efficient transfers to and from the boards.

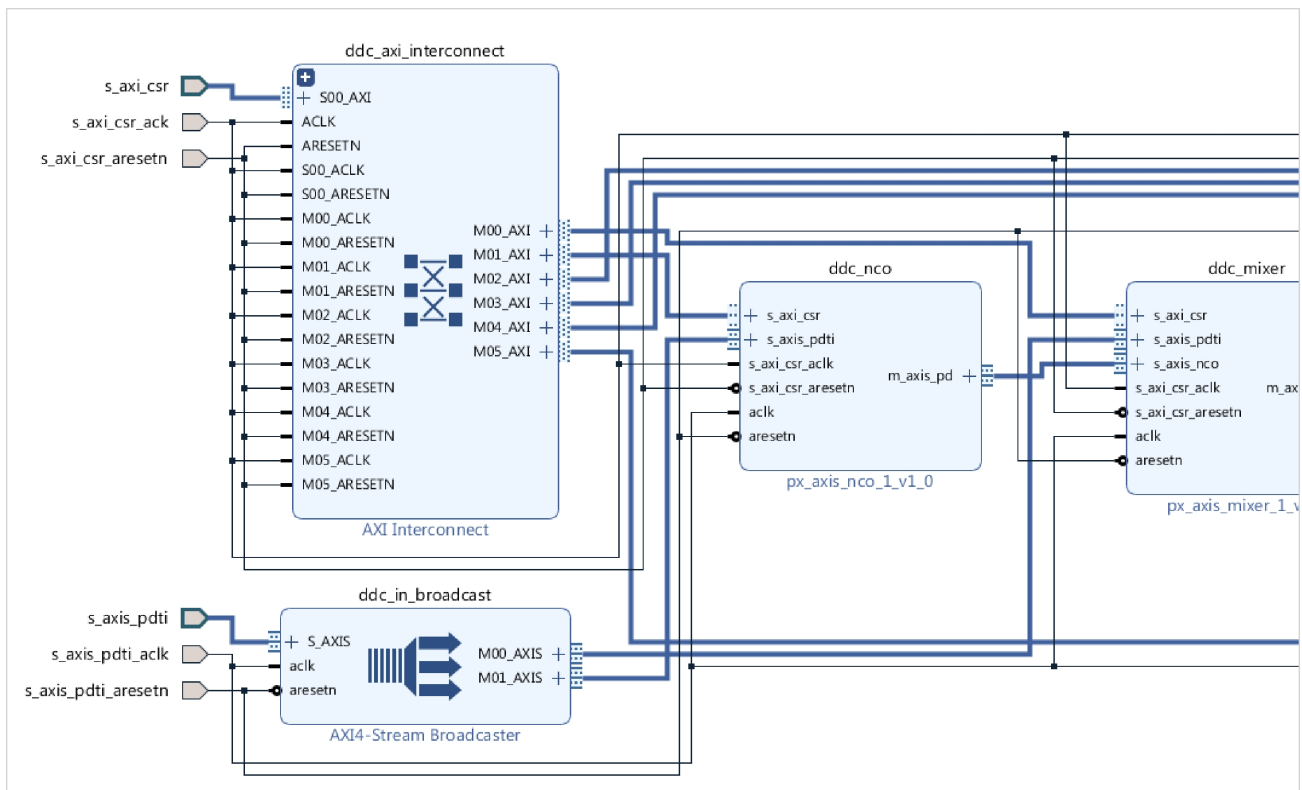
## NAVIGATOR DESIGN SUITE

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into the factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

The **Navigator FPGA Design Kit (FDK)** for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Jade product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Jade design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations.

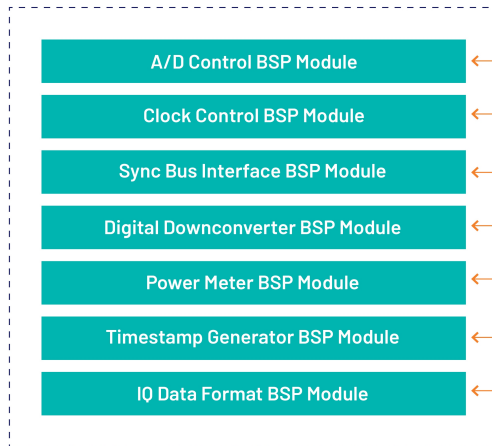
Navigator FDK includes an IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. Multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.

The **Navigator Board Support Package (BSP)** provides software support for Jade boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA. The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.

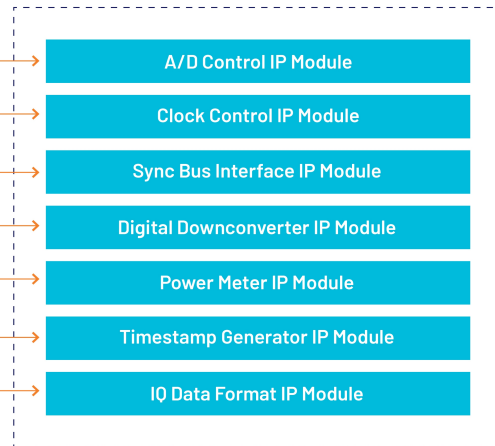


Navigator IP FPGA Design viewed in IP Integrator

## NAVIGATOR BOARD SUPPORT PACKAGE

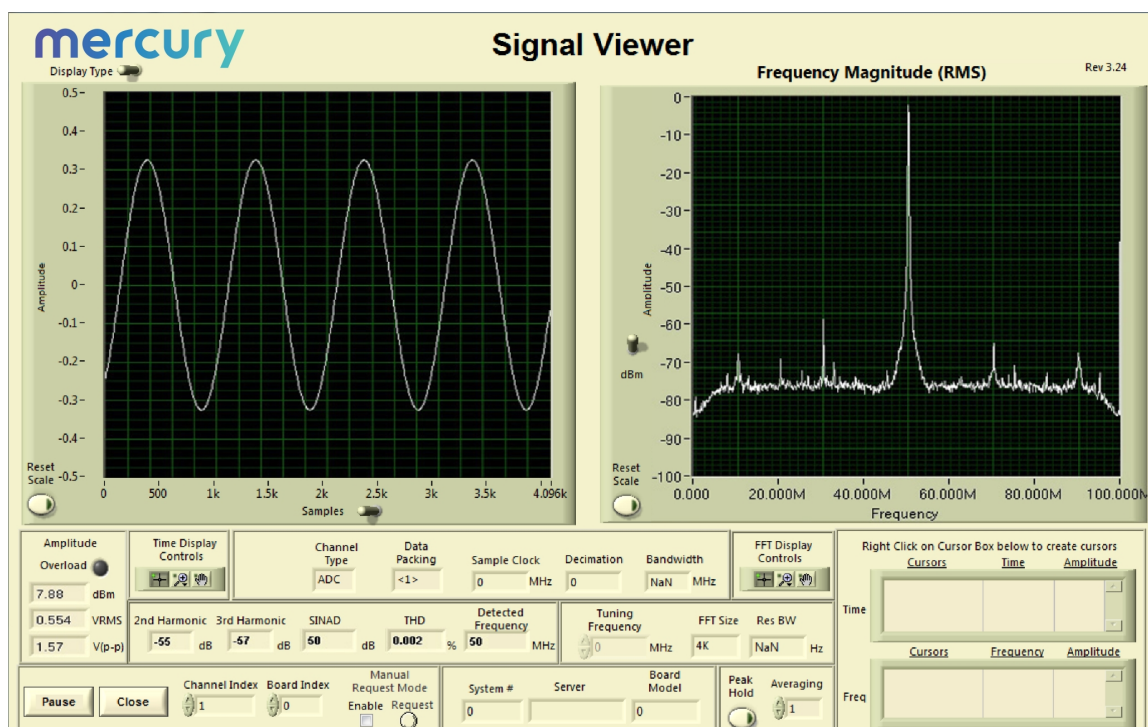


## NAVIGATOR FPGA DESIGN KIT



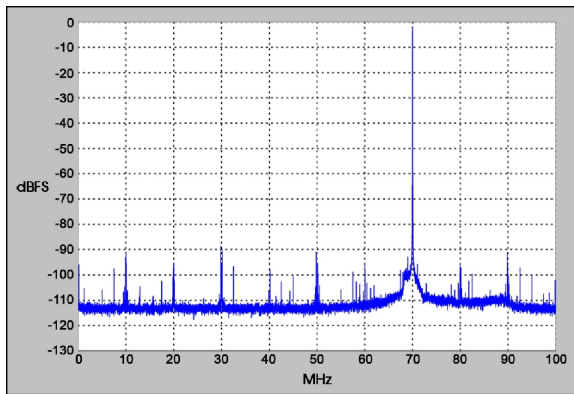
Because all Jade boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the **Signal Viewer**, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Jade board and Navigator BSP and start viewing analog signals immediately.



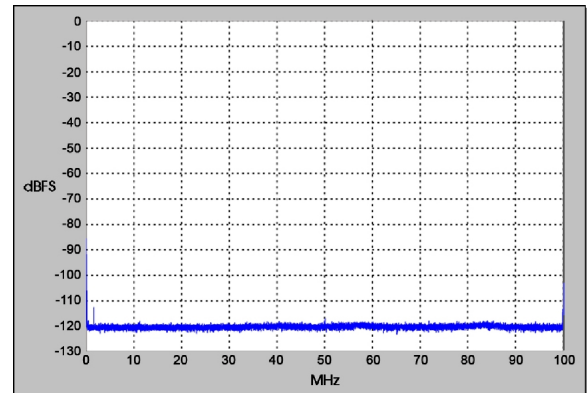
## A/D PERFORMANCE

**Spurious Free Dynamic Range**



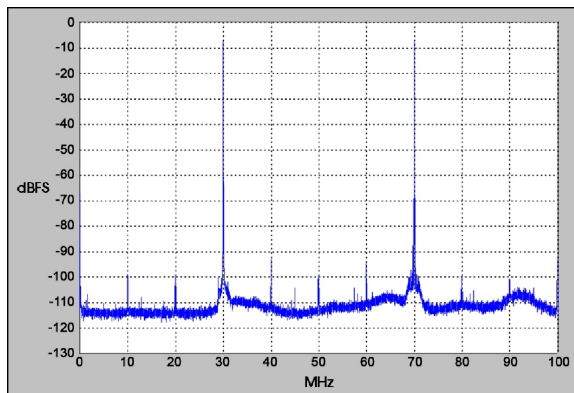
$f_{in} = 70 \text{ MHz}$ ,  $f_s = 200 \text{ MHz}$ , Internal Clock

**Spurious Pick-up**



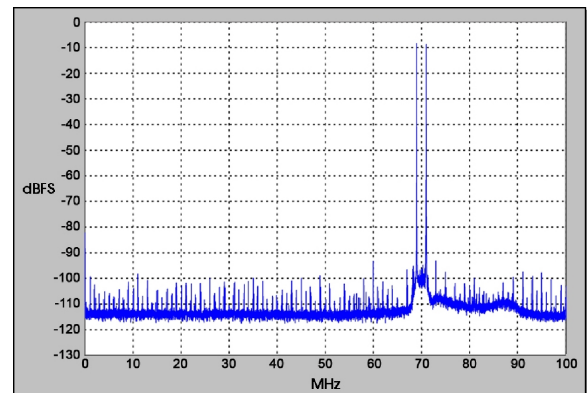
$f_s = 200 \text{ MHz}$ , Internal Clock

**Two-Tone SFDR**



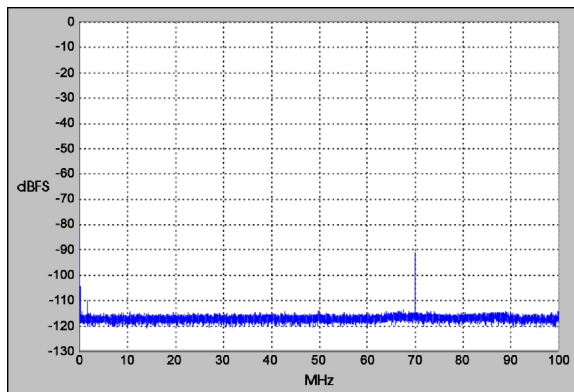
$f_1 = 30 \text{ MHz}$ ,  $f_2 = 70 \text{ MHz}$ ,  $f_s = 200 \text{ MHz}$

**Two-Tone SFDR**



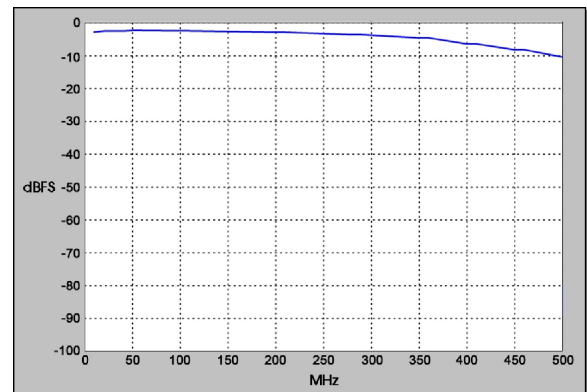
$f_1 = 69 \text{ MHz}$ ,  $f_2 = 71 \text{ MHz}$ ,  $f_s = 200 \text{ MHz}$

**Adjacent Channel Crosstalk**



$f_{in} \text{ Ch2} = 70 \text{ MHz}$ ,  $f_s = 200 \text{ MHz}$ , Ch 1 shown

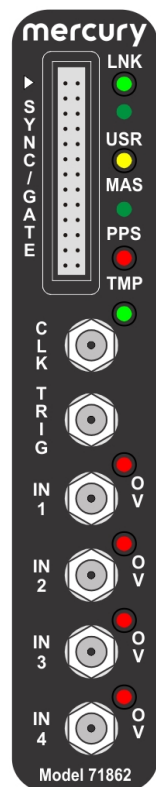
**Input Frequency Response**



$f_s = 200 \text{ MHz}$ , Internal Clock

## FRONT PANEL CONNECTIONS

The front panel includes six SSMC coaxial connectors for clock, trigger, and analog input signals, and a 26-pin Sync Bus input/output connector. The front panel also includes ten LEDs.



### Sync Bus

**Connector:** The 26-pin  $\mu$ Sync front panel connector, labeled **SYNCH/GATE**, provides clock, sync, and gate input/output pins for the Low-Voltage Positive Emitter-Coupled Logic (LVPECL) Sync Bus.

**Link LED:** The green **LNK** LED indicates the link speed when a valid link has been established over the PCIe interface, as follows: Gen 1 – LED blinks slowly (less than once per second); Gen 2 – LED blinks about once per second; Gen 3 – LED will be

constantly on.

- **User LED:** The green **USR** LED is for user applications.
- **Master LED:** The yellow **MAS** LED illuminates when this 71862 is the Sync Bus Master. When only a single 71862 is used, it must be a Master.
- **PPS LED:** The green **PPS** LED illuminates when a valid PPS signal is detected. The LED will blink at the rate of the PPS signal.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage

condition is indicated by any of the temperature/voltage sensors on the 71862 PCB.

- **Clock LED:** The green **CLK** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.
- **Clock Input Connector:** One SSMC coaxial connector, labeled **CLK**, for input of an external sample clock.
- **Trigger Input Connector:** One SSMC coaxial connector, labeled **TRIG**, for input of an external trigger.
- **Analog Input Connectors:** Four SSMC coaxial connectors, labeled **IN 1**, **IN 2**, **IN 3**, and **IN 4**: one for each ADS5485 A/D converter.
- **ADC Overload LEDs:** There are four red **OV** (overload) LEDs: one for each A/D input. Each LED indicates either an overload in the associated ADS5485 or an ADC FIFO overrun.

## SPECIFICATIONS

57862: 4 A/Ds; 58862: 8 A/Ds

### Front Panel Analog Signal Inputs (4 or 8)

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type:  
Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms  
3 dB Passband: 300 kHz to 700 MHz

### A/D Converters (4 or 8)

Type: Texas Instruments ADS5485  
Sampling Rate: 10 MHz to 200 MHz  
Resolution: 16 bits

### Wideband Digital Downconverters (4 or 8)

Decimation Range: 2x to 32x  
LO Tuning Freq. Resolution: 32 bits, 0 to  $f_s$

LO SFDR: >120 dB

Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

### Multiband Digital Downconverters (4 or 8)

Decimation Range: 2x to 1024x

LO Tuning Freq. Resolution: 32 bits, 0 to  $f_s$ , independent tuning for each channel

LO SFDR: >120 dB

Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

### Sample Clock Sources (1 or 2)

On-board clock synthesizer

### Clock Synthesizer (1 or 2)

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 3, 4, 6, 8, or 16 for the A/D clock

### External Clock (1 or 2)

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

## Timing Bus

26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

## External Trigger Input (1 or 2)

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

## Field Programmable Gate Array (1 or 2)

Standard: Xilinx Kintex UltraScale XCKU035-2

Option -084: Xilinx Kintex UltraScale XCKU060-2

Option -087: Xilinx Kintex UltraScale XCKU115-2

## Custom I/O

Option -104: provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57862; P3 and P5 connectors, Model 58862, for custom I/O

Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols

## Memory (1 or 2 banks)

Type: DDR4 SDRAM

Size: 5 GB

Speed: 1200 MHz (2400 MHz DDR)

## PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

## Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

## Physical

Dimensions: VPX board

Depth: 233.35 mm (9.187 in)

Height: 170.60 mm (6.717 in)

Weight: Approximately 14 oz (400 grams)

## ORDERING INFORMATION

Model	Description
57862	4-channel 200 MHz A/D with multiband DDCs and Kintex UltraScale FPGA 6U VPX
58862	8-channel 200 MHz A/D with multiband DDCs and Kintex UltraScale FPGA 6U VPX

## Options:

-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O to VPX P3, Model 57862; P3 and P5 Model 58862
-105	Gigabit serial FPGA I/O to VPX P2
-702	Air-cooled, Level 2
-763	Conduction-cooled, Level 3

Contact Mercury for compatible option combinations and complete specifications of rugged and conduction-cooled versions. Options may change, so be sure to contact Mercury for the latest information.

## ACCESSORY PRODUCTS

Model	Description
2171	Cable Kit: SSMC to SMA

## DEVELOPMENT SYSTEMS

Mercury offers development systems for Jade products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Jade boards. Please [contact Mercury](#) to configure a system that matches your requirements.

## FORM FACTORS

Jade products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Jade Model 71862 XMC (4-Channel 200 MHz A/D with Multiband DDCs, Kintex UltraScale FPGA) has the following variants:

Model	
52862	3U VPX board (single XMC)
57862	6U VPX board (single XMC)
58862	6U VPX board (dual XMC)
71862	XMC module
78862	PCIe board (single XMC)

## LIFETIME SUPPORT FOR JADE PRODUCTS

Mercury offers worldwide customers shorter development time, reliable, rugged solutions for a variety of environments, reduced costs, and mature software development tools. We offer free lifetime support from our engineering staff, which customers can depend on through phone and email, as well as software updates. Take advantage of our 40 years of experience in delivering high-performance radar, communications, SIGINT, EW, and data acquisition MIL-Aero solutions worldwide.



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