Flexor 5973-320

2-channel 3.0 GHz A/D, 2-channel 2.8 GHz D/A 3U VPX board with Virtex-7 FPGA

Complete radar and software radio interface solution

- Radar and communication receiver and transmitter
- Electronic Warfare transponder
- Waveform signal generator
- Wideband data acquisition
- Remote monitoring
- Sensor interfaces

Model 5973-320 is a member of the OnyxFX® family of high-performance 3U VPX baseboards with a Xilinx Virtex-7 FPGA and an available FMC I/O slot. As an integrated solution, the Model 5973-320 FlexorSet® combines the Model 5973 and the Model 3320 Flexor® FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

Designed to allow users to optimize data conversion rates and modes for specific application requirements, the FlexorSet provides preconfigured conversion profiles. Users can use these profiles which include: digital downconverter and digital upconverter modes, conversion resolution and A/D and D/A sample rates, or program their own profiles. In addition to supporting PCIe Gen. 3 as a native interface, the Model 5973-320 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

FEATURES

- Includes Xilinx® Virtex®-7 VXT FPGA
- GateXpress® supports dynamic FPGA reconfiguration across PCIe
- Two 3.0 GHz A/Ds
- Two 2.8 GHz D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for gigabit serial interboard communication
- LVDS connections to the Virtex-7 FPGA for custom I/O and synchronization

THE FLEXOR ARCHITECTURE

Based on the proven design of the Mercury Onyx family of Virtex-7 products, the 5973 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5973-320 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include two A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the acquisition IP modules contains IP for DDR3 SDRAM memories.

The 5973-320 features two sophisticated D/A waveform generator IP modules. A linked-list controller allows users to easily record to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. In each generator module, up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. The GateFlow FPGA Design Kits include all of the factory-installed modules as document source code. Developers can integrate their own IP with the factory-installed functions or use the GateFlow kit to completely replace the IP with their own.

XILINX VIRTEX-7 FPGA

The 5973-320 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

A 4X connection between the FPGA and the VPX P1 connector supports gigabit serial protocols.

Sixteen pairs of LVDS connections are provided between the FPGA and the VPX P2 connector for synchronization and custom I/O.

GATEXPRESS FOR FPGA CONFIGURATION

The Onyx architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

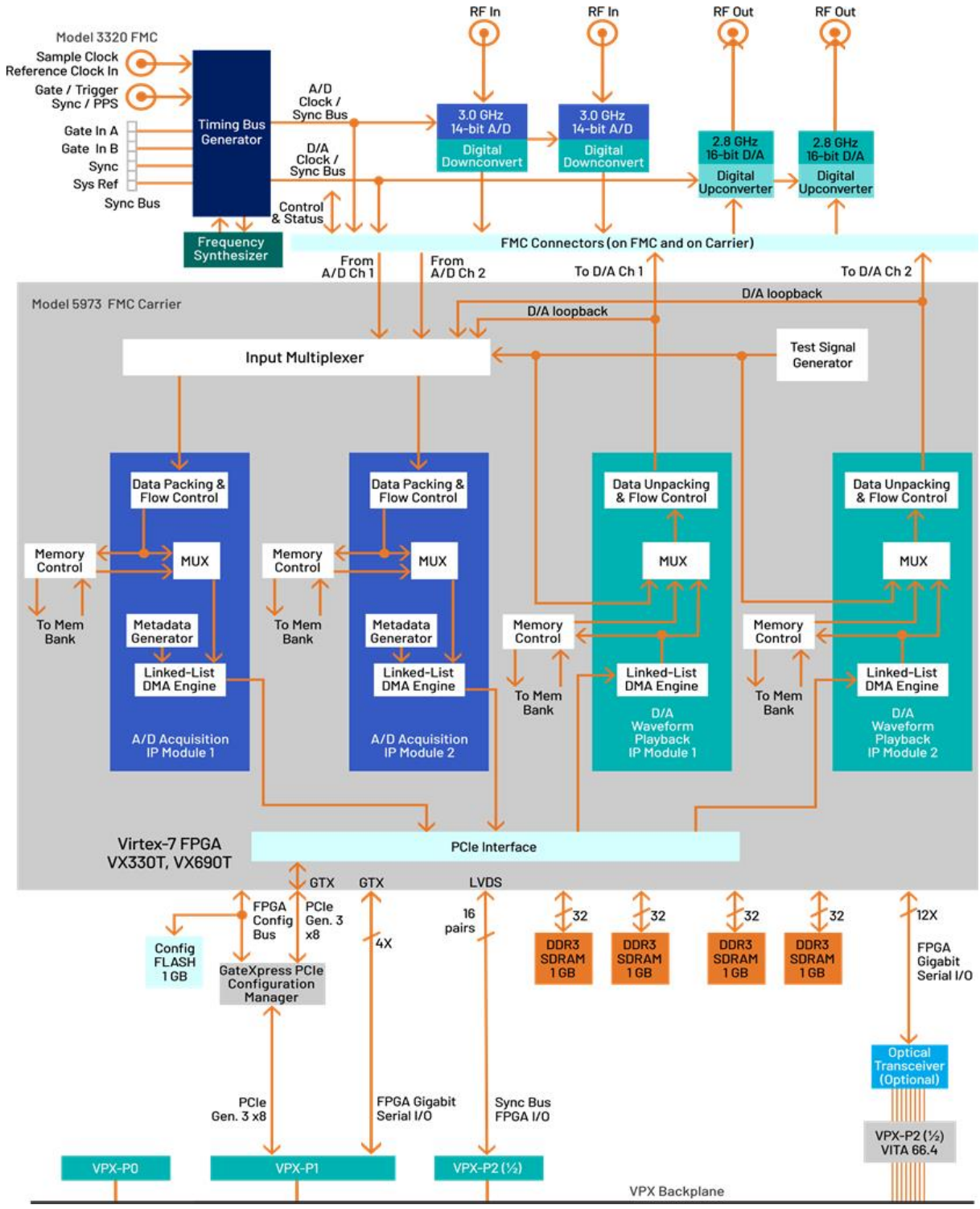
The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting. Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image:

- The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.
- The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.
- The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without a host computer reset to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

5973-320 BLOCK DIAGRAM

Click on a block for more information. See also Preconfigured Conversion Modes.



A/D CONVERTER AND DIGITAL DOWNCONVERTER STAGE

The board's analog interface accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See "Preconfigured Conversion Modes" on page 7 for supported modes.

A/D ACQUISITION IP MODULES

The 5973-320 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the two A/Ds, a test signal generator or from the two D/A Waveform Generator IP modules in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A WAVEFORM PLAYBACK IP MODULE

The 5973-320 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board or off-board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

CLOCKING AND SYNCHRONIZATION

The architecture includes a timing bus generator responsible for providing clocking to the data converters, FPGA and all synchronization circuits. When paired with the 5973, the FlexorSet's built-in functions include setup and support of the timing generator to produce the predefined data conversion profiles. This simplifies operation by allowing users to easily change profiles through software.

The timing bus generator has a built in frequency synthesizer that allows the board to operate without the need for an external sample clock. If users prefer, an external clock can be accepted on a front panel coax connector. In addition, the connector can be programmed to accept a 10 MHz system reference, locking the on-board clock to the reference that enables synchronization across multiple boards.

A front panel LVTTL Gate/Trigger/ Sync connector is also included on the board. Users can program the connector's function to operate in one of three modes to match the application requirements.

MEMORY RESOURCES

The 5973-320 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's waveform playback capabilities, providing local storage for user waveforms. PCI

PCI EXPRESS INTERFACE

The Model 5973-320 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

READYFLOW

Mercury provides ReadyFlow® BSPs (Board Support Packages) for all Cobalt, Onyx, and Flexor products. Available for both Linux and Windows, these packages:

- Provide a path for quick start-up through application completion
- Allow programming at high, intermediate and low levels to meet various needs
- Are illustrated with numerous examples
- Include complete documentation and definitions of all functions
- Include library and example source code.

ReadyFlow BSPs contain C-language examples that can be used to demonstrate the capabilities of Cobalt, Onyx, and Flexor products. These programming examples will help you get an immediate start on writing your own application. They provide sample code that is known to work, giving you a means of verifying that your board set is operational.

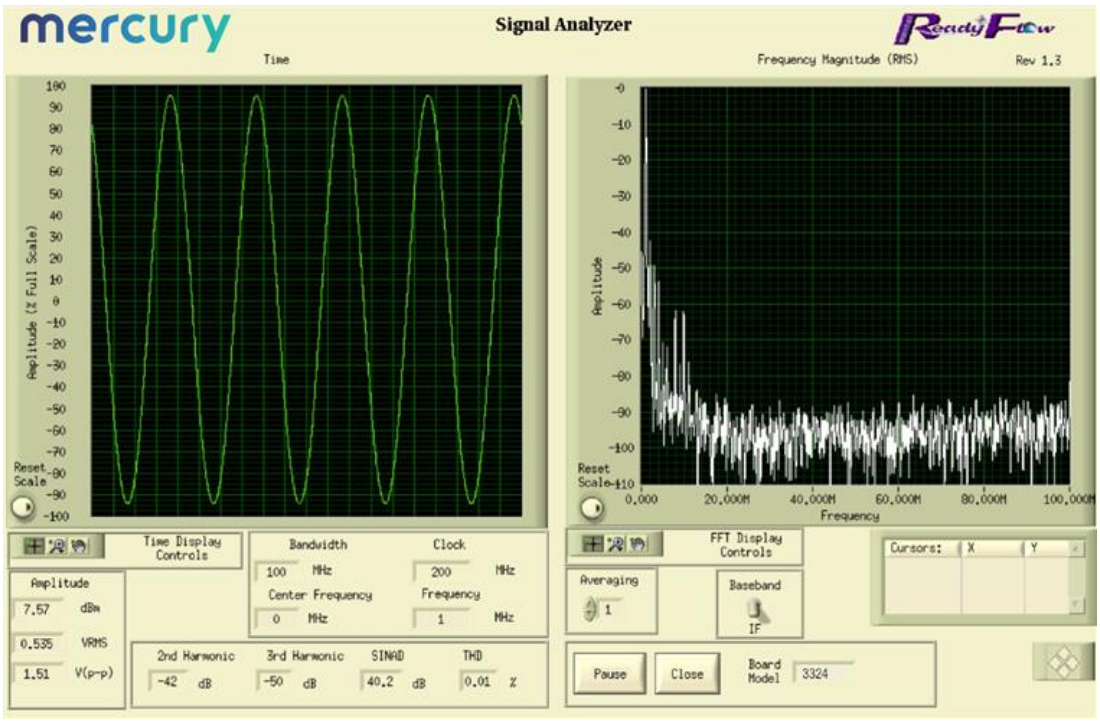
COMMAND LINE INTERFACE

The Command Line Interface provides access to pre-compiled executable examples that operate the hardware right out of the box, without the need to write any code. Board-specific hardware operating arguments can be entered in the command line to control parameters: number of channels to enable, sample clock frequency, data transfer size, reference clock frequency, reference clock source, etc.

The Command Line Interface can be used to call an example application from within a larger user application to control the hardware, and parameter arguments are passed to the application for execution. Functions that control data acquisition automatically save captured data to a pre-named host file or are routed to the Signal Analyzer example function for display.

SIGNAL ANALYZER

When used with the Command Line Interface, the Signal Analyzer allows users to immediately start acquiring and displaying A/D data. A full-featured analysis tool, the Signal Analyzer displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD, and SINAD. Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals.



GATEFLOW

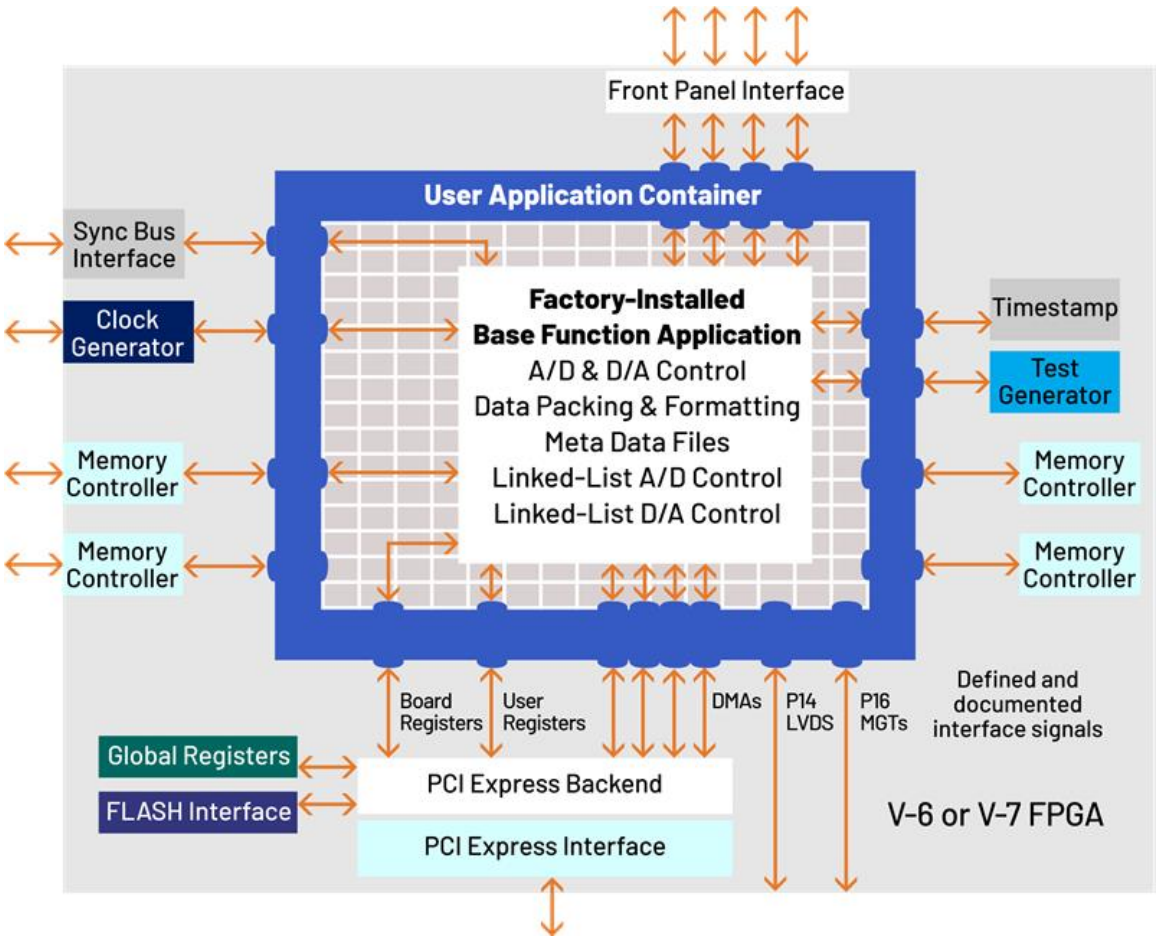
The GateFlow® FPGA Design Kit (FDK) allows the user to modify, replace and extend the standard installed functions in the FPGA to incorporate special modes of operation, new control structures, and specialized signal-processing algorithms.

The Cobalt (Virtex-6), Onyx (Virtex-7), and Flexor (Virtex-7) architectures configure the FPGA with standard factory-supplied interfaces including memory controllers, DMA engines, A/D and D/A interfaces, timing and synchronization structures, triggering and gating logic, time stamping and header tagging, data formatting engines, and the PCIe interface. These resources are connected to the User Application Container using well-defined ports that present easy-to-use data and control signals, effectively abstracting the lower-level details of the hardware.

The User Application Container

Shown below is the FPGA block diagram of a typical Cobalt, Onyx or Flexor module. The User Application Container holds a collection of different installed IP modules connected to the various interfaces through the standard ports surrounding the container. The specific IP modules for each product are described in further detail in the datasheet of that product.

The GateFlow FDK provides a complete Xilinx's ISE or Vivado project folder containing all the files necessary for the FPGA developer to recompile the entire project with or without any required changes. VHDL source code for each IP module provides excellent examples of how the IP modules work, how they might be modified, and how they might be replaced with custom IP to implement a specific function.



PRECONFIGURED CONVERSION MODES

When the Model 3320 is part of a FlexorSet, it is delivered with a set of six preconfigured modes. These allow users to easily select A/D and D/A settings that are commonly used in many applications. While these modes typically satisfy many applications, users can always configure the A/D and D/A settings to their specific requirements via the PCIe interface using the ReadyFlow Board Support Package.

A/D CONVERTER

mode	sample rate	DDC or bypass	output bits resolution	output bandwidth	real or complex	output data rate/chan	usable bandwidth
1	3.0 GHz	dec = 4	16 I + 16 Q	600 MHz	complex	3.0 GB/sec	600 MHz
2	2.8 GHz	dec = 4	16 I + 16 Q	560 MHz	complex	2.8 GB/sec	560 MHz
3	2.8 GHz	dec = 4	16 I + 16 Q	560 MHz	complex	2.8 GB/sec	560 MHz
4	2.5 GHz	bypass	12	2.5 GHz	real	5.0 GB/sec	1000 MHz
5	2.0 GHz	bypass	14	2.0 GHz	real	4.0 GB/sec	800 MHz
6	2.0 GHz	bypass	14	2.0 GHz	real	4.0 GB/sec	800 MHz

D/A CONVERTER

mode	sample rate	DDC or bypass	input bits resolution	real or complex	output data rate/chan	usable bandwidth
1	-	-	-	-	-	-
2	2.8 GHz	int = 2	16 I + 16 Q	complex	5.6 GB/sec	1120 MHz
3	2.8 GHz	int = 4	16 I + 16 Q	complex	2.8 GB/sec	560 MHz
4	-	-	-	-	-	-
5	2.0 GHz	int = 2	16 I + 16 Q	complex	4.0 GB/sec	800 MHz
6	2.0 GHz	int = 2	16	real	2.0 GB/sec	400 MHz

RATIONALE FOR EACH MODE

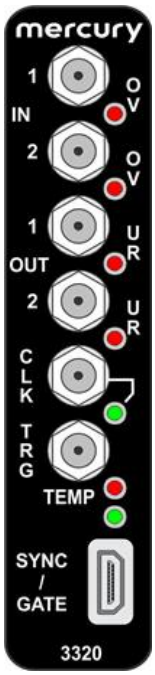
- Mode 1: Maximum A/D sample rate of 3 GS/s, but the DDC must be used. D/A cannot operate at this sample rate.
- Mode 2: Maximum sample rate for A/D and D/A both operating. DDC and DUC must be used, but D/A can generate twice the bandwidth of the A/D bandwidth.
- Mode 3: Maximum sample rate for A/D and D/A both operating (like Mode 2), but now A/D and D/A bandwidths are the same.
- Mode 4: Maximum A/D useable bandwidth achieved with DDC bypass (RAW) output data and 12 bit resolution. D/A cannot operate in this mode.
- Mode 5: Maximum useable signal bandwidth with A/D and D/A both operating. A/D is in bypass with 14-bit resolution. D/A uses DUC with interpolation of 2.
- Mode 6. Like Mode 5 except D/A interpolates real samples instead of complex samples resulting in 400 MHz bandwidth and a simpler output anti-aliasing filter.

GENERAL NOTES

1. "Useable bandwidth" is equal to 80% of the Nyquist bandwidth.
2. Anti-aliasing filters are required for A/D inputs and D/A outputs to ensure elimination of unwanted out-of-band signals per Nyquist criteria.
3. Data rates shown are for the interfaces between the FMC module and the FPGA of the FMC carrier for each channel.
4. By changing board-support software, other operating modes are possible, including different decimations and interpolation.
5. The sample rates shown for each mode are the maximum rates for that mode, but lower rates are also supported with other parameters scaled appropriately.
6. Only one mode is allowed at a time, which defines operations for both A/D and D/A.

FRONT PANEL CONNECTIONS

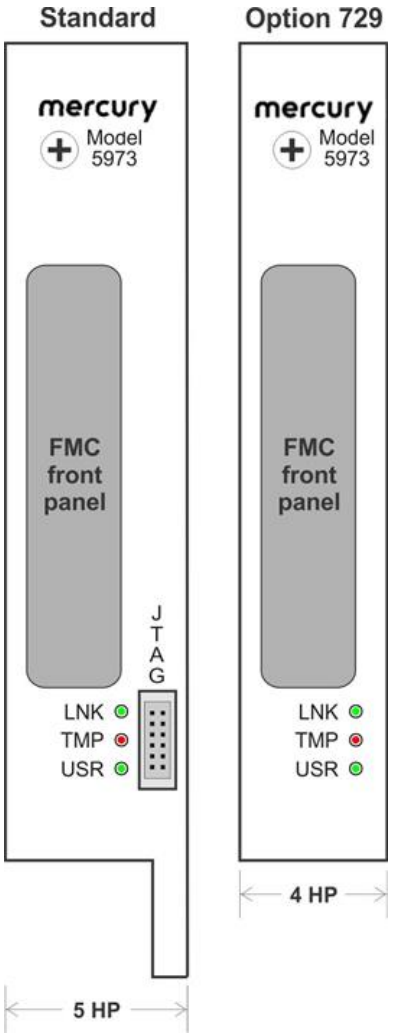
The FMC front panel includes six SSMC coaxial connectors, and a 19-pin µSync connector for input/output of timing and analog signals. The front panel also includes seven LEDs.



- **Analog Input Connectors:** Two SSMC coaxial connector, labeled **IN 1** and **2** one for each ADC input channel to the ADC32RF45.
- **ADC Overload LEDs:** The two red **OV** (overload) LEDs indicate either an overload in the associated ADC32RF45 or an ADC FIFO overrun.
- **Analog Output Connectors:** Two SSMC coaxial connectors, labeled **OUT 1** and **2** one for each ADC32RF45 output.
- **DAC Underrun LEDs:** There are two red **UR** underrun LEDs, one for each DAC output channel. The red underrun LED illuminates when the associated DAC5688 FIFO is out of data.
- **Clock Input Connector:** One SSMC connector, labeled **CLK** for the input of an external sample clock.
- **Clock LED:** The green **EXT CLK IN** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.
- **Trigger Input Connector:** One SSMC coaxial connector labeled **TRG** for input of an external trigger.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the PCB.
- **User LED:** The green unlabeled LED below the **TEMP** LED is for user applications.
- **Sync Bus Connector:** The 19-pin Sync Bus front panel connectors labeled **SYNC/GATE** provides sync and gate input signals for the Sync Bus.

FRONT PANEL CONNECTIONS

The 5973 3U VPX carrier front panel houses the front panel of the FMC module installed on the carrier. The VPX carrier front panel includes three LED indicators below the FMC panel.



- **JTAG Connector:** The VPX carrier front panel provides a 12-pin JTAG connector to download programs and to perform boundary-scan tests on 5973 devices.
- **Link LED:** The green **LNK** LED illuminates when a valid PCIe link has been established over the VPX P1 interface.
- **Over Temperature LED:** The red **TEMP** LED illuminates when an over-temperature or over-voltage condition is indicated by the temperature/voltage sensors on the Model 5973.
- **User LED:** The yellow **USR** LED is available for user applications.

Note: If your 5973 is ordered with Option 763 for mounting in a conduction-cooled VPX chassis, it would have a conduction-cooled VPX Carrier Front Panel.

SPECIFICATIONS

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel connectors
Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS42LB69

Sampling Rate: 10 MHz to 250 MHz

Resolution: 16 bits

Sample Clock Source

On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz) or front panel external clock

Synchronization: VCXO can be phase-locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16

External Clock

Type: Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input

Type: Front panel connector

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- Standard: Xilinx Virtex-7 XC7VX330T-2
- Option -076: Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O

4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Parallel (Option -104): 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory

Type: DDR3 SDRAM

Size: Four banks, 1 GB each

Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: 3U VPX

- Depth: 100 mm (3.937 in)
- Height: 170.6 mm (6.717 in)

ORDERING INFORMATION

Model	Description
5973-320	2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 FPGA - 3U VPX

Options:	
-076	XC7VX690T-2 FPGA
-110	VITA-66.4 12X optical interface
-702	Air-cooled, Level 2
-763	Conduction-cooled, Level 3

Contact Mercury for compatible option combinations and complete specifications of rugged and conduction-cooled versions. Options may change, so be sure to contact Mercury for the latest information.

FLEXORSET MODELS

This chart shows all available FlexorSets. Click on model numbers for more information.

Form Factor	Software/FPGA Tools	Carrier Model	FMC Model	FlexorSet Model	Description
3U VPX	Virtex-7 ReadyFlow BSP GateFlow FDK Vivado	5973	3312	5973-312	4-Channel 250 MHz A/D & 2-Channel 800 MHz D/A
				5973-313	4-Channel 250 MHz A/D & 2-Channel 800 MHz D/A with 4 multiband DDCs & interpolation filters
			3316	5973-316	8-Channel 250 MHz 16-bit A/D
				5973-317	8-Channel 250 MHz 16-bit A/D with 8 multiband DDCs
			3320	5973-320	2-Channel 3 GHz A/D & 2-Channel 2.8 GHz D/A
			3324	5973-324	4-Channel 500 MHz A/D & 4-Channel 2 GHz D/A
	KintexUltraScale Navigator BSP Navigator FDK Vivado	5983*	3312	5983-313*	4-Channel 250 MHz A/D & 2-Channel 800 MHz D/A with 4 multiband DDCs & interpolation filters
			3316	5983-317*	8-Channel 250 MHz 16-bit A/D with 8 multiband DDCs
			3320	5983-320*	2-Channel 3 GHz A/D & 2-Channel 2.8 GHz D/A
			3324	5983-324*	4-Channel 500 MHz A/D & 4-Channel 2 GHz D/A
PCIe	Virtex-7 ReadyFlow BSP GateFlow FDK Vivado	7070	3312	7070-312	4-Channel 250 MHz A/D & 2-Channel 800 MHz D/A
				7070-313	4-Channel 250 MHz A/D & 2-Channel 800 MHz D/A with 4 multiband DDCs & interpolation filters
			3316	7070-316	8-Channel 250 MHz 16-bit A/D
				7070-317	8-Channel 250 MHz 16-bit A/D with 8 multiband DDCs
			3320	7070-320	2-Channel 3 GHz A/D & 2-Channel 2.8 GHz D/A
			3324	7070-324	4-Channel 500 MHz A/D & 4-Channel 2 GHz D/A

*Consult with Mercury about the availability of a 5983A version of this product. For differences, see below.

Model 5983	Model 5983A
Flash Memory - 1 Gbit of FLASH Memory	**Flash Memory -**2 Gbit of BPI FLASH Memory
Optical I/O (Option 110) - VITA 66.4 - Up to 12 duplex optical lanes are available on a VITA 66.4 connector. With the installation of a serial protocol, the VITA 66.4 interface enables a high-bandwidth connection between 5983s mounted in the same chassis or over extended distances.	**Optical I/O (Option 110) - VITA 67.3D -** Provides 12 duplex lanes @ 10 Gb/sec through the lower half of VPX P2 (VPX P2B). With the installation of a serial protocol, the VITA 67.3D interface enables gigabit communications between boards and chassis, independent of the PCIe interface. Consult with Mercury before ordering Option 110 (optical).
	Custom Analog I/O (Option 113) - VITA 67.3 - VITA 67.3 provides 10 coax connections through the lower half of VPX P2.

ACCESSORY PRODUCTS

Model	Description
2171	Cable kit: SSMC to SMA
5292	High-speed synchronizer and distribution board - 3U VPX model
9192	Rackmount high-speed system synchronizer unit

DEVELOPMENT SYSTEMS

Mercury offers development systems for Flexor products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Flexor boards. Please contact Mercury to configure a system that matches your requirements.

Corporate Headquarters
50 Minuteman Road
Andover, MA 01810 USA
+1 978.967.1401 tel
+1 866.627.6951 tel
+1 978.256.3599 fax

International Headquarters
Mercury International
Avenue Eugène-Lance, 38
PO Box 584
CH-1212 Grand-Lancy 1
Geneva, Switzerland
+41 22 884 5100 tel

Learn more

Visit: mrcy.com/go/MP5973-320

For technical details, contact:
mrcy.com/CF5973-320