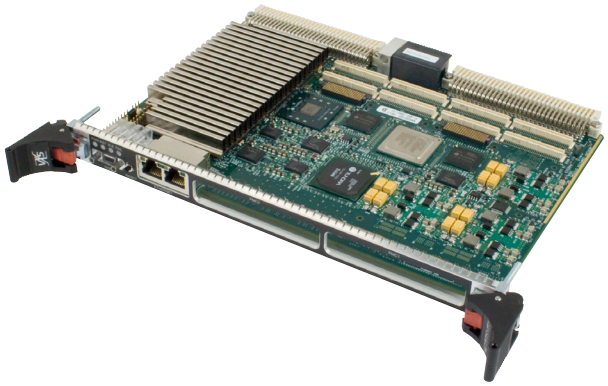
Ensemble™

DATASHEET

MERCURY COMPUTER SYSTEMS™

Ensemble 5000 Series
VXS HCD5220 Module

Balanced I/O and Processing in a Single VXS Payload Slot



- VITA 41 (VXS) 6U serial RapidIO®-enabled air-cooled module
- Two dual-core MPC8641D processors at up to 1.33 GHz
- Balanced processing and I/O
- Identical software infrastructure across Mercury products
- Flexible I/O supported on dual PMC/XMC sites

The Ensemble 5000 Series VXS HCD5220 Dual 8641D Dual-Core Processing Module from Mercury Computer Systems combines high-performance Power Architecture™ processing technology with balanced I/O from dual PMC/XMC sites and the scalable serial RapidIO® interconnect. Designed to meet the needs of a variety of applications, the HCD5220 can function as a single-board computer or as part of an embedded processing cluster for high-end digital signal processing. The HCD5220is supported by the rich set of features available from the cross-product MultiCore Plus® software infrastructure, which allows for ease of portability while offering an open software development architecture.

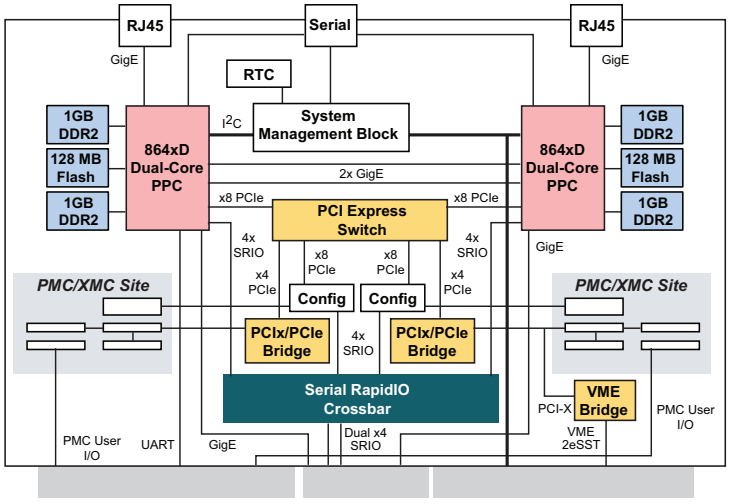


***Figure 1**. HCD5220 functional block diagram*

Power Architecture Processor

The Freescale™ MPC8641D dual-core processor integrates two standard e600 processor cores, two DDR2 memory controllers, 1 MB of L2 cache, and a flexible system-on-chip I/O subsystem. The dual e600 cores that make up the heart of the chip are inherited from the 7448 processor, and each retains the high-performance AltiVec™ vector processing unit. Algorithms optimized for the AltiVec engine port seamlessly to the 8641D. Increased bandwidth between both memory and external I/O and the processing cores allows for efficient processing beyond that available with prior families of Freescale processors.

Mezzanine Card Flexibility

Each of the standard PMC/XMC sites can be configured with off-the-shelf mezzanine cards using either PCI-X or PCI Express® protocols. PMC cards are supported with a PCI/PCI-X interface at up to 133 MHz on the primary site, and up to 100 MHz on the secondary site. PMC user-defined I/O is mapped to the backplane on one of the two PMC sites. XMCs are supported with x8, x4, x2, and x1 PCIe mezzanine cards per the VITA 42.3 standard. The XMC site can also be factory configured to support x1 or x4 serial RapidIO mezzanine cards per the VITA 42.2 standard.

Open System Standards

The HCD5220 employs three independent standards-based communication planes for data input and movement, application control, and system management:

- **ANSI/VITA 41.2: VXS Serial RapidIO Interconnect**
  The onboard serial RapidIO fabric enables communication with other system modules via the VXS P0 connector. Two x4 serial RapidIO links support data transfers at either 2.5 or 3.125 Gbaud, depending on system configuration.
- **ANSI/VITA 41.6: Gigabit Ethernet**
  Gigabit Ethernet is supported at the front panel and via the VXS backplane interface. Each 8641D processor provides a front-panel 10/100/1000Base-T connection via the standard RJ-45 connector. Additionally, each processor provides a separate Gigabit Ethernet interface to the VXS P0 connector compliant with the draft VITA 41.6 (Control Plane) standard. A combined total of 4 Gigabit Ethernet links, enabled by the 8641D system-on-chip interface, are available on each VXS-220 module.
- **ANSI/VITA 38: System Management Bus**
  The HCD5220 implements an onboard system management block, allowing any HCD5220 module in the system to perform remote queries on sensor values, set sensor thresholds, reset local and remote processors, and manage firmware updates. This management plane is implemented in accordance with the VITA 38 System Management Bus specification, implementing an I2C bus over the VME P1 connector.

Additional Features

The HCD5220 provides the many features typically found on a single-board computer. In addition to the sophisticated management subsystem and fabric interconnect, the VXS-220 provides users with a toolkit enabling many different application use cases.

Features include:

- 128 MB of write-protectable boot/application flash per processor with protected boot vector to avoid accidental erasure
- Thermal and voltage sensors integrated onboard
- System management block capable of managing firmware updates, reading and writing sensor thresholds, reading sensor values, and resetting the module
- RS-232 serial interface ports per processor to the front panel with an additional interface optionally routed to the backplane
- Real-time clock with granularity to 1 ms and time measurement of up to 30 years
- General-purpose timers for synchronization
- Watchdog timer able to interrupt each processor upon expiration
- Open board architecture that supports network booting, as well as booting from the onboard flash memory

Open Software Environment

For over 25 years, Mercury has been leveraging multicomputer software expertise, including recent multicore processor expertise, across its many platforms. This strategy is fully applied to the HCD5220. Because the processor, memory, and surrounding technologies are leveraged across product lines, software developed on the HCD5220 can interface seamlessly with other Mercury products. The same Linux® development and run-time environment is implemented on the HCD5220 as on other Mercury systems, such as the Ensemble 7100 and the VPA-200P.

The open software environment gives the HCD5220 access to a wide ecosystem of stacks, middleware, libraries, and tools. The Scientific Algorithm Library (SAL) is optimized for the onboard AltiVec engine, giving the HCD5220 industry-leading signal processing performance. A key new software package available for the HCD5220 is MultiCore SAL (MCSAL), which has the familiar SAL API interfaces, but is optimized for the multiple on-chip cores available with the 8641D.

Software support is available on the HCD5220 for the following products:

- **Open Development Suite for Linux**
  This Eclipse-based integrated development environment (IDE) includes a C/C++ optimizing compiler, a source level debugger, a language sensitive text editor, a performance profiler, a project builder, a version control system, a run-time error checker, and a graphical source browser. Mercury extensions allow multiprocessor-aware process launching and debugging, as well as a System Supervisor view for graphical remote management.
- **Trace Analysis Tool and Library (TATL™)**
  This "logic analyzer for software" provides insight into the dynamic interaction of up to a few hundred processors.
- **VSIPL and SAL (Scientific Algorithm Library)**
  Support for these Mercury standard numeric libraries is optimized for the 8641D architecture of the HCD5220.
- **Interprocessor Communication System (ICS)**
  Support is carried forward from the RACE++®/MCOE™ software environment. ICS provides a low-level interprocessor communication API, enabling users to take advantage of the high-bandwidth, low-latency serial RapidIO fabric with an easy-to-use software interface.
- **Performance Porting Package**
  Provides low-level handles for manipulation of the serial RapidIO fabric and may be used for simple data movement or as a base to build a custom middleware layer.

With MultiCore Plus (MCP) software, applications can use industry-standard middleware such as MPI, DRI, CORBA, or even standard TCP/IP sockets ported to run seamlessly over the fabric. MCP also offers a software tool that can help to migrate legacy applications created with MCOE into the MCP domain.

Specifications

Module

Two dual-core MPC8641D processors
Two PMC/XMC sites
    XMC factory-selectable for PCI Express or serial RapidIO connectivity
Air-cooled
Input voltage 5V and 3.3V

Processor Node

Dual-core 8641D	Up to 1.33 GHz
Cores per device	2
DDR2 SDRAM	Up to 2 GB per processor at up to 533 MHz

PMC-X / XMC Sites

Two PMC-X sites
PCI-X-to-PCI Express bridge
    Connects PMC sites to onboard PCI Express switch
PCI support at 33 MHz and 66 MHz
PCI-X support

Primary site	66, 100, and 133 MHz
Secondary site	66 and 100 MHz

PMC user-defined I/O from P4 to VME P2
PCI Express XMC sites per VITA 42.3 or
    serial RapidIO XMC sites per VITA 42.2

VME Interface

2eSST capable via Tundra® TSi148™

I/O

Two front-panel 10/100/1000Base-TX Ethernet ports
Two backplane Gigabit Ethernet ports per VITA 41.6
RS-232 serial interfaces per processor to front-panel interface
Additional serial interface optionally routed to backplane

Additional Resources

Onboard 128-MB boot/application flash per processor
Real-time clock
Watchdog timer
General-purpose 32-bit timers/counters
System management block
Thermal and voltage sensors

Environmental

Air Cooled L0 Commercial

Temperature	
Operating	0°C to 40°C
Storage	-40°C to +85°C
Altitude	
Operating	10,000 ft
Storage	30,000 ft
Humidity	10-90% non-condensing
Vibration	$0.003g^2$/Hz, based on 20-2000 Hz, 1 hr/axis
Shock	z-axis: 20g; x-, y-axes: 32g; 11 ms half-sine; 3-positive and 3-negative on each axis

Air Cooled L1 Rugged

Temperature	
Operating	-25°C to +55°C
Storage	-55°C to +85°C
Altitude	
Operating	30,000 ft
Storage	50,000 ft
Humidity	5-95% non-condensing
Vibration	$0.04g^2$/Hz, based on 20-2000 Hz, 1 hr/axis
Shock	z-axis: 50g; x-, y-axes: 80g; 11 ms half-sine; 3-positive and 3-negative on each axis
*CFM	15 (at sea level)**
	20 (at 10,000ft)**

* As altitude increases, air density decreases and, therefore, the cooling effect of a particular number of CFM decreases. Different limits can be achieved by trading among temperature, altitude, frequency, and airflow. Consult factory for additional information.
** Does not include XMC/PMCs. Consult factory for HCD5220 configured with XMC/PMCs.

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INNOVATION THAT MATTERS™

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