Flexor 5983-320

2-channel 3.0 GHz A/D, 2-channel 2.8 GHz D/A 3U VPX board with Kintex UltraScale FPGA

Complete radar and software radio interface solution

- Radar and communication receiver and transmitter
- Electronic Warfare transponder
- Waveform signal generator
- Wideband data acquisition
- Remote monitoring
- Sensor interfaces

Model 5983 is a member of the Flexor® family of high-performance 3U VPX baseboards with a Xilinx Kintex UltraScale FPGA and an available FMC I/O slot. As an integrated solution, the Model 5983-320 FlexorSet® combines the Model 5983 and the Model 3320 Flexor® FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983's mounted in the same chassis or even over extended distances between them.

Note: There is a 5983A version of this product. See FlexorSet Models.

FEATURES

- Supports Xilinx® Kintex® UltraScale FPGA
- GateXpress® supports dynamic FPGA reconfiguration across PCIe
- Two 3.0 GHz A/Ds
- Two 2.8 GHz D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- LVDS connections to the Kintex UltraScale FPGA for custom I/O and synchronization
- Optional optical Interface for gigabit serial interboard communication
- Compatible with several VITA standards including: VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
- Navigator® BSP for software development
- Navigator® FDK for custom IP development
- Free lifetime applications support

THE FLEXOR ARCHITECTURE

Based on the proven design of the Mercury Jade family of Kintex products, the 5983 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5983-320 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include two A/D acquisition IP modules for simplifying data capture and data transfer.

The 5983-320 features a sophisticated D/A waveform generator IP module. A linked-list controller allows users to easily record to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-320 to operate as a turnkey solution without the need to develop any FPGA IP.

EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. The Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Mercury factory-installed functions or use the Navigator kit to completely replace the Navigator IP with their own.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-320 to operate as a turnkey solution without the need to develop any FPGA IP.

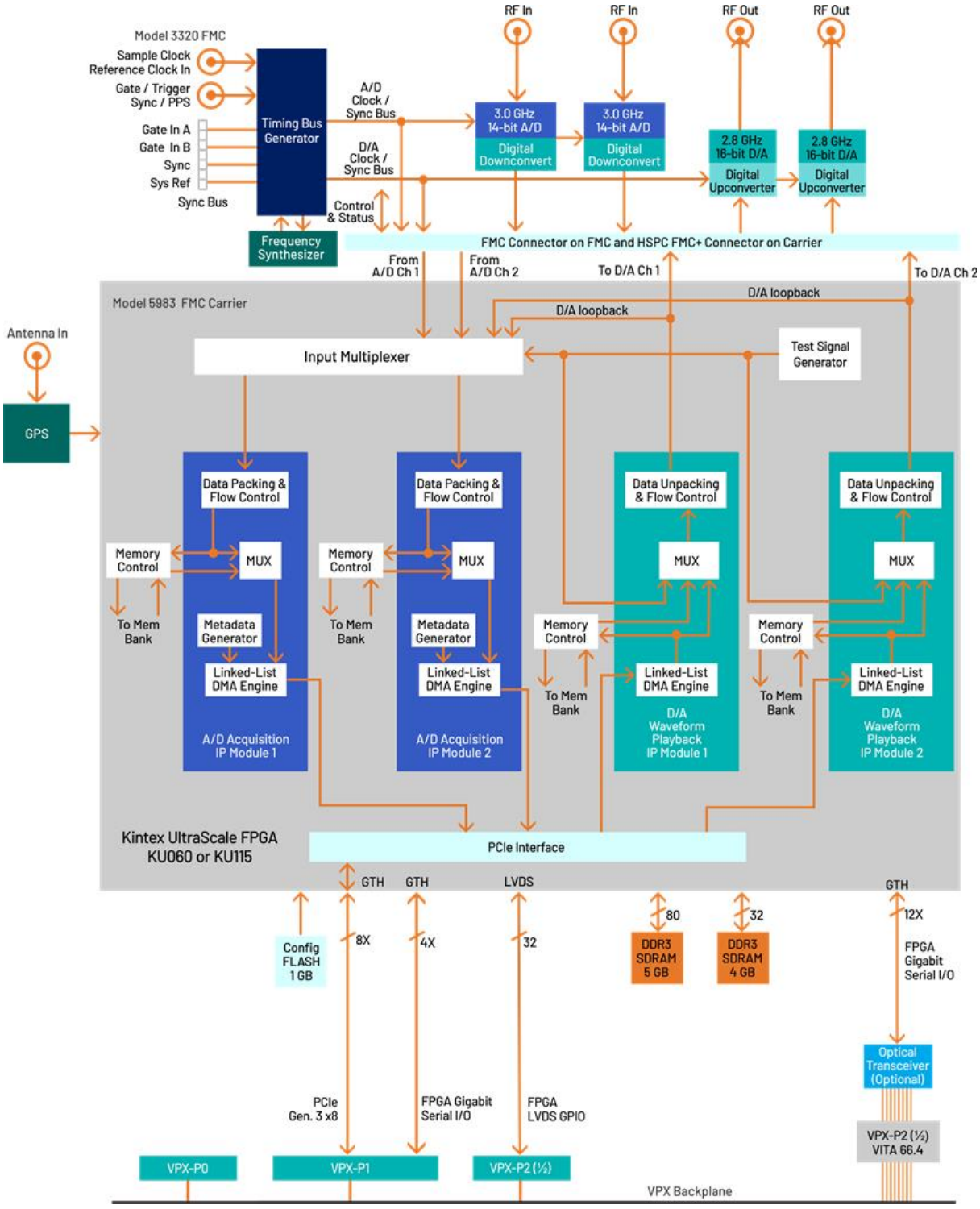
XILINX KINTEX ULTRASCALE FPGA

The 5983-320 can be optionally populated with one of two Kintex UltraScale FPGAs to match the specific requirements of the processing task. Supported FPGAs are KU060 or KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost KU060 can be installed.

Sixteen pairs of LVDS connections are optionally provided between the FPGA and the VPX P2 connector for custom I/O. For applications requiring custom gigabit links, a 4X connection is supported between the FPGA and the VPX P1 connector to support serial protocols.

5983-320 BLOCK DIAGRAM

Click on a block for more information.



A/D CONVERTER AND DIGITAL DOWNCONVERTER STAGE

The board's analog interface accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See "Preconfigured Conversion Modes" on page 9 for supported modes.

A/D ACQUISITION IP MODULES

The 5983-320 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the two A/Ds, a test signal generator or from the two D/A Waveform Generator IP modules in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A WAVEFORM GENERATOR IP MODULE

The 5983-320 factory-installed functions include two sophisticated D/A Waveform Generator IP modules. A linked-list controller allows users to easily record waveforms stored in either onboard or off-board host memory to the two D/As.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

CLOCKING AND SYNCHRONIZATION

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector.

This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.

MEMORY RESOURCES

The 5983-313 architecture supports two independent DDR3 SDRAM memory banks. The banks are four and five gigabytes each and are part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI EXPRESS INTERFACE

The Model 5983-320 includes an industry standard interface fully compliant with PCI Express Gen. 1, 2, and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

GPS

An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

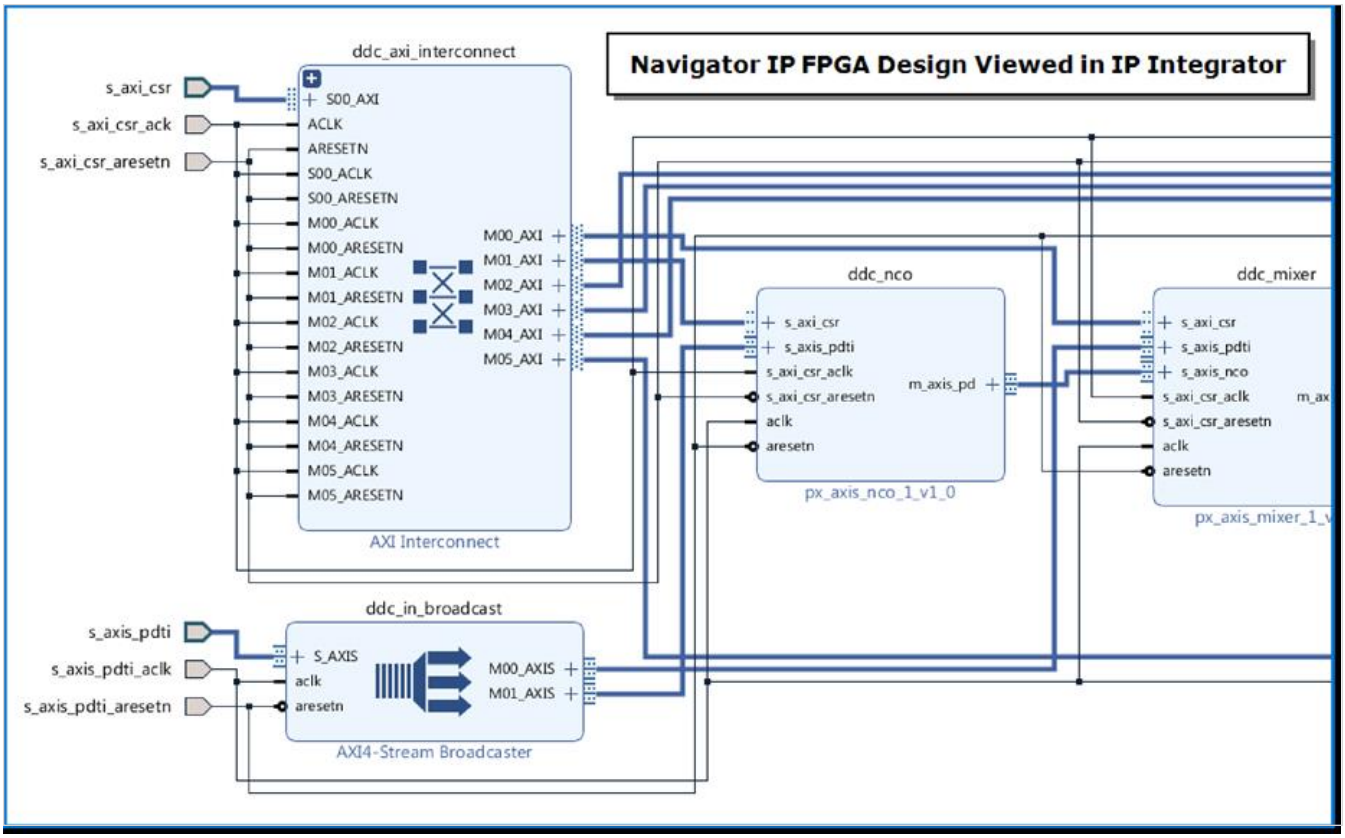
NAVIGATOR DESIGN SUITE

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into the factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

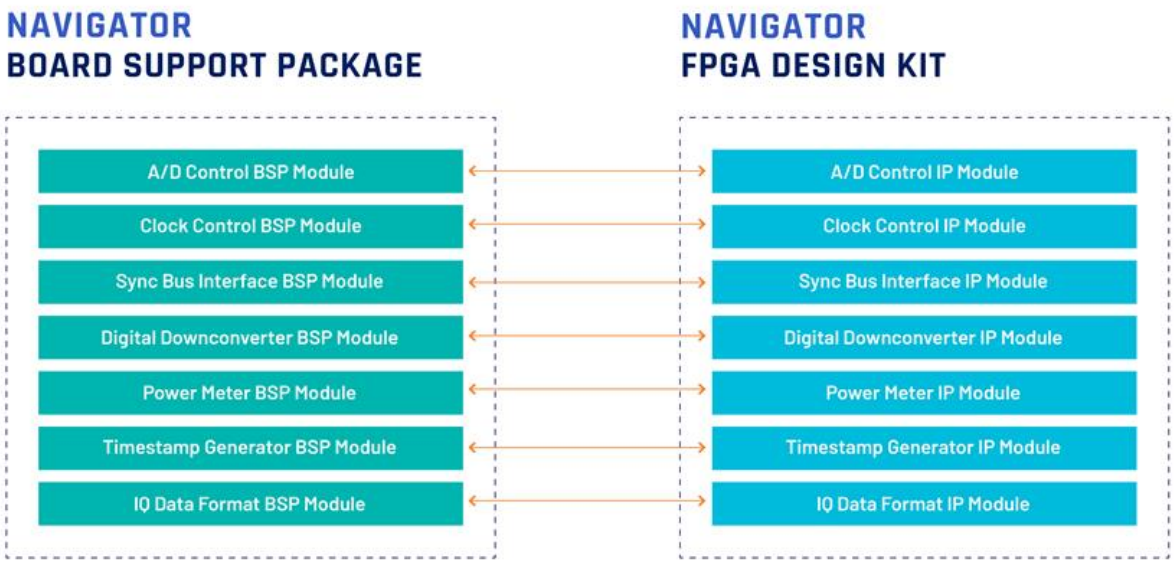
The Navigator FPGA Design Kit (FDK) for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Jade product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Jade design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations.

Navigator FDK includes an IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.

The **Navigator Board Support Package (BSP)** provides software support for Jade boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA. The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.

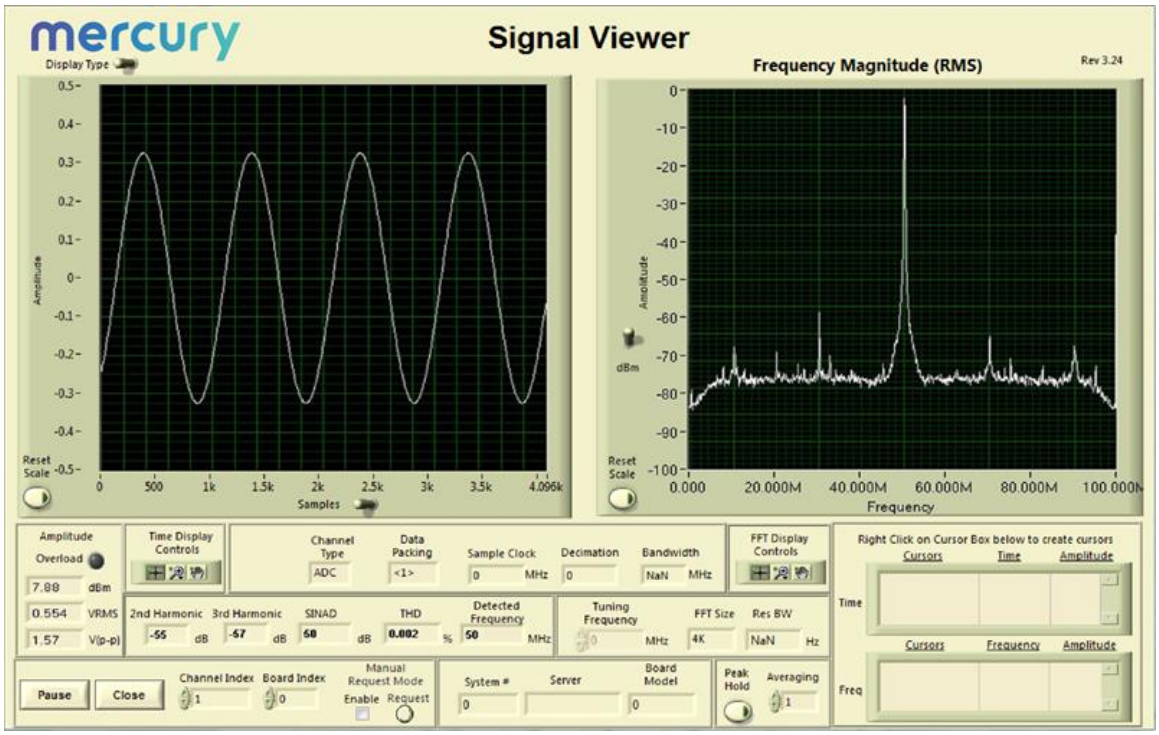


Navigator IP FPGA Design viewed in IP Integrator



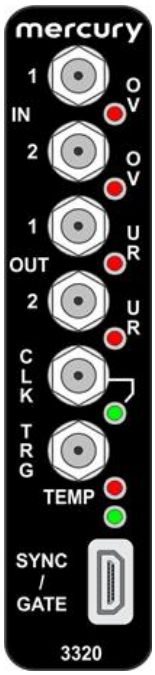
Because all Jade boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the **Signal Viewer**, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Jade board and Navigator BSP and start viewing analog signals immediately.



FRONT PANEL CONNECTIONS

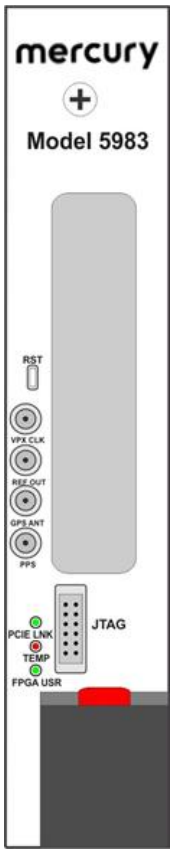
The FMC front panel includes six SSMC coaxial connectors, and a 19-pin µSync connector for input/output of timing and analog signals. The front panel also includes seven LEDs.



- **Analog Input Connectors:** Two SSMC coaxial connector, labeled **IN 1** and **2** one for each ADC input channel to the ADC32RF45.
- **ADC Overload LEDs:** The two red **OV** (overload) LEDs indicate either an overload in the associated ADC32RF45 or an ADC FIFO overrun.
- **Analog Output Connectors:** Two SSMC coaxial connectors, labeled **OUT 1** and **2** one for each ADC32RF45 output.
- **DAC Underrun LEDs:** There are two red **UR** underrun LEDs, one for each DAC output channel. The red underrun LED illuminates when the associated DAC5688 FIFO is out of data.
- **Clock Input Connector:** One SSMC connector, labeled **CLK** for the input of an external sample clock.
- **Clock LED:** The green **EXT CLK IN** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.
- **Trigger Input Connector:** One SSMC coaxial connector labeled **TRG** for input of an external trigger.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the PCB.
- **User LED:** The green unlabeled LED below the **TEMP** LED is for user applications.
- **Sync Bus Connector:** The 19-pin Sync Bus front panel connectors labeled **SYNC/GATE** provides sync and gate input signals for the Sync Bus.

FRONT PANEL CONNECTIONS

The 5983 3U VPX carrier front panel houses the front panel of the FMC installed on the carrier. The carrier front panel includes a reset button, two or four MMCX coaxial connectors, a JTAG connector, and three LED indicators



- **Reset Button:** The white reset button, labeled **RST**, provides a reset and safe reboot of the onboard GPS receiver (Option 180).
- **VPX Clock Connector:** The MMCX connector labeled **VPX CLK** provides output of the 100-MHz PCI clock from the VPX P0 connector (see VPX P0 Utility Connector).
- **10 MHz Reference Connector:** With Option 180, the MMCX connector labeled **REF OUT** provides output of the 10-MHz PCI clock from the onboard GPS receiver.
- **GPS Antenna Connector:** With Option 180, the front panel has one MMCX connector, labeled **GPS ANT**, for input of an antenna RF signal for the onboard GPS receiver. The antenna input signal has a sensitivity of +2 dBm to -167 dBm into 50W input impedance.
- **PPS Connector:** The MMCX connector labeled **PPS** provides output of a PPS signal that can be derived from the onboard GPS receiver (Option 180).
- **PCIe Link LED:** The green **PCIE** LNK LED illuminates when a valid PCIe link has been established over the VPX interface.
- **JTAG Connector:** The carrier front panel provides a 12-pin JTAG connector to download programs and to perform boundary-scan tests on the devices.
- **Over Temperature LED:** The red **TEMP** LED illuminates when an over-temperature or over-voltage condition is indicated by the temperature/voltage sensors.
- **User LED:** The yellow **FPGA USR** LED is available for user applications.

Note: If your 5983 is ordered with Option 763 for mounting in a conduction-cooled VPX chassis, it would have a conduction-cooled VPX Carrier Front Panel.

SPECIFICATIONS

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel SSMC connectors

Transformer Type: Mini-Circuits TC1-1-13M

Full Scale Input: +6.6 dBm into 50 ohms

3 dB Passband: 4.5 to 3000 MHz

A/D Converters

Type: Texas Instruments ADC32RF45

Sampling Rate: See the 3320 Preconfigured Conversion Modes table.

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel SSMC connectors

Transformer Type: Coil Craft WBC4-14L

Full-Scale Output: +4 dBm into 50 ohms

3 dB Passband: 1.5 MHz to 1200 MHz D

D/A Converters

Type: Texas Instruments DAC39J84

Sampling Rate and Resolution: See 3320 Preconfigured Conversion Modes table

Sample Clock Sources

Timing bus generator provides A/D and D/A clocks

Timing Bus Generator

Clock Source: Selectable from on-board frequency synthesizer or front panel external clock

Synchronization: Frequency synthesizer can be locked to an external 10 MHz PLL system reference

External Clock

Type: Front panel SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

External Trigger Input

Type: Front panel SSMC connector

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- Standard: Xilinx Kintex UltraScale XCKU060-2
- Optional: Xilinx Kintex UltraScale XCKU115-2

Custom FPGA I/O

4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Parallel: 16 pairs of LVDS connections are provided between the FPGA and the VPX P2 connector for custom I/O

Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory

Type: DDR3 SDRAM

Size: Two banks, one 4 GB and one 5 GB

Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50 n ° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

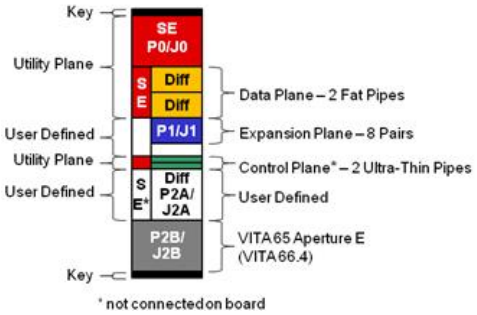
Physical

Dimensions: 3U VPX

- Depth: 100 mm (3.937 in)
- Height: 170.6 mm (6.717 in)

Open VPX Compatibility

The Model 5983-320 is compatible with the following module profile, as defined by the VITA 65 Open-VPX Specification: SLT3-PAY-2F1F2U1E-14.6.6-1.



PRECONFIGURED CONVERSION MODES

When the Model 3320 is part of a FlexorSet, it is delivered with a set of six preconfigured modes. These allow users to easily select A/D and D/A settings that are commonly used in many applications. While these modes typically satisfy many applications, users can always configure the A/D and D/A settings to their specific requirements via the PCIe interface using the ReadyFlow Board Support Package.

A/D CONVERTER

mode	sample rate	DDC or bypass	output bits resolution	output bandwidth	real or complex	output data rate/chan	usable bandwidth
1	3.0 GHz	dec = 4	16 I + 16 Q	600 MHz	complex	3.0 GB/sec	600 MHz
2	2.8 GHz	dec = 4	16 I + 16 Q	560 MHz	complex	2.8 GB/sec	560 MHz
3	2.8 GHz	dec = 4	16 I + 16 Q	560 MHz	complex	2.8 GB/sec	560 MHz
4	2.5 GHz	bypass	12	2.5 GHz	real	5.0 GB/sec	1000 MHz
5	2.0 GHz	bypass	14	2.0 GHz	real	4.0 GB/sec	800 MHz
6	2.0 GHz	bypass	14	2.0 GHz	real	4.0 GB/sec	800 MHz

D/A CONVERTER

mode	sample rate	DDC or bypass	input bits resolution	real or complex	output data rate/chan	usable bandwidth
1	-	-	-	-	-	-
2	2.8 GHz	int = 2	16 I + 16 Q	complex	5.6 GB/sec	1120 MHz
3	2.8 GHz	int = 4	16 I + 16 Q	complex	2.8 GB/sec	560 MHz
4	-	-	-	-	-	-
5	2.0 GHz	int = 2	16 I + 16 Q	complex	4.0 GB/sec	800 MHz
6	2.0 GHz	int = 2	16	real	2.0 GB/sec	400 MHz

RATIONALE FOR EACH MODE

- Mode 1: Maximum A/D sample rate of 3 GS/s, but the DDC must be used. D/A cannot operate at this sample rate.
- Mode 2: Maximum sample rate for A/D and D/A both operating. DDC and DUC must be used, but D/A can generate twice the bandwidth of the A/D bandwidth.
- Mode 3: Maximum sample rate for A/D and D/A both operating (like Mode 2), but now A/D and D/A bandwidths are the same.
- Mode 4: Maximum A/D useable bandwidth achieved with DDC bypass (RAW) output data and 12 bit resolution. D/A cannot operate in this mode.
- Mode 5: Maximum useable signal bandwidth with A/D and D/A both operating. A/D is in bypass with 14-bit resolution. D/A uses DUC with interpolation of 2.
- Mode 6. Like Mode 5 except D/A interpolates real samples instead of complex samples resulting in 400 MHz bandwidth and a simpler output anti-aliasing filter.

GENERAL NOTES

1. “Useable bandwidth” is equal to 80% of the Nyquist bandwidth.
2. Anti-aliasing filters are required for A/D inputs and D/A outputs to ensure elimination of unwanted out-of-band signals per Nyquist criteria.
3. Data rates shown are for the interfaces between the FMC module and the FPGA of the FMC carrier for each channel.
4. By changing board-support software, other operating modes are possible, including different decimations and interpolation.
5. The sample rates shown for each mode are the maximum rates for that mode, but lower rates are also supported with other parameters scaled appropriately.
6. Only one mode is allowed at a time, which defines operations for both A/D and D/A.

FLEXORSET MODELS

This chart shows all available FlexorSets. Click on model numbers for more information.

Form Factor	Software/FPGA Tools	Carrier Model	FMC Model	FlexorSet Model	Description
3U VPX	Virtex-7 ReadyFlow BSP GateFlow FDK Vivado	5973	3312	5973-312	4-Channel 250 MHz A/D & 2-Channel 800 MHz D/A
				5973-313	4-Channel 250 MHz A/D & 2-Channel 800 MHz D/A with 4 multiband DDCs & interpolation filters
			3316	5973-316	8-Channel 250 MHz 16-bit A/D
				5973-317	8-Channel 250 MHz 16-bit A/D with 8 multiband DDCs
			3320	5973-320	2-Channel 3 GHz A/D & 2-Channel 2.8 GHz D/A
			3324	5973-324	4-Channel 500 MHz A/D & 4-Channel 2 GHz D/A
	KintexUltraScale Navigator BSP Navigator FDK Vivado	5983*	3312	5983-313*	4-Channel 250 MHz A/D & 2-Channel 800 MHz D/A with 4 multiband DDCs & interpolation filters
			3316	5983-317*	8-Channel 250 MHz 16-bit A/D with 8 multiband DDCs
			3320	5983-320*	2-Channel 3 GHz A/D & 2-Channel 2.8 GHz D/A
			3324	5983-324*	4-Channel 500 MHz A/D & 4-Channel 2 GHz D/A
PCIe	Virtex-7 ReadyFlow BSP GateFlow FDK Vivado	7070	3312	7070-312	4-Channel 250 MHz A/D & 2-Channel 800 MHz D/A
				7070-313	4-Channel 250 MHz A/D & 2-Channel 800 MHz D/A with 4 multiband DDCs & interpolation filters
			3316	7070-316	8-Channel 250 MHz 16-bit A/D
				7070-317	8-Channel 250 MHz 16-bit A/D with 8 multiband DDCs
			3320	7070-320	2-Channel 3 GHz A/D & 2-Channel 2.8 GHz D/A
			3324	7070-324	4-Channel 500 MHz A/D & 4-Channel 2 GHz D/A

*Consult with Mercury about the availability of a 5983A version of this product. For differences, see below.

Model 5983	Model 5983A
Flash Memory - 1 Gbit of FLASH Memory	**Flash Memory -**2 Gbit of BPI FLASH Memory
Optical I/O (Option 110) - VITA 66.4 - Up to 12 duplex optical lanes are available on a VITA 66.4 connector. With the installation of a serial protocol, the VITA 66.4 interface enables a high-bandwidth connection between 5983s mounted in the same chassis or over extended distances.	**Optical I/O (Option 110) - VITA 67.3D -** Provides 12 duplex lanes @ 10 Gb/sec through the lower half of VPX P2 (VPX P2B). With the installation of a serial protocol, the VITA 67.3D interface enables gigabit communications between boards and chassis, independent of the PCIe interface. Consult with Mercury before ordering Option 110 (optical).
	Custom Analog I/O (Option 113) - VITA 67.3 - VITA 67.3 provides 10 coax connections through the lower half of VPX P2.

ORDERING INFORMATION

Model	Description
5983-320	2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 FPGA - 3U VPX

Options:	
-087	XCKU115-2 FPGA
-110	VITA-66.4 12X optical interface
-180	GPS Support
-702	Air-cooled, Level 2
-763	Conduction-cooled, Level 3

Contact Mercury for compatible option combinations and complete specifications of rugged and conduction-cooled versions. Options may change, so be sure to contact Mercury for the latest information.

DEVELOPMENT SYSTEMS

Mercury offers development systems for Flexor products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Flexor boards. Please contact Mercury to configure a system that matches your requirements.

ACCESSORY PRODUCTS

Model	Description
2171	Cable kit: SSMC to SMA
5292	High-speed synchronizer and distribution board - 3U VPX model
9192	Rackmount high-speed system synchronizer unit

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Learn more

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For technical details, contact:
mrcy.com/CF5983-320