Quartz 6350

8-channel A/D & D/A in a rugged small form factor enclosure with Xilinx Zynq UltraScale+ RFSoC – Gen 1

Ideal for deployment in harsh environments

- High-bandwidth data streaming
- Waveform signal generator
- Communication receiver and transmitter
- Electronic Warfare transponder
- Analog I/O for digital recording and playback
- Sensor interfaces

The Quartz® 6350 is a high-performance, small form factor system based on the Xilinx Zynq UltraScale+ RFSoC. The RFSoC integrates eight RF-class A/D and D/A converters into the Zynq's multiprocessor architecture, creating a multichannel data conversion and processing solution on a single chip.

The 6350 delivers RFSoC performance in small footprint with a complete system in a ruggedized enclosure ideal for deployment in harsh environments. Complementing the RFSoC's on-chip resources are the 6350's sophisticated clocking section, a low-noise front end for RF input and output, 16 GBytes of DDR4, a gigabit serial optical interface capable of supporting dual 100 GigE connections, an optional GPS receiver, and general purpose I/O signal paths to the FPGA.

ARCHITECTURE

The 6350 design places the RFSoC as the cornerstone of the architecture. All control and data paths are accessible by the RFSoC's programmable logic and processing system. A full suite of Mercury-developed IP and software functions utilize this architecture to provide data capture, processing and waveform generating solutions for many of the most common application requirements.

FEATURES

- Small form factor rugged enclosure
- Conduction-cooled
- Designed to the IP67 specification for dust and water immersion
- Sealed military-grade circular connectors
- Incorporates Xilinx® Zynq® UltraScale+™ RFSoC
- 16 GB of DDR4 SDRAM
- On-board GPS receiver
- Optional dual 100 GigE UDP optical interface
- Optional fan cooling for benchtop use
- Navigator® BSP for software development
- Navigator® FDK for custom IP development

DESIGNED FOR HARSH ENVIRONMENTS

The Model 6350 delivers the signal and processing performance of the Quartz RFSoC family in a Small Form Factor (SFF) rugged package. Optimized for SWaP (size, weight and power), the 6350 measures 3.53" H 5.65" W 9.57" D and weighs in at just under 8 pounds.

Designed for use in rugged environments, the 6350 is designed to the IP67 specification for dust and water immersion. It's internal 'I-beam' construction creates a chassis that is both extremely rugged and efficient for moving heat out of the box, making it ideal for deployment in the harshest environments and well matched to conduction-cooled installations. The 6350 can also be used with an optional fan plate for desktop development.

EXTENDABLE IP DESIGN

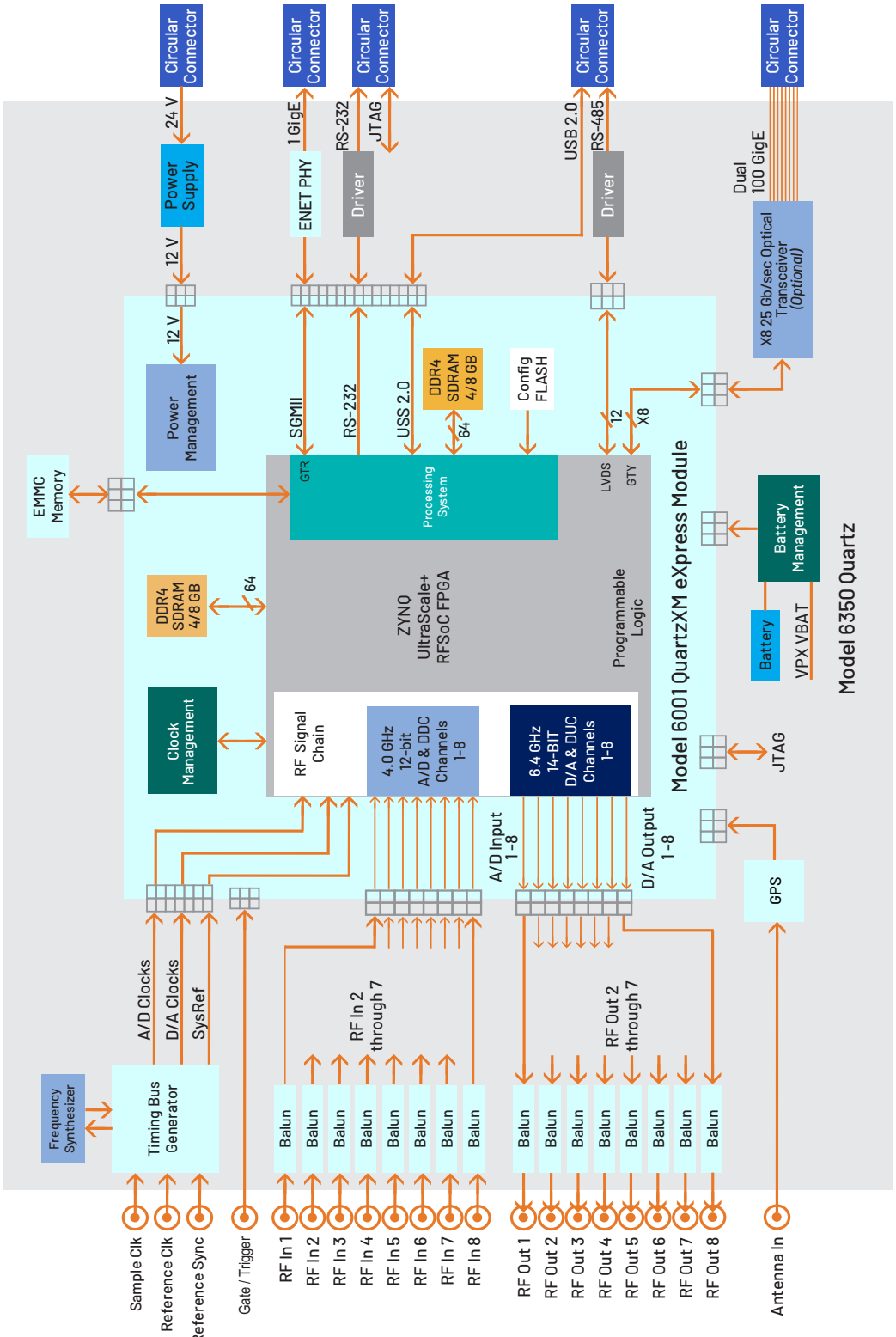
For applications that require specialized functions, users can install their own custom IP for data processing. Mercury's Navigator FPGA Design Kit (FDK) includes the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado® IP Integrator. In addition to the IP Integrator block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the factory-installed functions or use the Navigator kit to completely replace the Mercury IP with their own.

The Navigator Board Support Package (BSP), the companion product to the Navigator FDK, provides a complete C-callable library for control of the 6350's hardware and IP. The Navigator FDK and BSP libraries mirror each other where each IP function is controlled by a matching software function, simplifying the job of keeping IP and software development synchronized.

The Navigator BSP includes support for Xilinx's PetaLinux running on the ARM Cortex-A53 processors. When running under PetaLinux, the Navigator BSP libraries enable complete control of the 6350 either from applications running locally or on the ARMs, or using the Navigator API control and command from remote system computers.

6350 BLOCK DIAGRAM

Click on a block for more information.



A/D CONVERTER STAGE

The 6350 accepts analog IF or RF inputs on eight front panel coax connectors. These inputs are transformer-coupling into the RF signal chain of the RFSoC. Inside the RFSoC, the analog signals are routed to eight 4 GSPS, 12-bit A/D converters. Each converter has built-in digital downconverters with programmable 1x, 2x, 4x or 8x decimation and independent tuning. The A/D digital outputs are delivered into the Zynq's programmable logic and processor system for signal processing, data capture or for routing to other resources.

In addition to the A/D's built-in decimation, an additional stage of IP-based decimation provides another 16x stage of data reduction, ideal for applications that need to stream data from all eight A/Ds.

D/A CONVERTER STAGE

The RFSoC's eight D/A converters accept baseband real or complex data streams from the FPGA's programmable logic. Each 6.4 GSPS, 14-bit D/A includes a digital upconverter with independent tuning and interpolations of 1x, 2x, 4x and 8x. Each D/A output is transformer-coupled to a coax connection located on the front panel.

CLOCKING AND SYNCHRONIZATION

An on-board timing bus generator uses a programmable frequency synthesizer to generate the sample clock and all required timing signals. The on-board sample clock can also be locked to a reference clock received through a front panel coax connector. A multifunction gate/trigger input is also available on the front panel for external control of data acquisition and playback.

MEMORY RESOURCES

The 6350 architecture supports 8 GBytes of DDR4 SDRAM memory accessible from the Programmable Logic. User-installed IP, which, along with the Mercury-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications. An additional 8 GBytes bank of DDR4 SDRAM is available to the Processing System as program memory and storage.

100 GIGE INTERFACE

The Model 6350 supports eight 25 Gb/sec full duplex optical lanes to a miniature rugged circular connector. With the dual built-in 100 GigE UDP interfaces or installation of a user provided serial protocol, this optical interface enables a high-speed gigabit data streaming path between the box and data storage or processing subsystems.

GPS

A GPS receiver provides time and position information to the FPGA and ARM processors. This information can be used for precise data tagging. The GPS provides a 1 PPS and 10 MHz reference clock to the FPGA.

OPTIMIZED IP

Xilinx has created an integrated processing solution in the RFSoC that is unprecedented. The key to unlocking the potential of the RFSoC is efficient operation using optimized IP and application software. Mercury helps streamline the process from development to deployed application by providing a full suite of built-in functions. These address the data flow and basic processing needed for some of the most common applications.

Several example applications using the Model 6350 are described below. For each example, the board's included IP is all that is needed to demonstrate the application and may satisfy the full set of requirements for any particular application. These applications can also be the starting point for adding additional IP from the Navigator IP library or for adding custom IP.

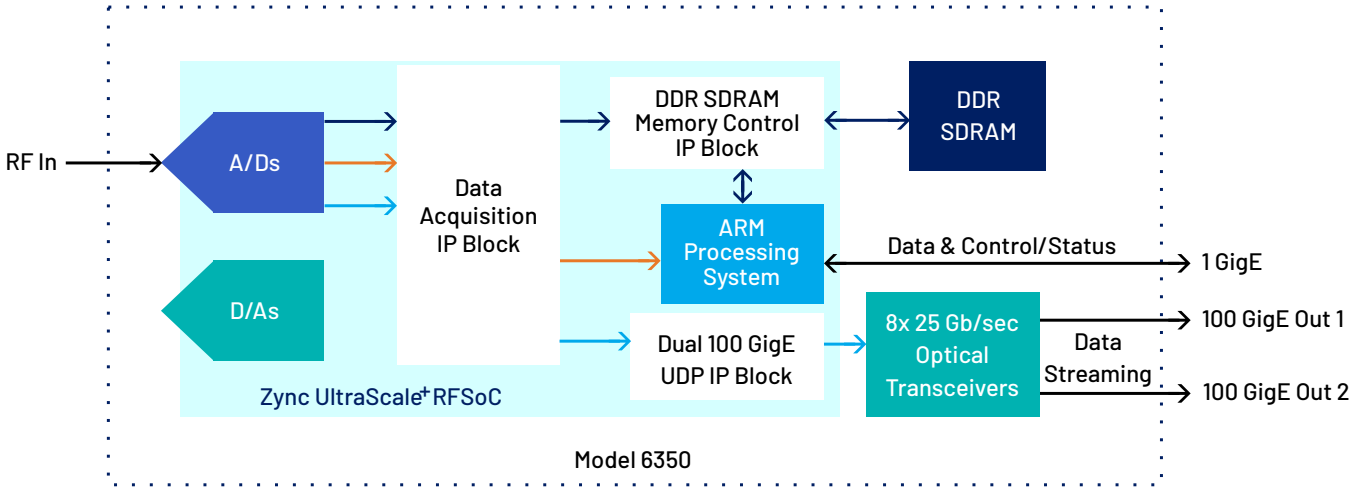
EXAMPLE 1 - HIGH BANDWIDTH DATA STREAMING

The RFSoC's eight 4 GSPS A/Ds are capable of producing an aggregate data rate of 64 GB/sec when all channels are enabled.

While capturing this much raw data is not feasible, the A/Ds' built-in digital down converters can reduce this data throughput in many applications to a rate reasonable for the data streaming and storage components downstream in the system.

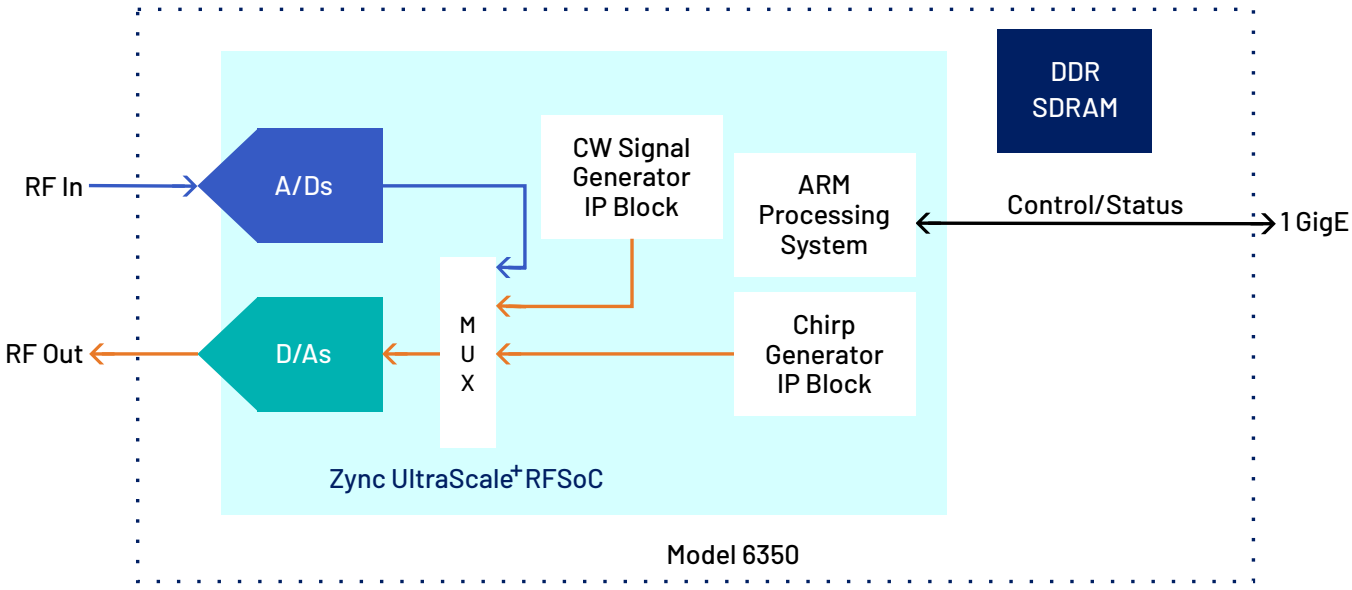
In some applications capturing the raw, full bandwidth data is crucial. The 6350's dual 100 GigE UDP engine provides a high bandwidth path for moving data off of the board (shown with light blue arrows). Along with the built-in data acquisition IP, the 6350 can stream two full bandwidth A/D data streams over optical cable to a downstream storage or processing subsystem.

The 6350's built-in IP functions also provide paths for capturing data in the DDR4 SDRAM memory for retrieval by the ARM processing system or the FPGA programmable logic (shown with dark blue arrows) and for sending data over the ARM's 1 GigE interface (shown in yellow arrows).



EXAMPLE 2 - ANALOG LOOPBACK AND WAVEFORM GENERATOR

The 6350's IP supports multiple D/A signal source options. A simple loopback path allows samples received by the A/Ds to be output through the D/As (shown with a dark blue arrow) . A CW signal generator produces a sine output with programmable frequency (shown with a yellow arrow). A chirp generator, ideal for radar applications, outputs sweep signals with programmable frequency, ramp, phase offset, gain offset and length (shown with a light blue arrow). The generators also include flexible trigger options with both internal and external triggering.



CONNECTIONS

The front panel of Model 6350 has the following connectors:

- Eight SMA connectors labeled **IN 1-8**, which provide **A/D input** to the A/D converters on the 6350.
- Eight SMA connectors labeled **OUT 1-8**, which provide **D/A output** from the D/A converters on the 6350.

Quartz 6350 Front Panel

The rear panel of Model 6350 has the following connectors:

- **GATE:** Provides a trigger input. This trigger input is DC-coupled and compatible with the LVTTL levels, but is 5V tolerant.
- **REF:** Provides an input for an external 10 MHz reference. This signal can be used to lock the on-board sample clock synthesizer to an external reference.
- **USB 2.0 / RS485:** Interfaces to the RFSoC processor's USB 2.0 Port 0.
- **1000 BASE-T:** Provides an Ethernet connection to the 6350 at 1000 Base-T mode.
- **JTAG / RS-232:** Used to download to the FPGA and program QSPI configuration memory.
- **24V DC IN:** Provides power to the 6350.
- **2 x 100GbE:** Provides an optical connector for the 6350.
- **GPS:** For input of an antenna RF signal for the onboard GPS receiver.

Quartz 6350 Rear Panel

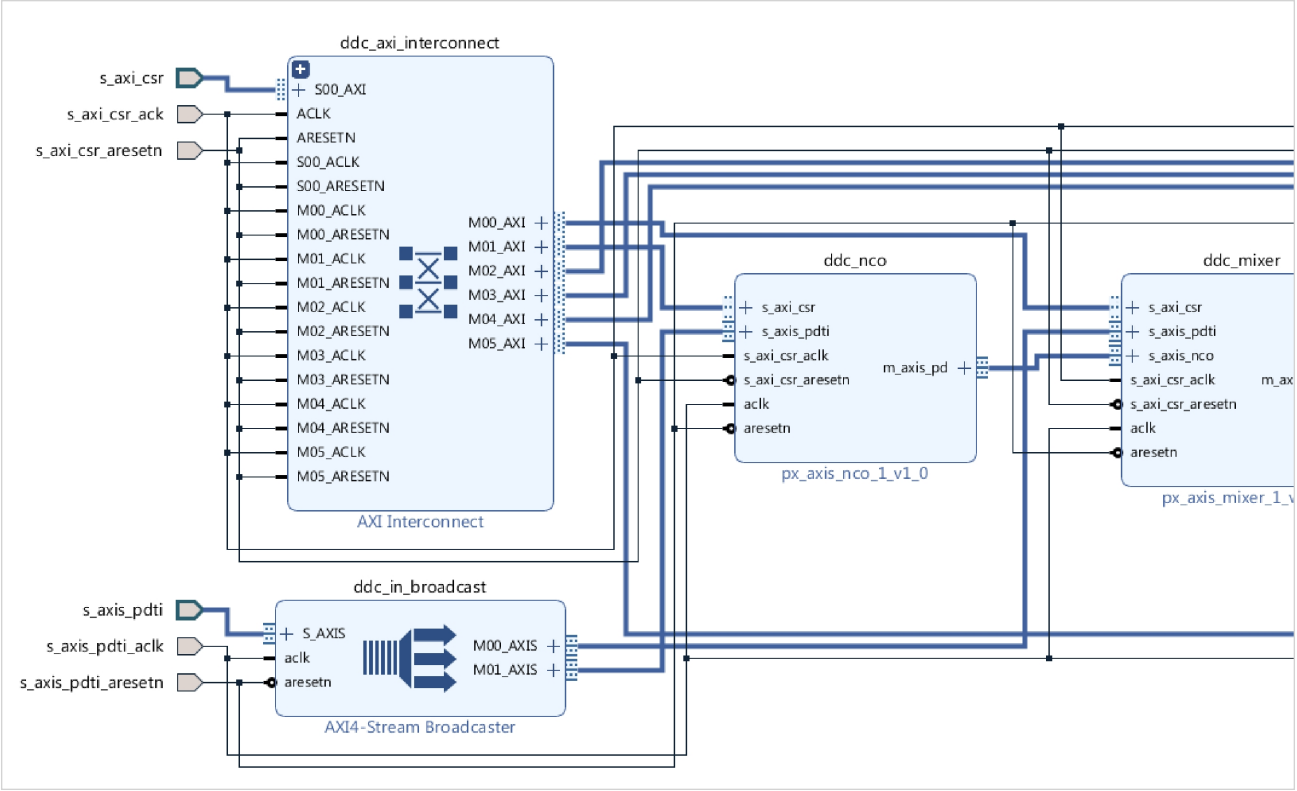
NAVIGATOR DESIGN SUITE

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into the factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

The Navigator FPGA Design Kit (FDK) for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Jade product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Jade design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations.

Navigator FDK includes an IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.

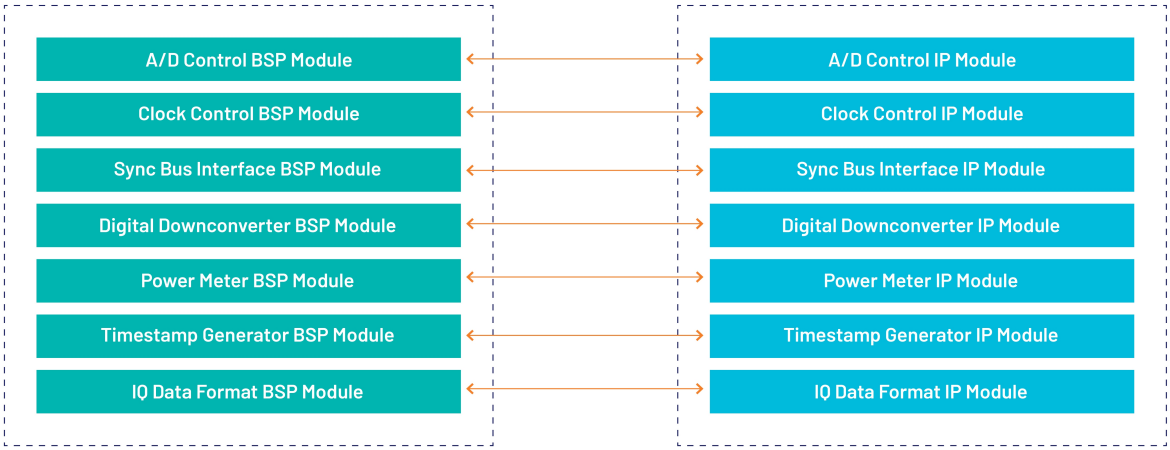
The **Navigator Board Support Package (BSP)** provides software support for Jade boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA. The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.



Navigator IP FPGA Design viewed in IP Integrator

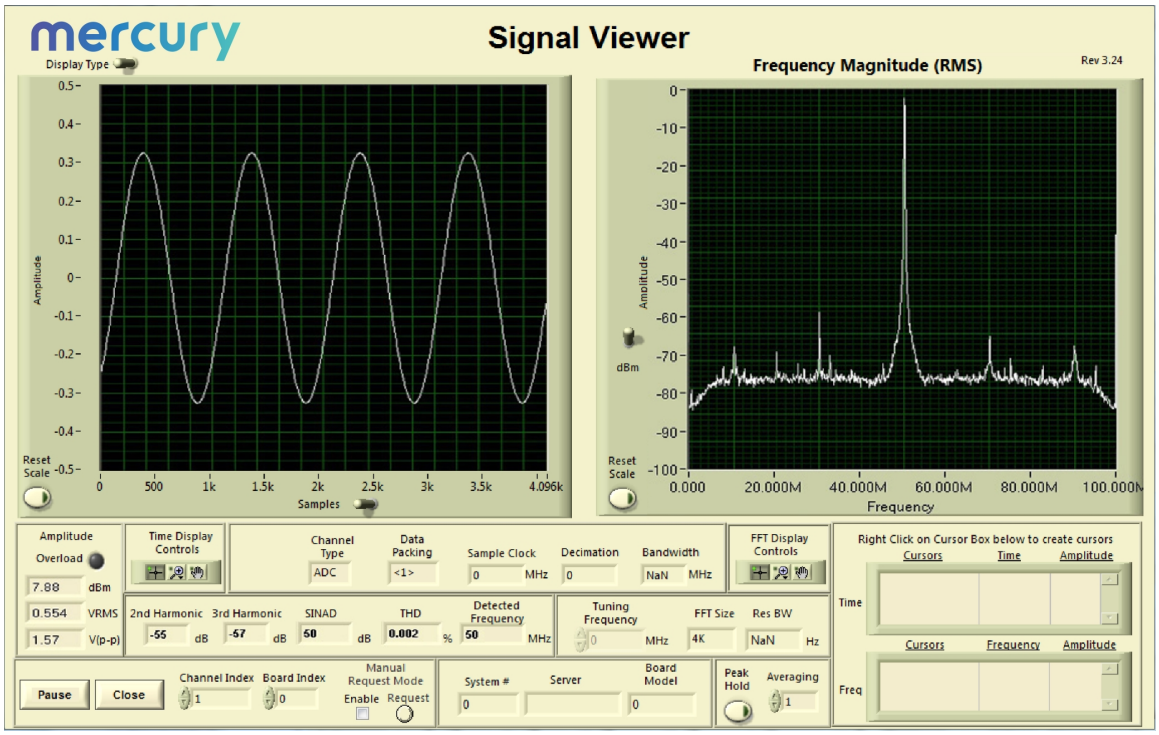
NAVIGATOR BOARD SUPPORT PACKAGE

NAVIGATOR FPGA DESIGN KIT



Because all Jade boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the **Signal Viewer**, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Jade board and Navigator BSP and start viewing analog signals immediately.



SPECIFICATIONS

Field Programmable Gate Array

Type: (standard) Xilinx Zynq UltraScale+ RFSoC XCZU27DR

- Option -028: Xilinx Zynq UltraScale+ RFSoC XCZU28DR

Speed: (standard) -1 speed grade

- Option -002: -2 speed grade

RFSoC RF Signal Chain

Analog Inputs

- Quantity: 8
- Location: Front panel (IN 1-8)
- Connector Type: SMA
- Input Type: Transformer-coupled
- Transformer Type: Mini-Circuits TCM1-83X+
- Full Scale Input: +10 dBm into 50 ohms
- 3 dB Passband: 10 MHz to 3700 MHz

A/D Converters

- Quantity: 8
- Sampling Rate: 4.0 GHz
- Resolution: 12 bits

Digital Downconverters

- Quantity: 1 per A/D
- Decimation Range: 1x, 2x, 4x, and 8x
- LO Tuning Freq. Resolution: 48 bits, 0 to f_s
- Filter: 80% pass band, 89 dB stop-band attenuation

Analog Outputs

- Quantity: 8
- Location: Front panel (OUT 1-8)
- Connector Type: SMA
- Output Type: Transformer-coupled
- Transformer Type: Mini-Circuits TCM1-83X+
- Full Scale Output: 0 dBm into 50 ohms
- 3 dB Passband: 10 MHz to 3700 MHz

D/A Converters

- Quantity: 8
- Sampling Rate: 6.4 GHz
- Resolution: 14 bits

Digital Upconverters

- Quantity: 1 per D/A
- Interpolation Range: 1x, 2x, 4x, and 8x
- LO Tuning Freq. Resolution: 48 bits
- Filter: 80% pass band, 89 dB stop-band attenuation

Sample Clock

- Source: On-board programmable clock

Reference Clock

- Source: On-board oscillator, on-board GPS, or external source
- External Source Location: Rear panel (REF)
- Connector Type: SMA
- Level: -10 dBm to +24 dBm

Gate/Trigger

- Source: Programmable through software or external connector
- External Source Location: Rear Panel (GATE)
- Connector Type: SMA
- Level: TTL

GPS

Source: On-board

Antenna Connector Location: Rear panel (GPS)

Connector Type: SMA

RFSoC Processing System

ARM Cortex-A53:

- Quantity: 4
- Speed: 1.5 GHz

ARM Cortex-R5:

- Quantity: 2
- Speed: 600 MHz

Processor I/O:

Interfaces: USB 2.0 and RS-485

- Location: Rear panel (USB2.0/RS485)
- Connector Type: Circular, Glenair Mighty Mouse Series

Interface: 1 GigE

- Location: Rear Panel (1000BASE-T)
- Connector Type: Circular, Glenair Mighty Mouse Series

Interface: RS-232

- Location: Rear Panel (JTAG/RS-232)
- Connector Type: Circular, Glenair Mighty Mouse Series

FPGA I/O

Optical (Option -110): 8X full duplex optical lanes @ 25 Gb/sec

- Location: Rear panel (2x 100GbE)
- Connector Type: circular, Glenair SuperNine Series
- Protocol: Factory-installed dual 100 GigE UDP IP cores provides greater than 24 GB/sec data transfers, other protocols supported with user-installed IP

JTAG

Location: Rear Panel (JTAG/RS-232)

Connector Type: Circular, Glenair Mighty Mouse Series

Memory

Processing System:

- Type: DDR4 SDRAM
- Size: (standard) 4 GB
  - Option -151: 8 GB
- Speed: 1200 MHz (2400 MHz DDR)
- Type: eMMC
- Size: 64 GB

Programmable Logic:

- Type: DDR4 SDRAM
- Size: (standard) 4 GB
  - Option -151: 8 GB
  - Speed: 1200 MHz (2400 MHz DDR)

FPGA Configuration FLASH:

- Type: QSPI NOR Flash
- Size: 2x 1 Gb

Environmental

Option -703: Level L3 (conduction-cooled)

- Operating Temp: -20° to 60° C (with 50° C cold plate)
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 100%

Physical

Dimensions:

- Depth: 243.08 mm (9.57 in)
- Height: 89.66 mm (3.53 in)
- Width: 143.51 mm (5.65 in)

Weight: 8 lbs.

Power:

Voltage: +12 to +28 VDC (+24 VDC nominal)

Location: Rear Panel (24VDC IN)

Connector Type: Circular, Glenair Mighty Mouse Series

Maximum Power Consumption: 46.62 Watts

ORDERING INFORMATION

Model	Description
6350	8-channel A/D & D/A in a rugged small form factor enclosure with Zynq UltraScale+ RFSoC Processor - Gen 1

Options	Description
-002	-2 FPGA speed grade, -1 standard
-028	XCZU28DR FPGA (XCZU27DR is standard)
-110	MPO 8X optical interface
-151	8GB processor system memory, 8 GB programmable logic memory
-703	Air-cooled, Level L3

Contact Mercury for compatible option combinations.

ACCESSORY PRODUCTS

Model	Description
2187	6350 Accessories

Option	Description
-150	Development cable set without optical cable
-151	Development cable set with optical cable
-701	Top cover plate with built-in fan, replaces standard top plate for benchtop cooling

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