

Jade 57841/58841

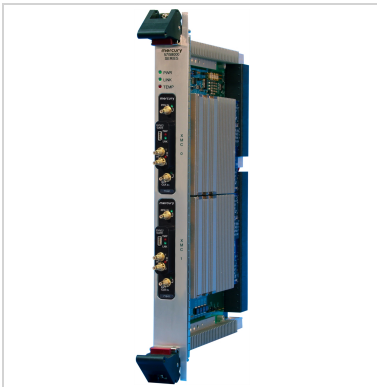
1- or 2-channel 3.6 GHz A/D,

2- or 4-channel 1.8 GHz A/D

6U VPX boards with Kintex UltraScale FPGA

Complete radar and software radio interface solution

- Radar and software radio receiver
- Communications receiver
- Analog signal interface for data recording
- Wideband data acquisition
- Remote monitoring
- Sensor interfaces



These models consist of one or two Jade® 71841 XMC modules mounted on a VPX carrier board. The 57841 is a 6U board with one 71841 module while the 58841 is a 6U board with two XMC modules.

They include four or eight A/Ds, complete multiboard clock and sync sections, and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the FPGA for custom digital I/O.

XILINX KINTEX ULTRASCALE FPGAS

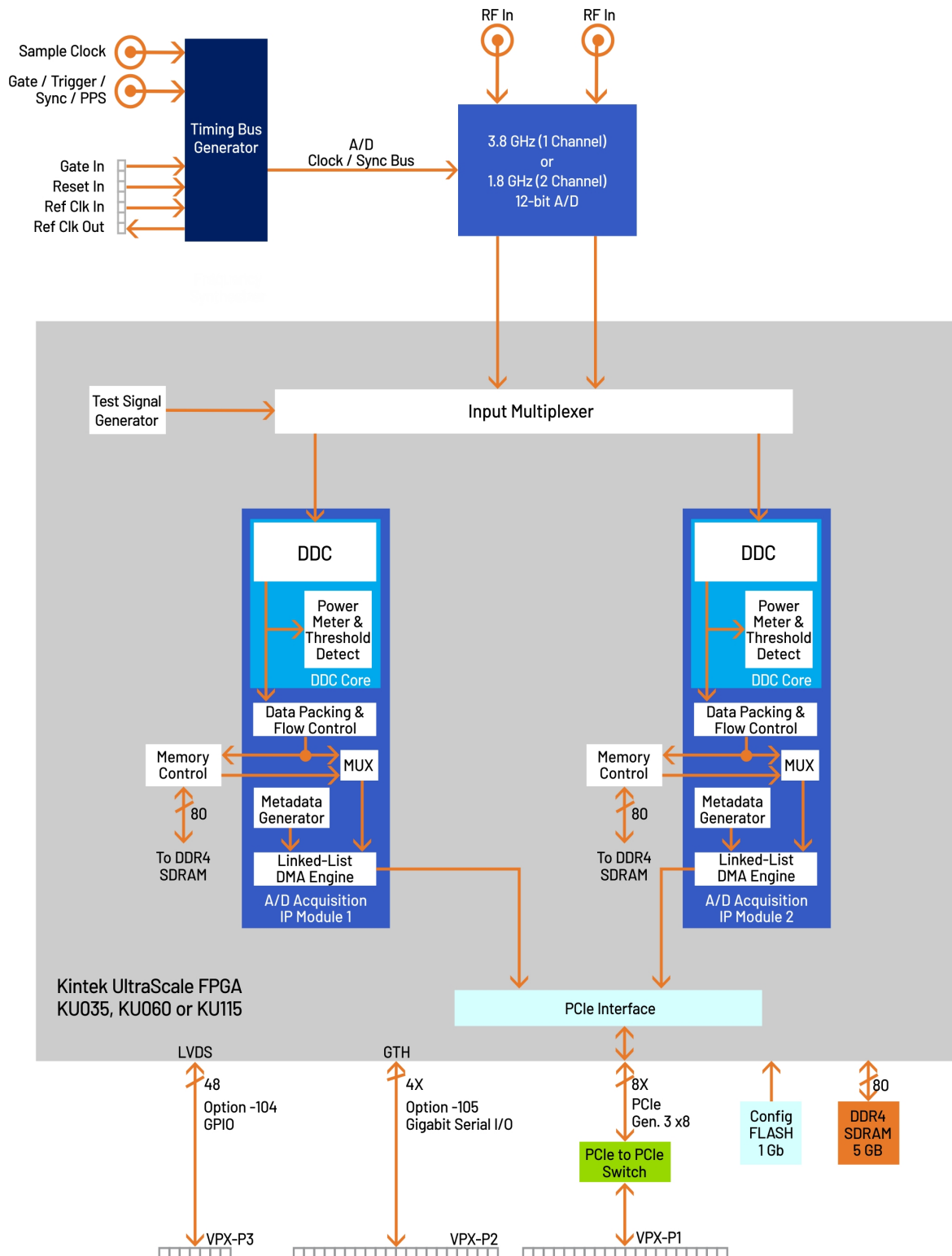
Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs: KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

FEATURES

- Xilinx® Kintex® UltraScale™ FPGA
- One-channel mode with one or two 3.6 GHz, 12-bit A/Ds
- Two-channel mode with two or four 1.8 GHz, 12-bit A/Ds
- Programmable DDCs (digital downconverters)
- 5 or 10 GB of DDR4 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express interface (Gen. 1, 2 & 3) up to x8
- Optional LVDS port and gigabit serial connections for custom FPGA I/O
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions

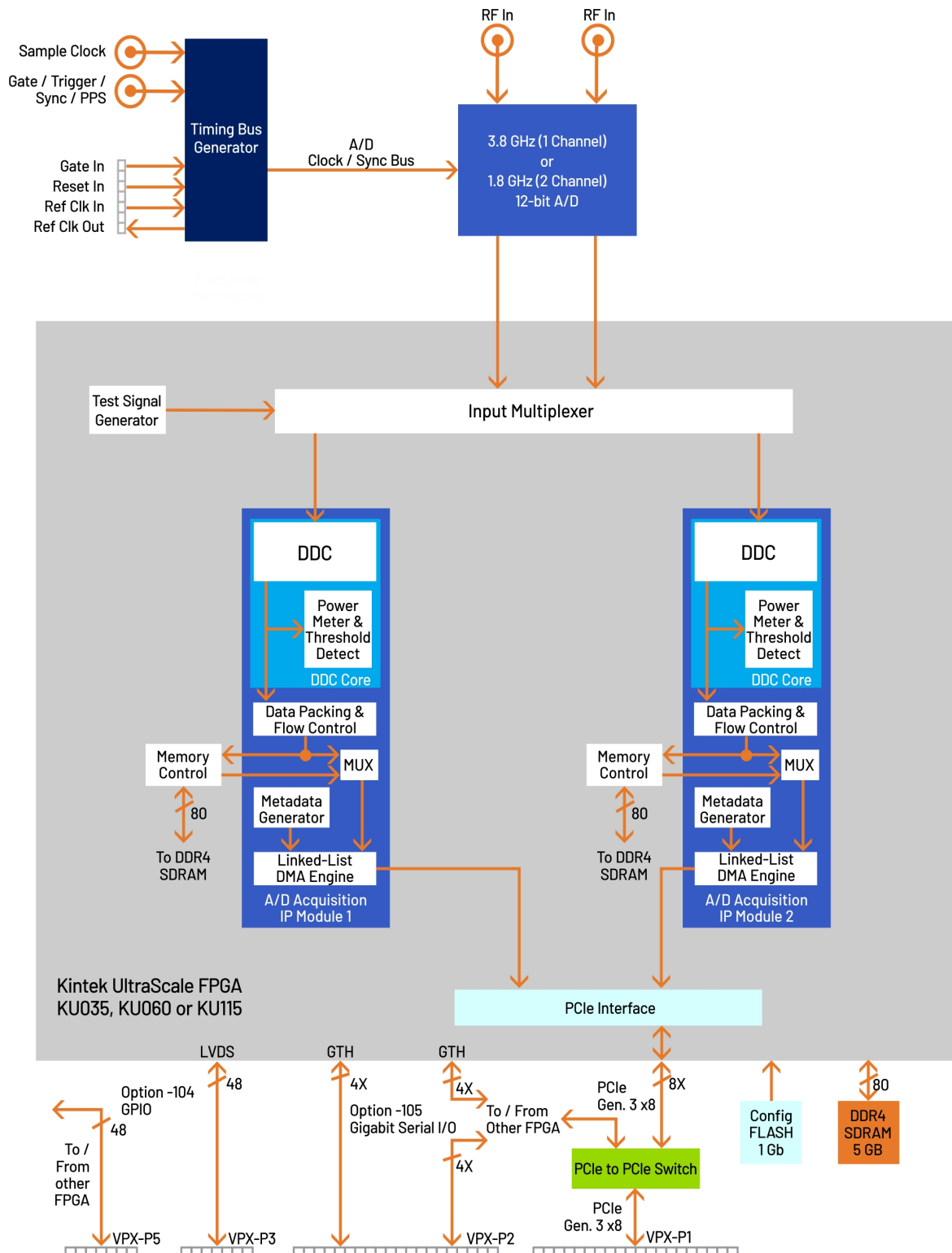
57841 BLOCK DIAGRAM

Click on a block for more information.



58841 BLOCK DIAGRAM

Block diagram shows half of the 58841. All resources are actually double of what is shown except for the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5.



THE JADE ARCHITECTURE

Evolved from the proven designs of Mercury's Cobalt[®] and Onyx[®] families, Jade[®] raises the processing performance while lowering the overall power requirements by building on the Xilinx family of Kintex UltraScale FPGAs. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions as well as providing an ideal platform for user-created intellectual property (IP).

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions include one or two A/D acquisition IP modules.

Each of the acquisition IP modules contains a powerful, programmable DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

A/D CONVERTER STAGE

The board's analog interface accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The full-scale input level of the ADC12D1800 can be digitally trimmed from +2 dBm to +4 dBm to simplify system calibration. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other board resources.

A/D ACQUISITION IP MODULES

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP modules can receive data from the A/Ds, or the test signal generators. The IP modules have associated a 5 or 10 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of the SDRAM is used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half

stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory is supported with a DMA engine for moving A/D data through the PCI-X interface. This powerful linked list DMA engine is capable of a unique Acquisition Gate Driven mode: In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

CLOCKING AND SYNCHRONIZATION

These models accept a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel μ Sync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The μ Sync bus includes gate, reset, and in and out reference clock signals. Two units can be synchronized with a simple cable. For larger systems, multiple units can be synchronized using the Model 5792 or 5892 high-speed sync module to drive the sync bus.

MEMORY RESOURCES

The architecture supports 5 or 10 GB bank of DDR4 SDRAM memory. User-installed IP along with the Mercury-supplied DDR4 controller core(s) within the FPGA can take advantage of the memory for custom applications.

PCI EXPRESS INTERFACE

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the boards.

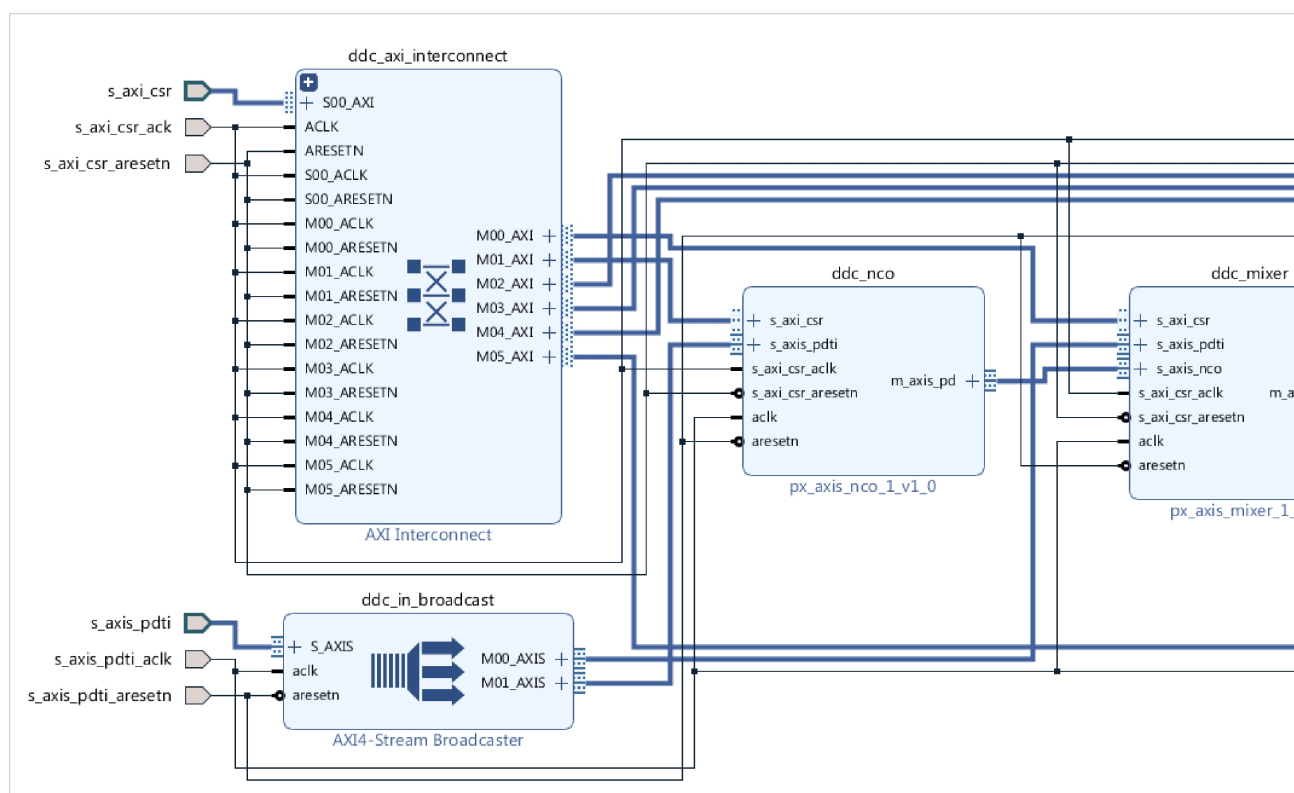
NAVIGATOR DESIGN SUITE

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into the factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

The **Navigator FPGA Design Kit (FDK)** for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Jade product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Jade design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations.

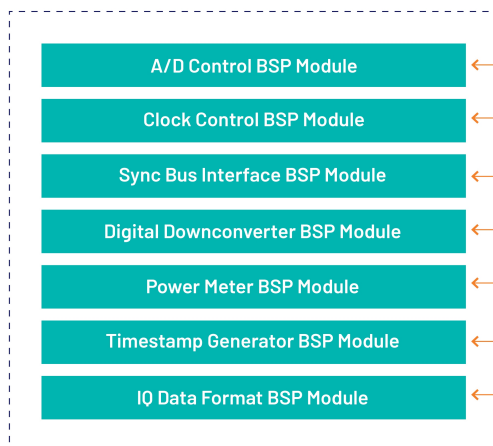
Navigator FDK includes an IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.

The **Navigator Board Support Package (BSP)** provides software support for Jade boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA. The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.

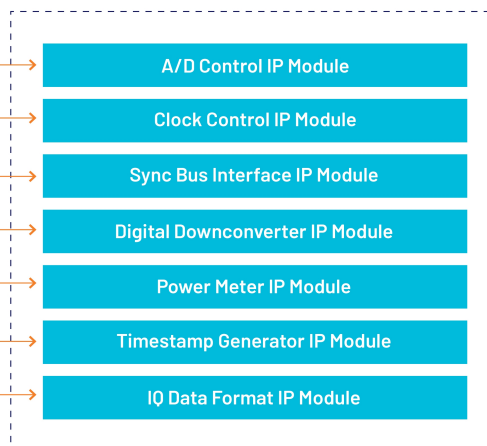


Navigator IP FPGA Design viewed in IP Integrator

NAVIGATOR BOARD SUPPORT PACKAGE

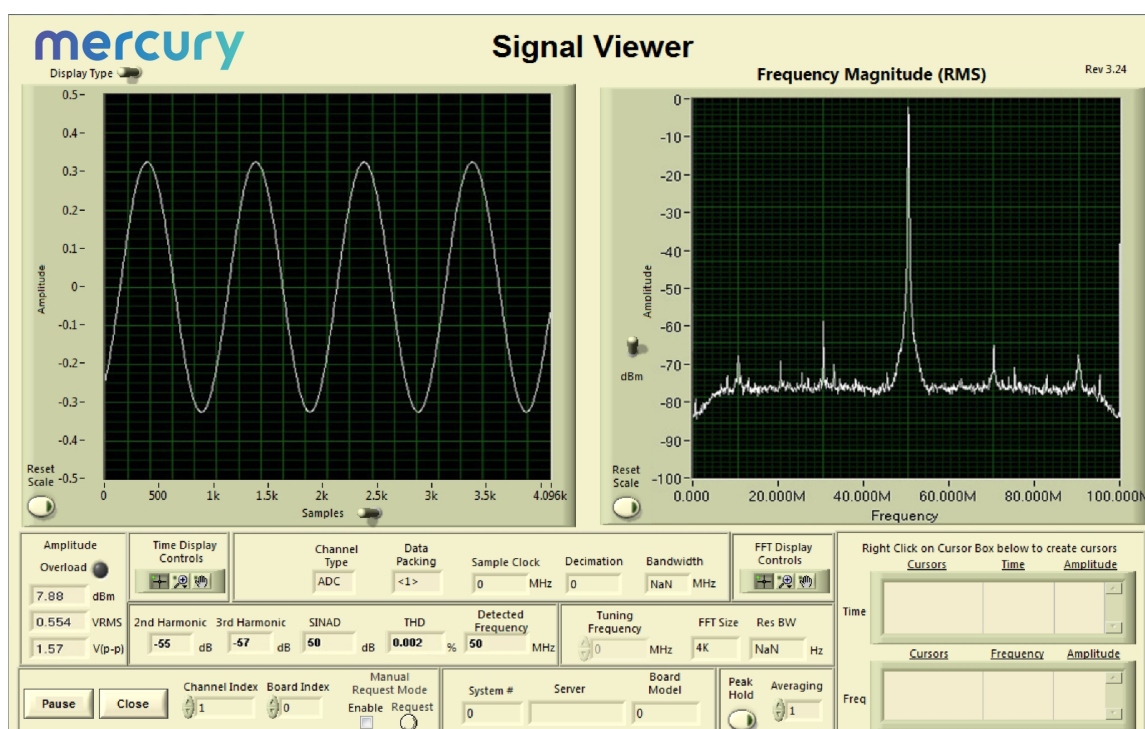


NAVIGATOR FPGA DESIGN KIT



Because all Jade boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the **Signal Viewer**, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Jade board and Navigator BSP and start viewing analog signals immediately.



FRONT PANEL CONNECTIONS

The front panel includes four SSMC coaxial connectors for clock, PPS, and analog input signals, and a 19-pin μ Sync input/output connector. The front panel also includes five LED indicators.



PPS Input

Connector: One SSMC coaxial connector, labeled **PPS IN**, for input of an external PPS or Gate signal.

• **PPS LED:** The green **PPS IN** LED illuminates when a valid PPS signal is detected. This LED will blink at the rate of the PPS signal.

Sync Bus

Connector: A μ Sync 19-pin connector, labeled **SYNC/GATE**, provides clock reset, reference clock, and gate inputs for A/D processing, and a reference clock output

for synchronizing multiple boards using an external sync module.

- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the PCB.
- **Link LED:** The green **LTK** LED illuminates in the following ways when a valid link has been established over the PCIe interface: Gen 1 – the LED blinks slowly (less than once per second); Gen 2 – the LED blinks about once per second; Gen 3 – the LED is constantly on.

- **Analog Input Connectors:** Two SSMC coaxial connectors, labeled **IN 1** and **IN 2**, for analog signal inputs to the ADC12D1800 A/D converter. **IN 1** is connected to the Q input of the ADC12D1800; **IN 2** is connected to the I input.
- **ADC Overload LED:** There is one red **OV** overload LED for the A/D input. This LED indicates an overload detection in the ADC12D1800, or an ADC FIFO overrun.
- **Clock Input Connector:** One SSMC coaxial connector, labeled **EXT CLK IN**, for input of an external sample clock for the ADC12D1800 A/D converter.
- **Clock LED:** The green **EXT CLK IN** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.

SPECIFICATIONS

Model 57861: One A/D; Model 58861: Two A/Ds

Front Panel Analog Signal Inputs (2 or 4)

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converters (1 or 2)

Type: Texas Instruments ADC12D1800

Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz

Resolution: 12 bits

Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz

Full Scale Input Level: may be trimmed from +2 dBm to +4 dBm with a 15-bit integer

Digital Downconverters (2 or 4)

Modes: One or two channels, programmable

Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz

Single-channel mode: decimation can be programmed to 8 or 16 to 512 in steps of 16

Dual-channel mode: decimation can be programmed to 4 or 8 to 256 in steps of 8; both channels share the same decimation value

Either mode: the DDC can be bypassed completely

LO Tuning Freq. Resolution: 32 bits, 0 to f_s

LO SFDR: >120 dB

Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: User-programmable 18-bit coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Source (1 or 2)

Front panel SSMC connector

Timing Bus (1 or 2)

19-pin μ Sync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input (1 or 2)

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)

Standard: Xilinx Kintex UltraScale XCKU035-2

Option -084: Xilinx Kintex UltraScale XCKU060-2

Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O

Option -104: provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector, Model 57861; and P5 connector, Model 58861 for custom I/O

Option -105: provides two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory

Type: DDR4 SDRAM

Size: 5 GB Model 57841; 10 GB Model 58841

Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: VPX board

Depth: 170.61 mm (6.717 in)

Height: 100 mm (3.937 in)

Weight: Approximately 14 oz (400 grams)

6U VPX INTERFACE

The 57841 & 58841 comply with the VITA 65.0 6U VPX specification. In addition to supporting PCIe Gen. 3, x8 on the VPX P1 connector, option -105 adds additional gigabit serial lanes for supporting user-installed protocols. On the 57841 option -105 installs four lanes from the FPGA to the P2 connector. On the 58841 the option installs four lanes from each of the FPGAs to the P2 connector and an additional four lanes between the FPGAs.

The 57841 & 58841 offer flexible interface options for the VPX-P3 and -P5 to meet system-specific requirements.

On the 57841 option -104 installs 24 pairs of LVDS connections between the first FPGA to the P3 connector. On the 58841 the option installs an addition 24 pairs between the second FPGAs and the P5 connector.

ORDERING INFORMATION

Model	Description
57841	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Kintex UltraScale FPGA - 6U VPX
58841	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Kintex UltraScale FPGA - 6U VPX

Options:

-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O to VPX P2, Model 57141A; P2 and P5 Model 58141A
-105	Gigabit serial FPGA I/O to VPX P1
-702	Air-cooled, Level 2
-763	Conduction-cooled, Level 3

Contact Mercury for compatible option combinations and complete specifications of rugged and conduction-cooled versions. Options may change, so be sure to contact Mercury for the latest information.

ACCESSORY PRODUCTS

Model	Description
2171	Cable Kit: SSMC to SMA
5792/5892	System Synchronizer and Distribution Board
5794/5894	High-Speed Clock Generator
9192	Rackmount high-speed system synchronizer

DEVELOPMENT SYSTEMS

Mercury offers development systems for Jade products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Jade boards. Please [contact Mercury](#) to configure a system that matches your requirements.

FORM FACTORS

Jade products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Jade Model 71841 XMC (1-Channel 3.6 GHz or 2-Channel 1.8 GHz 12-bit A/D with DDC, Kintex UltraScale FPGA) has the following variants:

Model	
52841	3U VPX board (single XMC)
57841	6U VPX board (single XMC)
58841	6U VPX board (dual XMC)
71841	XMC module
78841	PCIe board (single XMC)



Corporate Headquarters

50 Minuteman Road
Andover, MA 01810 USA
+1 978.967.1401 tel
+1 866.627.6951 tel
+1 978.256.3599 fax

International Headquarters

Mercury International
Avenue Eugène-Lance, 38
PO Box 584
CH-1212 Grand-Lancy 1
Geneva, Switzerland
+41 22 884 5100 tel

Learn more

Visit: mrcy.com/go/MP57841

For technical details, contact:
mrcy.com/go/CF57841



The Mercury Systems logo is a registered trademark of Mercury Systems, Inc. Other marks used herein may be trademarks or registered trademarks of their respective holders. Mercury products identified in this document conform with the specifications and standards described herein. Conformance to any such standards is based solely on Mercury's internal processes and methods. The information contained in this document is subject to change at any time without notice.

