DATASHEET

MERCURY COMPUTER SYSTEMS™

OpenFDK

Accelerate FPGA Design and Integration

- Standards-based interfaces (OCP) for interoperability and re-use
- Enhanced developer productivity
- Reduced design cycles through verification and simulation
- Lower cost through IP re-use
- Variety of toolsets customizable for your exact system and design needs

OpenFDK (Open FPGA Developer's Kit) from Mercury Computer Systems ease application development by supplying optimized infrastructure IP to abstract the lower-level hardware details and system utilities for FPGA integration and control. OpenFDK elements provide a consistent set of IP and design resources across platforms (ATCA®, 6U VPX/VXS, 3U VPX) for optimal code portability.

The OpenFDK IP modules deliver a pre-validated environment and infrastructure for an application-ready platform. To ensure timing and performance, the IP modules are supplied with significant timing margin. The IP is placed to allow application logic to interface with the communication infrastructure in a modular way that simplifies placement and routing of the FPGA.

OpenFDK Components

Because the utilization of FPGA technology in systems varies greatly, Mercury supplies a variety of OpenFDK tools designed to accommodate your specific system and design needs.

OpenFDK consist of the following components:

- Hardware-specific layer for pin descriptions and basic FPGA I/O functionality
- Communications infrastructure IP to interface with applications, including multi-ported memory controllers, fabric connections, and streaming I/O protocols
- Software APIs for board control and data transfer
- Diagnostic bitstreams to validate hardware and IP functionality, including link checkers and memory checkers on all external interfaces
- Dataflow design examples, which can be used as templates for application development

Standard Interfaces for Interoperability and Re-Use

The re-use of already developed and validated IP offers significant advantages, including the ability to port existing application code to different form factors with minimal modification and re-validation. To avoid the learning curve associated with many proprietary interfaces, the OpenFDK IP is designed with standard Open Core Protocol (OCP) interfaces, which enable interoperability with IP components from other OCP-affiliated IP suppliers. These OCP interfaces standardize the connectivity among components to provide the framework for modular FPGA IP design.

Mercury has defined the following standard OCP interfaces for our components:

- WCI – Worker Control Interface (register read/write interface)
- WSI – Worker Streaming Interface
- WMemI – Worker Memory Interface
- WMI – Worker Messaging Interface

Decoupling the interface from the underlying functional logic of a component permits the redesign of that function with minimal impact to the complete FPGA design. Isolation of the component through standard interfaces requires only that the component be unit-tested when the function is modified, instead of re-validating the entire system, making it easier to incorporate last-minute application design changes into the system.

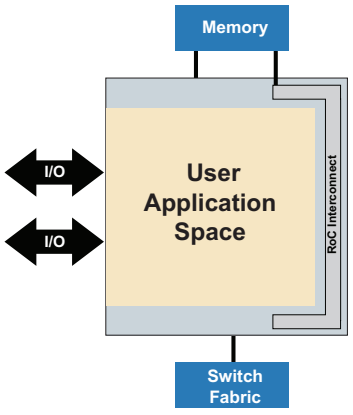


***Figure 1**. OpenFDK functional block diagram*

Accelerated System Integration

Complex systems require integration of FPGAs with other processors for maximum effectiveness. The OpenFDK IP includes both IP modules and easy-to-use software API support for seamless communication between Power Architecture™ boards and FPGA boards. OpenFDK provides an extension of the fabric interconnect into the FPGA with the Mercury RoC (RACE®-on-Chip) bus. This multi-point, high-bandwidth communication pathway for the FPGA compute node enables system memory mapping and shared-memory buffer creation within the FPGA. The RoC architecture is responsible for the FPGA node's dramatic high-speed data movement and seamless integration into the multicomputer switch fabric.

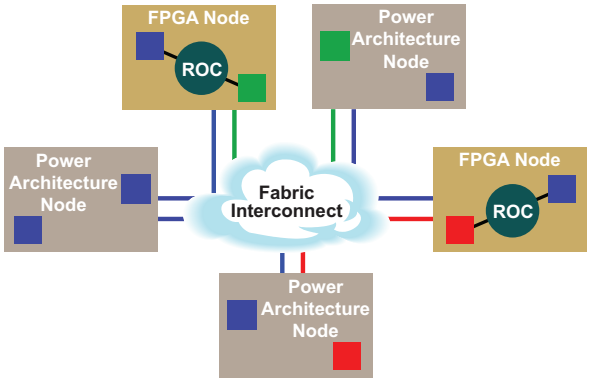


***Figure 2**. RoC architecture in multicomputer switch fabric*

OpenFDK Tools for Traditional Multicomputer Applications

OpenFDK tools aid users in developing FPGA applications from a collection of Mercury-supplied re-usable IP modules, user-developed IP modules, and third-party IP modules for a traditional fabric-connected multicomputer environment.

The Mercury communication infrastructure IP components included in these toolkits (depending on platform) are:

- I/O protocols, such as serial front-panel data port (SFPDP, VITA 17.1)
- SRAM and DRAM multi-ported memory controllers for low-latency, efficient memory utilization
- DMA endpoints
- Fabric interconnect protocols, such as serial RapidIO®, PCI Express®, and 10GE
- RoC multi-point, high-bandwidth communication pathway
- Internal control ring (ICR) lightweight, control, and status pathway
- FPGA mesh LVDS sockets
- BERT checkers for memory and I/O links

StreamFDK Tools for FPGA-Centric Streaming Applications

Mercury offers streaming-based OpenFDK tools designed for point-to-point, mesh, and fabric-connected FPGA boards, where the need to have an FPGA as a peer to a processor is not required. The communications infrastructure IP in StreamFDK is geared toward mixed-signal boards (A/D and D/A), and digital IO boards with preprocessing functionality, as well as FPGA-centric beamforming dataflows. StreamFDK provides a channelized dataflow architecture to support these processing requirements. In these architectures, a processor is needed simply for initialization, control, maintenance, and medium bandwidth communications.

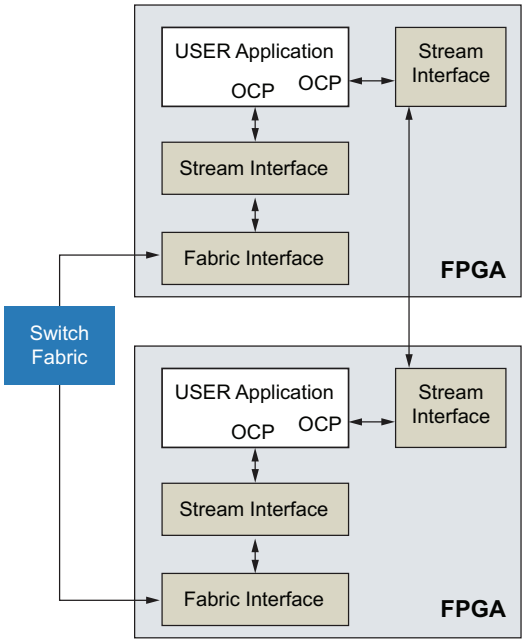


***Figure 3**. StreamFDK block diagram*

The Mercury StreamFDK infrastructure IP included with these tools (depending on platform) are:

- A/D and D/A interfaces
- I/O protocols, such as serial front-panel data port (SFPDP, VITA 17.1, VITA49)
- High-speed serial I/O sockets that incorporate Aurora or XAUI, point-to-point RapidIO (guaranteed delivery) interfaces
- FPGA mesh LVDS sockets
- Protocol interfaces (RapidIO, PCIe, 10GE)
- Out-of-band control buses to connect to onboard processors or FPGA-embedded Power Architecture processors

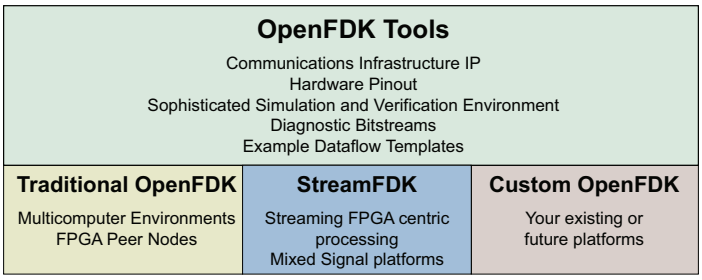
Customizing OpenFDK Tools

Based on our extensive experience in developing toolkits for a variety of FPGA devices and form factors, Mercury can efficiently develop an OpenFDK set of tools to fit your present and future system architectures. Because we craft each of these tools to fit your specific needs, we can modify the communication infrastructure components for the level of hardware abstraction, as necessary.

For boards that are designed by the user, Mercury can provide a design kit that allows user-designed boards to have FDK on them. This allows Mercury standard MultiCore Plus® software to communicate with the board. Customized tools enhance developers' productivity by allowing them to concentrate on system architecture and FPGA application design.

IP Library Components

- SDRAM controllers DDR2, DDR3
- SRAM QDRII+ memory controllers
- Memory multiplexers
- SFPDP interfaces
- Serial RapidIO interfaces
- PCIe interfaces
- Multi-channel fabric-based DMA controllers
- XAUI
- Aurora
- Serial RapidIO point-to-point
- VITA 49
- Stream interfaces



Software Support

OpenFDK includes an interface library that can run on a general-purpose processor to control and use the FPGA. This library includes functions to:

Load FPGA patterns from:

- File
- Fabric-connected memory
- Flash memory

Control the FPGA:

- Take ownership
- Reset the FPGA
- Inquire or reset error states

Use the FPGA:

- Map FPGA memory for use from the general-purpose processor
- Map general-purpose processor memory for use from the FPGA
- Transfer data either way by using programmed I/O or DMA
- Generate mailbox interrupts to notify the software application of processing completion or data available

FPGAs can be loaded easily from a file during application development. They can also be loaded by applications that re-use the FPGA for different bitstreams. To optimize for systems that use the same bitstream for many FPGAs, load the file into compute node memory and then load it into multiple FPGAs directly from compute node memory. Once the FPGA is mature, it can be loaded into the flash memory and programmed quickly from there.

Once the FPGA is loaded, it can be easily used via Mercury's standard ICS APIs. This allows for memory mapping or using DMA engines in the same way two compute nodes talk to each other, or a compute node talks to an I/O device. Either the FPGA's or the general-purpose processor's DMA engine can be used to master transfers. The FPGA can send notification to the software running on the general-purpose processor by sending either a value being polled or a mailbox interrupt to wake up a sleeping application.

Specifications

Development Environment and Tools

Mentor QuestaSim® VHDL/Verilog

Synplicity® (Xilinx®)

Xilinx ISE

Altera Quartus®

See the Release Notes for current versions.

Related Reference Documents for OpenFDK

SVE – Simulation and Verification Environment datasheet

MultiCore Plus Software Environment Brochure

Specific Mercury high-performance board datasheet(s)

Operating System Support

Linux®

VxWorks®

MCOE™

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MERCURY COMPUTER SYSTEMS™

INNOVATION THAT MATTERS™

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