Quartz 6350S

8-channel A/D & D/A small form factor subsystem with Xilinx Zynq UltraScale+ RFSoC - Gen 1

Ideal for deployment in harsh environments

- High-bandwidth data streaming
- Waveform signal generator
- Communication receiver and transmitter
- Electronic Warfare transponder
- Analog I/O for digital recording and playback
- Sensor interfaces

The Quartz® Model 6350S is a high-performance RF converter and processing subsystem in a small, rugged module. Designed to be integrated into larger systems with minimal design effort, the 6350S delivers the performance and high-channel density of RFSoC in a small, convenient footprint.

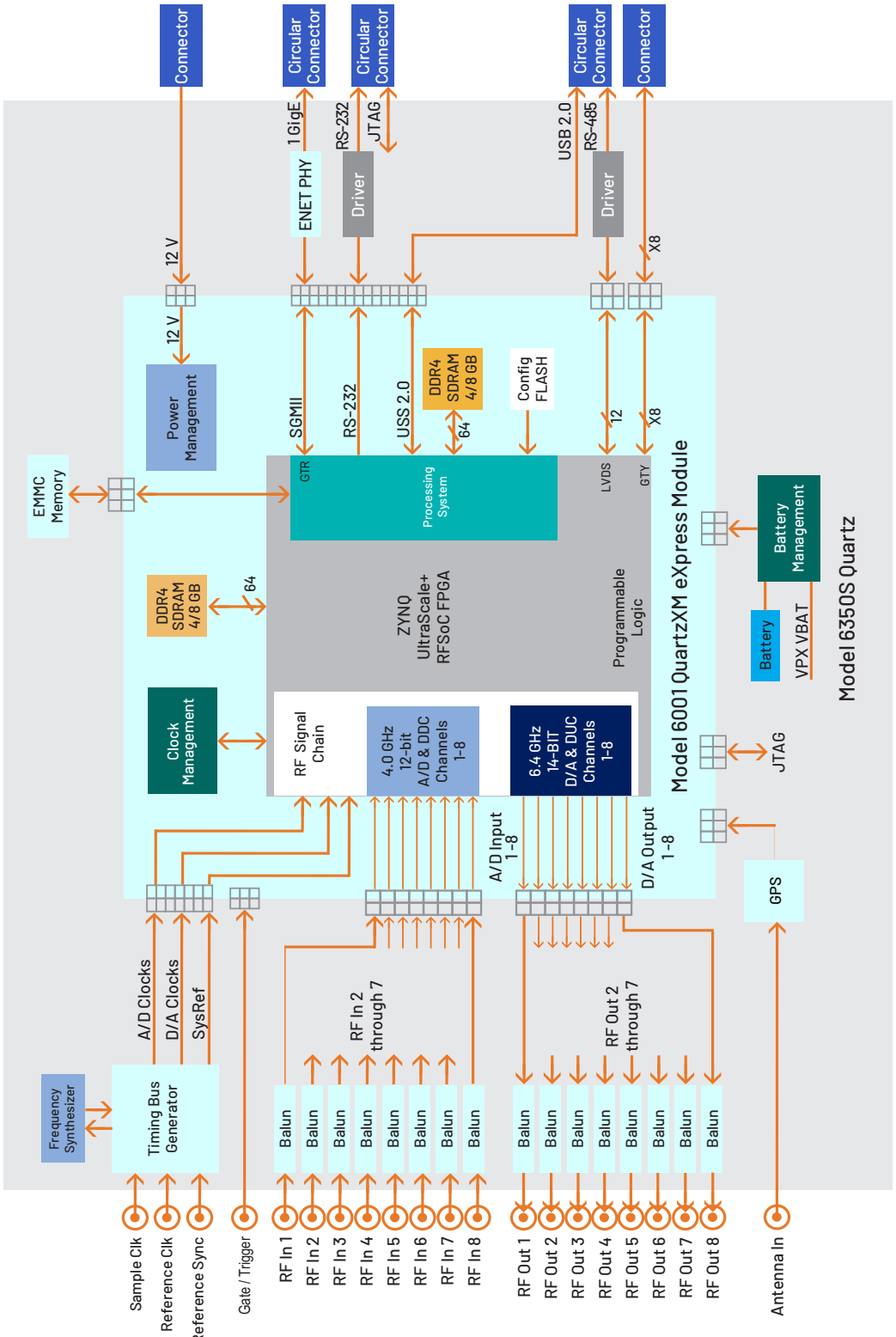
Complementing the RFSoC's on-chip resources are the 6350S's sophisticated clocking section, a low-noise front end for RF input and output, 16 GBytes of DDR4, an 8-lane gigabit serial interface operating at 28 Gbits/sec, and general-purpose I/O signal paths to the FPGA

FEATURES

- Complete RF converter and processing subsystem
- Multi-module synchronization
- Rugged and conduction-cooled
- Ideal for integration into custom enclosures
- Incorporates Xilinx® Zynq® UltraScale+™ RFSoC
- 16 GB of DDR4 SDRAM
- Navigator® BSP for software development
- Navigator® FDK for custom IP development
- Free lifetime applications support

6350S BLOCK DIAGRAM

Click on a block for more information.



ARCHITECTURE

The 6350S design places the RFSoC as the cornerstone of the architecture. All control and data paths are accessible by the RFSoC's programmable logic and processing subsystem. A full suite of Mercury-developed IP and software functions utilize this architecture to provide data capture, processing and waveform generating solutions for many of the most common application requirements.

EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. Mercury's Navigator FPGA Design Kit (FDK) includes the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado® IP Integrator. In addition to the IP Integrator block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the factory-installed functions or use the Navigator kit to completely replace the Mercury IP with their own.

The Navigator Board Support Package (BSP), the companion product to the Navigator FDK, provides a complete C-callable library for control of the 6350S's hardware and IP. The Navigator FDK and BSP libraries mirror each other where each IP function is controlled by a matching software function, simplifying the job of keeping IP and software development synchronized.

The Navigator BSP includes support for Xilinx's PetaLinux running on the ARM Cortex-A53 processors. When running under PetaLinux, the Navigator BSP libraries enable complete control of the 6350S either from applications running locally or on the ARMs, or using the Navigator API control and command from remote system computers.

A/D CONVERTER STAGE

The 6350S accepts analog IF or RF inputs on eight coax connectors. These inputs are transformer-coupled into the RF signal chain of the RFSoC. Inside the RFSoC, the analog signals are routed to eight 4 GSPS, 12-bit A/D converters. Each converter has built-in digital downconverters with programmable 1x, 2x, 4x or 8x decimation and independent tuning. The A/D digital outputs are delivered into the Zynq's programmable logic and processor subsystem for signal processing, data capture, or for routing to other resources.

In addition to the A/D's built-in decimation, an additional stage of IP-based decimation provides another 16x stage of data reduction, ideal for applications that need to stream data from all eight A/Ds.

D/A CONVERTER STAGE

The RFSoC's eight D/A converters accept baseband real or complex data streams from the FPGA's programmable logic. Each 6.4 GSPS, 14-bit D/A includes a digital upconverter with independent tuning and interpolations of 1x, 2x, 4x and 8x. Each D/A output is transformer-coupled to a coax connection located on the edge of the module.

CLOCKING AND SYNCHRONIZATION

An on-board timing bus generator uses a programmable frequency synthesizer to generate the sample clock and all required timing signals. The on-board sample clock can also be locked to a reference clock received through a coax connector. A multifunction gate/trigger input is also available for external control of data acquisition and playback.

MEMORY RESOURCES

The 6350S architecture supports up to 8 GBytes of DDR4 SDRAM memory accessible from the Programmable Logic. User-installed IP, which along with the Mercury-supplied DDR4 controller core within the FPGA, can take advantage of the memory for custom applications. An additional 8 GByte bank of DDR4 SDRAM is available to the Processing Subsystem as program memory and storage.

HIGH-SPEED GIGABIT SERIAL INTERFACE

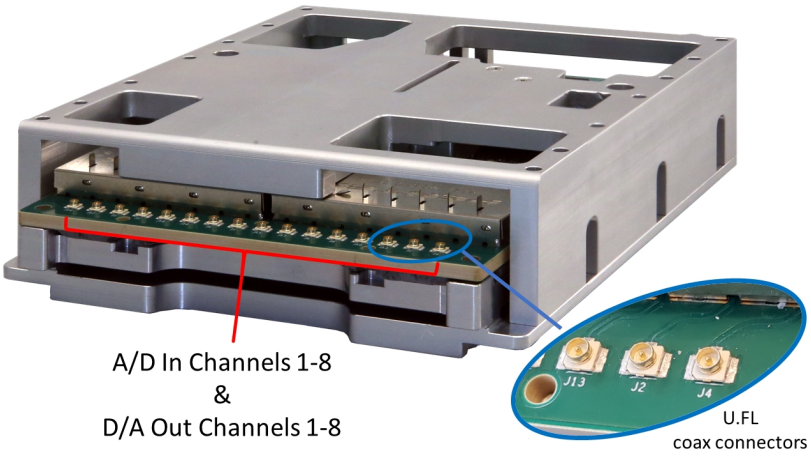
The Model 6350S supports eight 28 Gb/sec full duplex lanes. Users can choose to connect to other serial-enabled devices with high-speed copper cables or connect to a copper-to-optical interface for enabling long transfer distances. With the 100 GigE UDP interfaces provided with the Navigator FPGA Design Kit, or installation of a user-provided serial protocol, this optical interface enables a high-speed gigabit data streaming path between the module and data storage or other processing components.

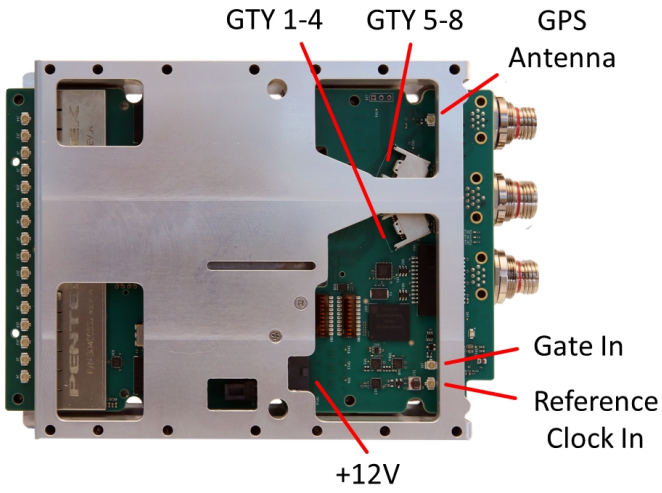
GPS

A GPS receiver provides time and position information to the FPGA and ARM processors. This information can be used for precise data tagging. The GPS provides a 1 PPS and a reference clock to the FPGA.

DESIGNED FOR STREAMLINED INTEGRATION

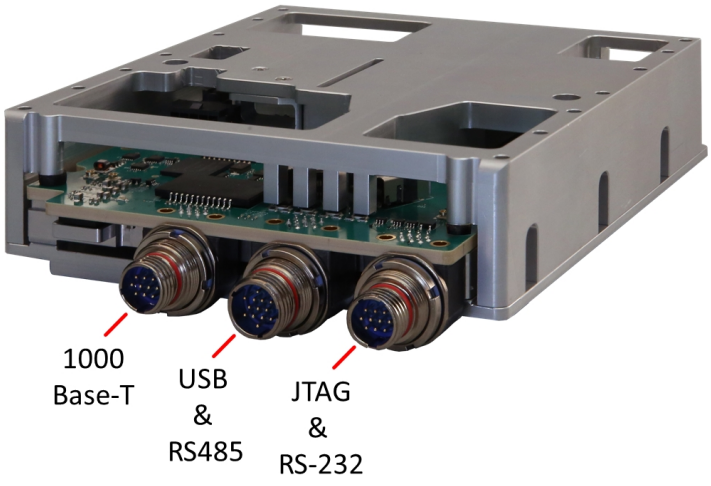
Model 6350S is a complete RF converter and processing system in a small, rugged module. Requiring only a single 12V power supply, the module can be integrated as a component in a larger system with minimal design effort.





All analog I/O and control and communication interfaces are easily accessible, simplifying connections to other system components.

The bottom surface of the module provides an efficient thermal interface, enabling conduction-cooling and allowing fan-less operation in most installations.



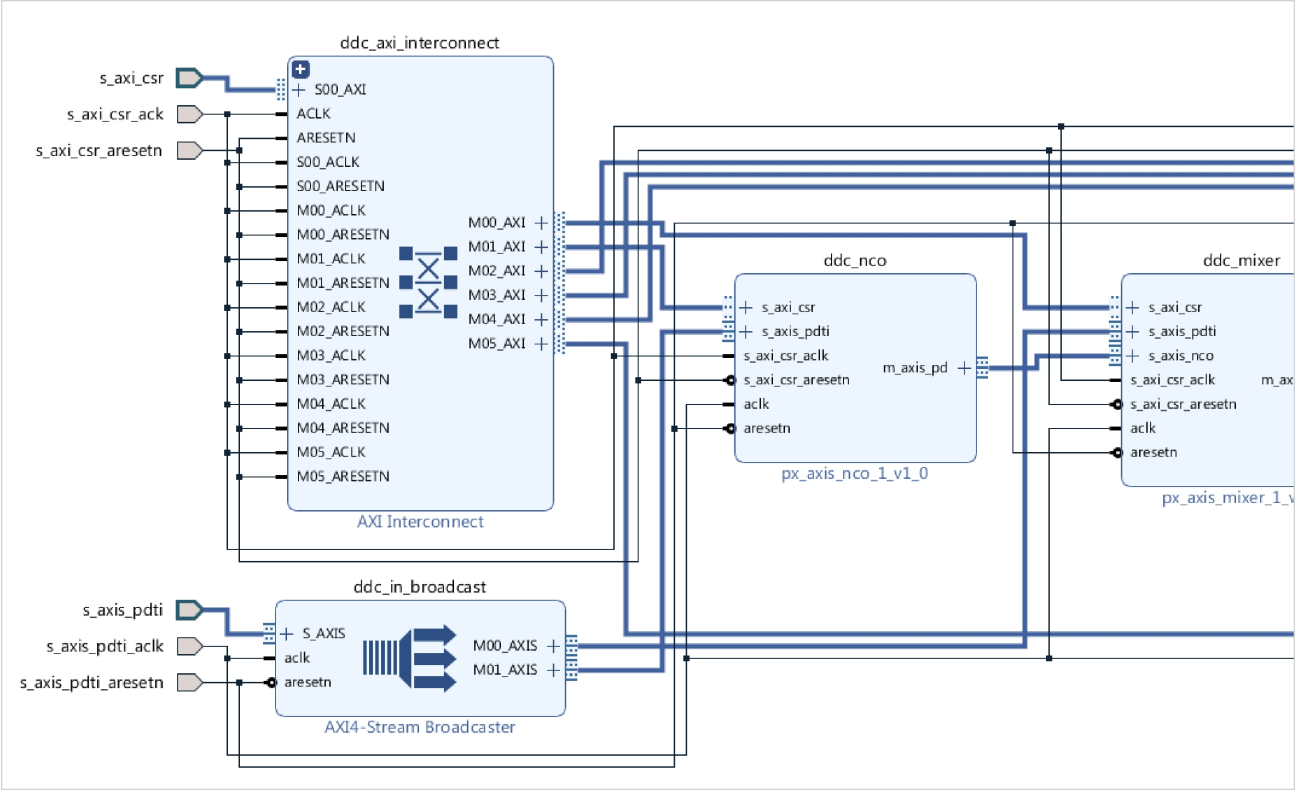
NAVIGATOR DESIGN SUITE

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into the factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

The Navigator FPGA Design Kit (FDK) for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Jade product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Jade design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations.

Navigator FDK includes an IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.

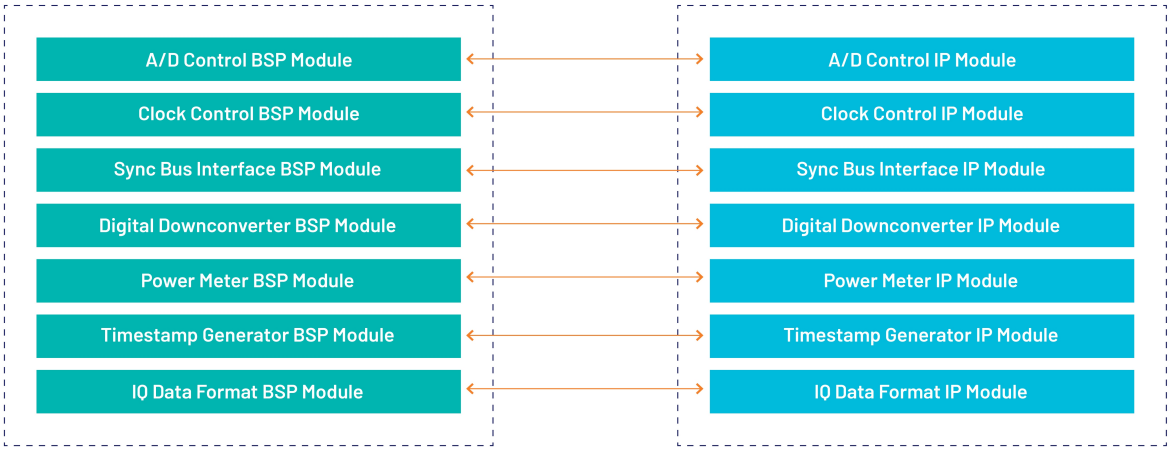
The **Navigator Board Support Package (BSP)** provides software support for Jade boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA. The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.



Navigator IP FPGA Design viewed in IP Integrator

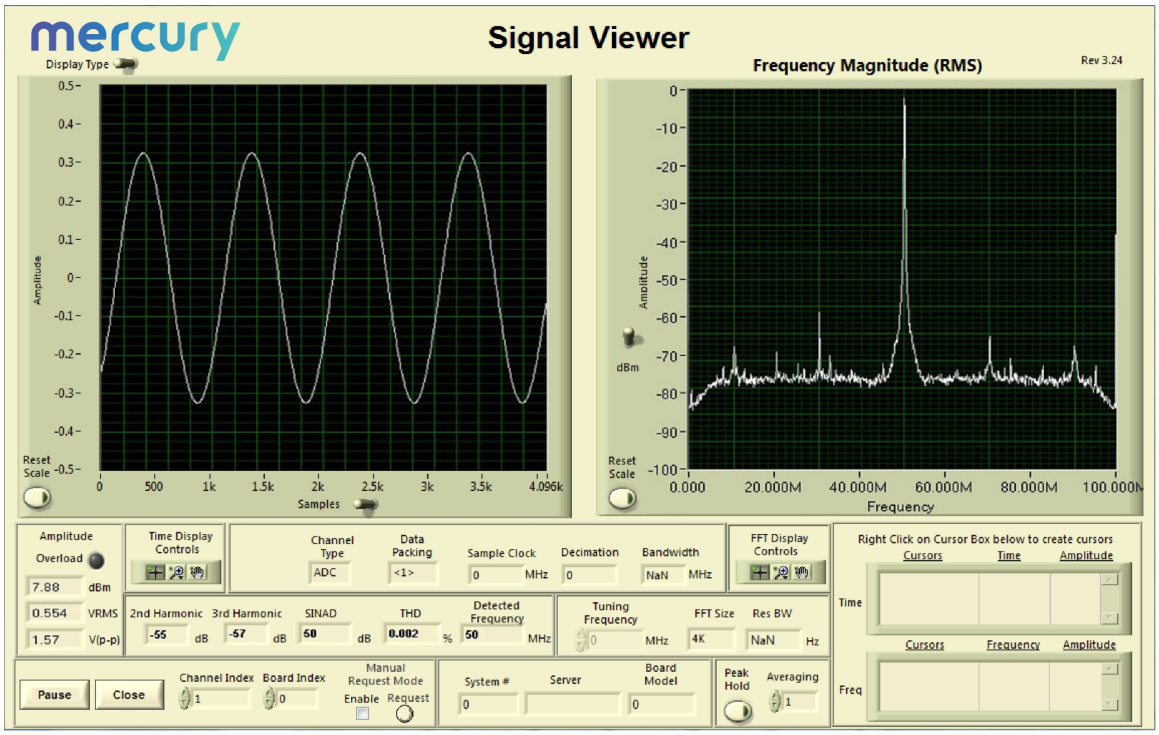
NAVIGATOR BOARD SUPPORT PACKAGE

NAVIGATOR FPGA DESIGN KIT



Because all Jade boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the **Signal Viewer**, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Jade board and Navigator BSP and start viewing analog signals immediately.



SPECIFICATIONS

Field Programmable Gate Array

Type: (standard) Xilinx Zynq UltraScale+ RFSoC XCZU27DR

- Option -028: Xilinx Zynq UltraScale+ RFSoC XCZU28DR

Speed: (standard) -1 speed grade

- Option -002: -2 speed grade

RFSoC RF Signal Chain

Analog Inputs

- Quantity: 8
- Location: Front edge (A/D In Channels 1-8)
- Connector Type: U.FL
- Input Type: Transformer-coupled
- Transformer Type: Mini-Circuits TCM1-83X+
- Full Scale Input: +10 dBm into 50 ohms
- 3 dB Passband: 10 MHz to 3700 MHz

A/D Converters

- Quantity: 8
- Sampling Rate: 4.0 GHz
- Resolution: 12 bits

Digital Downconverters

- Quantity: 1 per A/D
- Decimation Range: 1x, 2x, 4x, and 8x
- LO Tuning Freq. Resolution: 48 bits, 0 to f_s
- Filter: 80% pass band, 89 dB stop-band attenuation

Analog Outputs

- Quantity: 8
- Location: Front edge (D/A Out Channels 1-8)
- Connector Type: U.FL
- Output Type: Transformer-coupled
- Transformer Type: Mini-Circuits TCM1-83X+
- Full Scale Output: 0 dBm into 50 ohms

  3 dB Passband: 10 MHz to 3700 MHz

D/A Converters

- Quantity: 8
- Sampling Rate: 6.4 GHz
- Resolution: 14 bits

Digital Upconverters

- Quantity: 1 per D/A
- Interpolation Range: 1x, 2x, 4x, and 8x
- LO Tuning Freq. Resolution: 48 bits
- Filter: 80% pass band, 89 dB stop-band attenuation

Sample Clock

- Source: On-board programmable clock

Reference Clock

- Source: On-board oscillator, on-board GPS, or external source
- External Source Location: Top panel (Reference Clock In)
- Connector Type: U.FL
- Level: -10 dBm to +24 dBm

Gate/Trigger

- Source: Programmable through software or external connector
- External Source Location: Top panel (Reference Clock In)
- Connector Type: U.FL
- Level: TTL

GPS

Source: On-board

Antenna Connector Location: Top panel (GPS Antenna)

Connector Type: U.FL

RFSoC Processing System

ARM Cortex-A53:

- Quantity: 4
- Speed: 1.5 GHz

ARM Cortex-R5:

- Quantity: 2
- Speed: 600 MHz

Processor I/O:

- Interfaces: USB 2.0 and RS-485
  - Location: Rear edge (USB & RS485)
  - Connector Type: Circular, Glenair Mighty Mouse Series
- Interface: 1 GigE
  - Location: Rear edge (1000 Base-T)
  - Connector Type: Circular, Glenair Mighty Mouse Series

- Interface: RS-232
  - Location: Rear edge (JTAG & RS-232)
  - Connector Type: Circular, Glenair Mighty Mouse Series

FPGA I/O

Interface: GTY

Quantity: 8 full duplex lanes

Speed: 8 Gb/sec

Location: Top panel (GTY 1-4 & GTY 5-8)

Connector Type: Samtec ARF6

Protocol: 100 GigE UDP IP core provided in Navigator FPGA Design Kit or user-supplied

JTAG

Location: Rear edge (JTAG/RS-232)

Connector Type: Circular, Glenair Mighty Mouse Series

Memory

Processing System:

- Type: DDR4 SDRAM
  - Size: (standard) 4 GB
  - Option -151: 8 GB
- Speed: 1200 MHz (2400 MHz DDR)
  - Type: eMMC
  - Size: 64 GB

Programmable Logic:

- Type: DDR4 SDRAM
  - Size: (standard) 4 GB
  - Option -151: 8 GB
  - Speed: 1200 MHz (2400 MHz DDR)

FPGA Configuration FLASH:

- Type: QSPI NOR Flash
  - Size: 2x 1 Gb

Environmental

Option -703: Level L3 (conduction-cooled)

- Operating Temp: –20° to 60° C (with 50° C cold plate)
- Storage Temp: –50° to 100° C
- Relative Humidity: 0 to 100%

Physical

Dimensions:

- Depth: 170 mm (6.7 in)
- Height: 38 mm (1.5 in)
- Width: 117 mm (4.6 in)

Weight: 29.8 oz.

Power

Voltage: +12

Location: Top panel (+12V)

Connector Type: Molex IPL1

Maximum Power Consumption: 46.62 Watts

ORDERING INFORMATION

Model	Description
6350S	8-channel A/D & D/A small form factor subsystem with Xilinx Zynq UltraScale+ RFSoC - Gen 1

Options	Description
-002	-2 FPGA speed grade, -1 standard
-028	XCZU28DR FPGA (XCZU27DR is standard)
-151	8GB processor system memory, 8 GB programmable logic memory
-703	Air-cooled, Level L3

Contact Mercury for compatible option combinations.

ACCESSORY PRODUCTS

Model	Description
2187	6350S Accessories

Option	Description
-150	Development cable set without optical cable
-151	Development cable set with optical cable
-701	Top cover plate with built-in fan, replaces standard top plate for benchtop cooling

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