Cobalt 78610

LVDS digital I/O
PCIe board with Virtex-6 FPGA

Ideal for control and data capture applications

- Provides 32 pairs of LVDS digital I/O
- LVDS is popular for high-speed video, graphics, and general-purpose computer buses
- User-configurable Virtex-6 FPGA
- Rugged, conduction-cooled option for military and avionics applications

The 78610 digital I/O board provides 32 LVDS differential inputs or outputs plus LVDS clock, data valid, and data flow control on a front panel 80-pin connector. Its built-in data capture and data generation feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

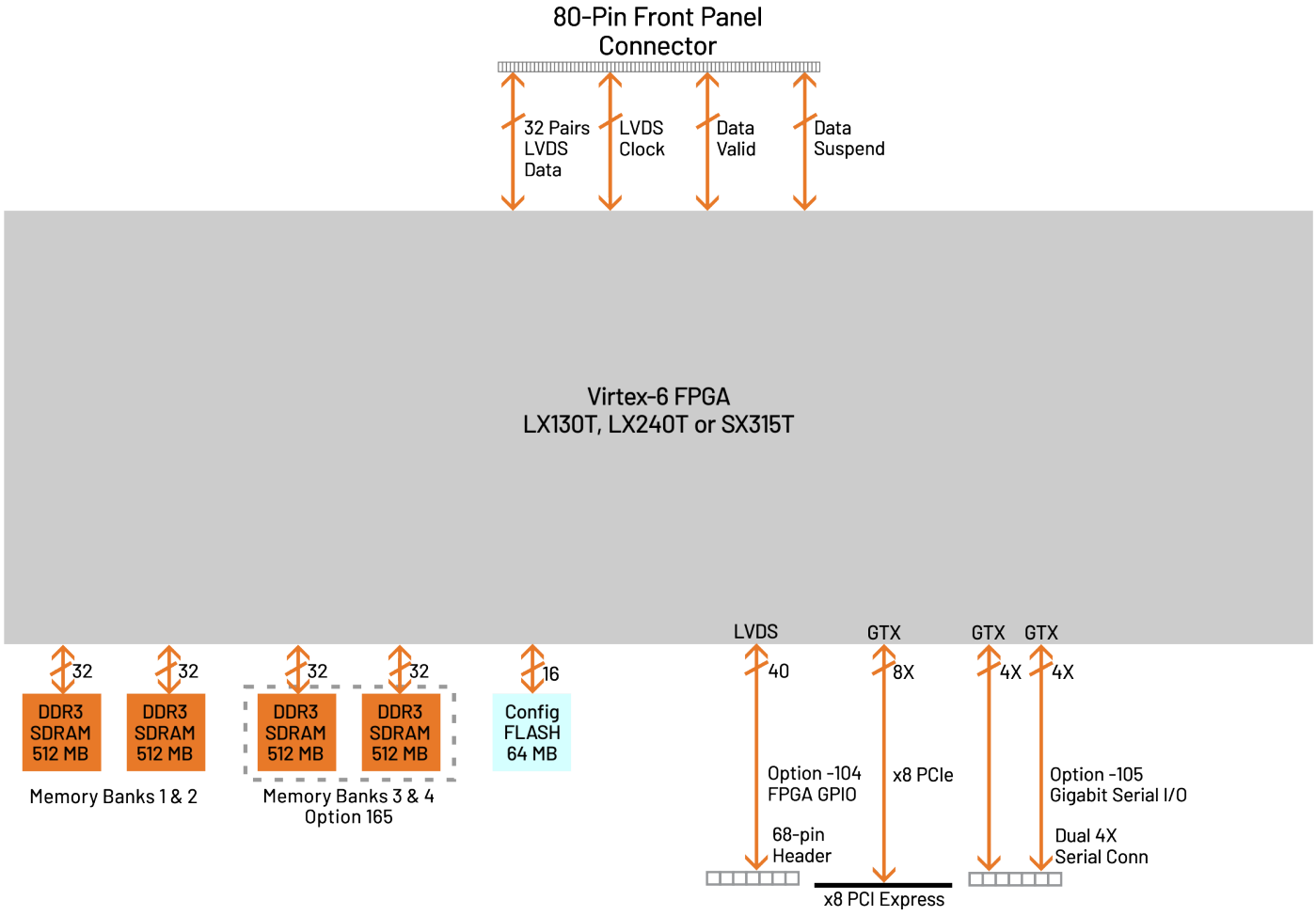
In addition to supporting PCI Express Gen. 1 as a native interface, the 78610 includes a general-purpose connector for application-specific I/O.

FEATURES

- 32 bits of LVDS digital I/O
- One LVDS clock
- One LVDS data valid
- One LVDS data suspend
- Supports LXT and SXT Virtex-6 FPGA
- DMA controller moves data to and from system memory
- Up to 2 GB of DDR3 SDRAM
- PCI Express interface
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O to the carrier board

78610 BLOCK DIAGRAM

Click on a block for more information.



THE COBALT ARCHITECTURE

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's interface. The 78610 factory-installed functions include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

IP modules for DDR3 SDRAM memories, a controller for all data clocking, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78610 to operate as a complete turnkey solution without the need to develop any FPGA IP.

EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. The GateFlow FPGA Design Kits include all of the factory-installed modules as document source code. Developers can integrate their own IP with the factory-installed functions or use the GateFlow kit to completely replace the IP with their own.

XILINX VIRTEX-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

ACQUISITION IP MODULE

The module can be configured for digital input mode by setting a jumper on the board. In this case, the board accepts input data Clock and input Data Valid signals. This supports a continuous input Clock with data accepted only when the Data Valid line is true. The board can optionally generate a Data Suspend output signal indicating that the 78610 is no longer capable of accepting data. The board accepts 32 bits from the front panel connector or from a non-board test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Memory banks are supported with DMA engines for easily moving input data through the PCIe interface.

GENERATION IP MODULE

The module can be configured for digital output mode by setting a jumper on the board. In this case, the board generates output data Clock and output Data Valid signals. This supports a continuous output Clock with data valid only when the Data Valid line is true. The board can optionally accept a Data Suspend input signal to halt data generation when the destination device is no longer capable of accepting data.

A linked-list controller allows users to generate 32-bit digital words out through the front panel LVDS connector from tables stored in either on-board or off-board host memory. Parameters including length of table, delay from software trigger, table repetition, etc. can be programmed for entry. Up to 64 individual link entries can be chained together to create complex output patterns with minimum programming.

MEMORY RESOURCES

The 78610 hardware architecture supports up to four independent 512 MB memory banks of DDR3 SDRAM. The board is always configured with 1 GB of memory (Banks 1 and 2).

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. For customers who need more memory to support their IP, Banks 3 and 4 can be optionally added for a total of 2 GB of DDR3 SDRAM.

PCI EXPRESS INTERFACE

The Model 78610 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting a PCIe x4 or x8 connection, the interface includes multiple DMA controllers for efficient transfers to and from the module.

READYFLOW

Mercury provides ReadyFlow® BSPs (Board Support Packages) for all Cobalt, Onyx, and Flexor products. Available for both Linux and Windows, these packages:

- Provide a path for quick start-up through application completion
- Allow programming at high, intermediate and low levels to meet various needs
- Are illustrated with numerous examples
- Include complete documentation and definitions of all functions
- Include library and example source code.

ReadyFlow BSPs contain C-language examples that can be used to demonstrate the capabilities of Cobalt, Onyx, and Flexor products. These programming examples will help you get an immediate start on writing your own application. They provide sample code that is known to work, giving you a means of verifying that your board set is operational.

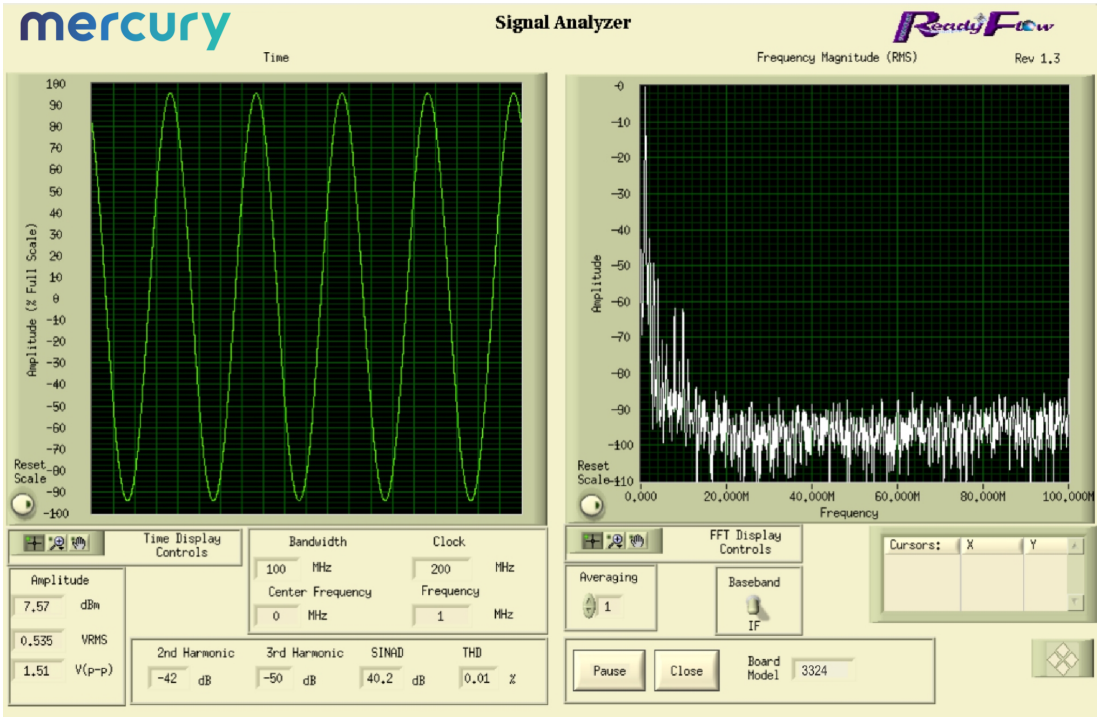
COMMAND LINE INTERFACE

The Command Line Interface provides access to pre-compiled executable examples that operate the hardware right out of the box, without the need to write any code. Board-specific hardware operating arguments can be entered in the command line to control parameters: number of channels to enable, sample clock frequency, data transfer size, reference clock frequency, reference clock source, etc.

The Command Line Interface can be used to call an example application from within a larger user application to control the hardware, and parameter arguments are passed to the application for execution. Functions that control data acquisition automatically save captured data to a pre-named host file or are routed to the Signal Analyzer example function for display.

SIGNAL ANALYZER

When used with the Command Line Interface, the Signal Analyzer allows users to immediately start acquiring and displaying A/D data. A full-featured analysis tool, the Signal Analyzer displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD, and SINAD. Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals.



GATEFLOW

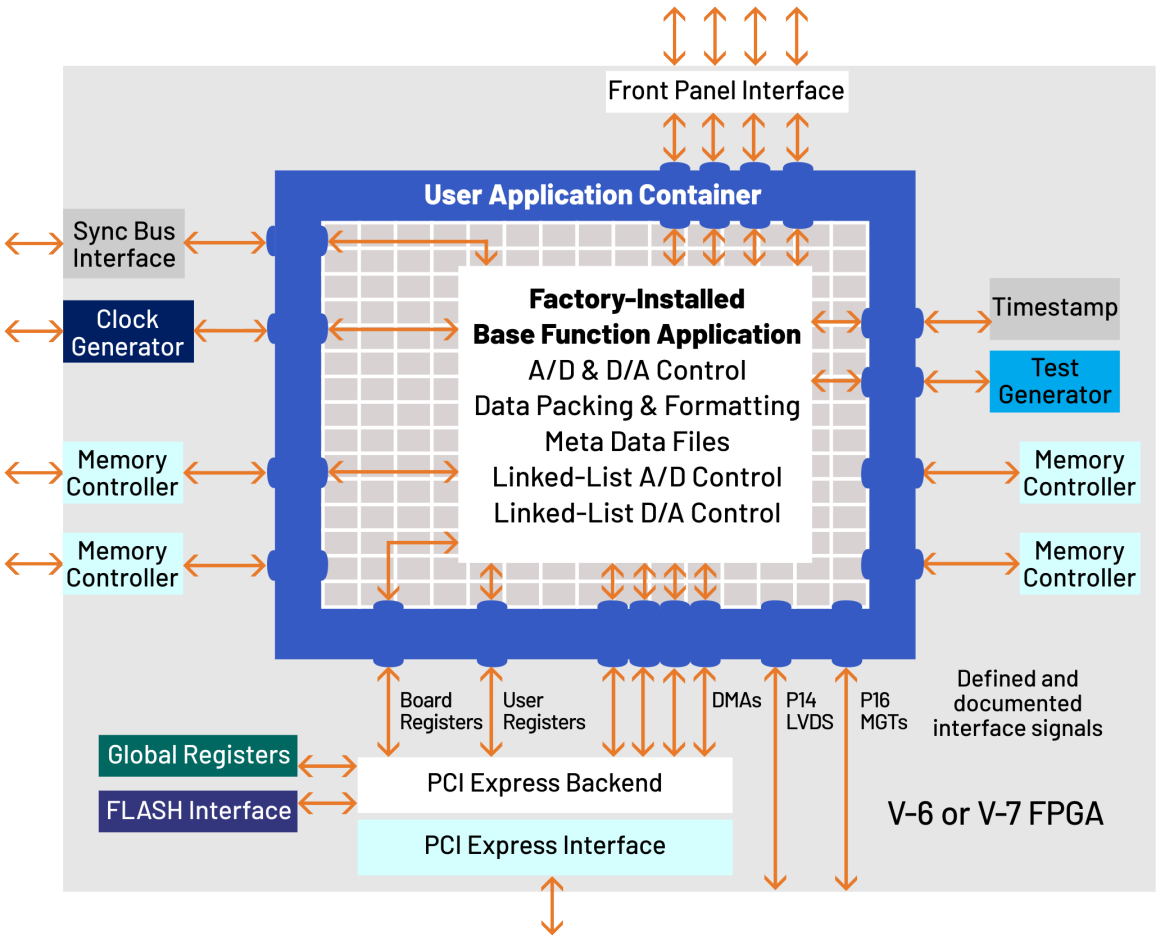
The GateFlow® FPGA Design Kit (FDK) allows the user to modify, replace and extend the standard installed functions in the FPGA to incorporate special modes of operation, new control structures, and specialized signal-processing algorithms.

The Cobalt (Virtex-6), Onyx (Virtex-7), and Flexor (Virtex-7) architectures configure the FPGA with standard factory-supplied interfaces including memory controllers, DMA engines, A/D and D/A interfaces, timing and synchronization structures, triggering and gating logic, time stamping and header tagging, data formatting engines, and the PCIe interface. These resources are connected to the User Application Container using well-defined ports that present easy-to-use data and control signals, effectively abstracting the lower-level details of the hardware.

The User Application Container

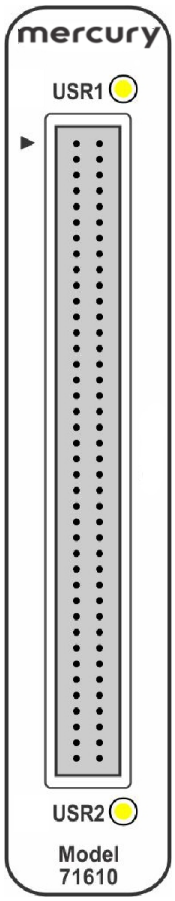
Shown below is the FPGA block diagram of a typical Cobalt, Onyx or Flexor module. The User Application Container holds a collection of different installed IP modules connected to the various interfaces through the standard ports surrounding the container. The specific IP modules for each product are described in further detail in the datasheet of that product.

The GateFlow FDK provides a complete Xilinx's ISE or Vivado project folder containing all the files necessary for the FPGA developer to recompile the entire project with or without any required changes. VHDL source code for each IP module provides excellent examples of how the IP modules work, how they might be modified, and how they might be replaced with custom IP to implement a specific function.



FRONT PANEL CONNECTIONS

The XMC front panel provides an 80-pin digital input/output connector. The front panel also includes two LEDs.



- **USR 1 and USR 2 LEDs:** The yellow LEDs indicate Input /Output operating status.

SPECIFICATIONS

Front Panel Analog Signal Inputs

Data Lines: 35 LVDS differential pairs (32 pairs supported in factory-installed functions), 2.5 V compliant

Clock: One LVDS differential pair, 2.5 V compliant

Data Valid: One LVDS differential pair, 2.5 V compliant

Data Suspend: One LVDS differential pair, 2.5 V compliant

Field Programmable Gate Array

- Standard: Xilinx Virtex-6 XC6VLX130T
- Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O

- Option -104: Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- Option -105: Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

Memory

- Standard: Two 512 MB DDR3 SDRAM memory banks (1 and 2), 400 MHz DDR
- Option 165: Two 512 MB DDR3 SDRAM memory banks (3 and 4), 400 MHz DDR

PCI Express Interface

PCI Express Bus: Gen. 1 x4 or x8

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: Half-length PCIe card

- Depth: 181 mm (7.13 in)
- Height: 111 mm (4.38 in) (including PCIe connectors)

Weight: PCIe Carrier: 110 grams (3.9 oz.)

XMC;Module: Approximately 14 oz. (400 grams)

ORDERING INFORMATION

Model	Description
78610	LVDS Digital I/O with Virtex-6 FPGA - PCIe

Options	Description
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
-702	Air-cooled, Level 2
-713	Conduction-cooled, Level 3

*This option is always required. Contact Mercury for compatible option combinations.

FORM FACTORS

Cobalt products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Cobalt Model 71610 XMC (LVDS Digital I/O with Virtex-6 FPGA) has the following variants:

Model	
52610	3U VPX board (single XMC with optical/backplane RF)
57610	6U VPX board (single XMC)
58610	6U VPX board (dual XMC)
71610	XMC module

DEVELOPMENT SYSTEMS

Mercury offers development systems for Cobalt products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Cobalt boards. Please contact Mercury to configure a system that matches your requirements.

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