

# DRF5660

## 3U VPX SOSA Aligned 6-Channel A/D and D/A Board based on the Intel® Agilex™ 9 Direct RF-Series

### Developed in alignment with the SOSA Technical Standard

- High-bandwidth data streaming
- Waveform signal generator
- Communication receiver and transmitter
- 5G transponder
- Analog I/O for digital recording and playback
- Sensor interfaces



**The DRF5660 is a high-performance, SOSA™ aligned 3U Open VPX board based on the Intel Agilex 9 Direct RF-Series.** Six 4 GSPS A/D and six 12 GSPS D/A converters are integrated into the Agilex 9's multiprocessor architecture, creating a multichannel data conversion and processing solution on a single chip. The DRF5660 brings Agilex 9 performance to 3U VPX with a complete system on a board.

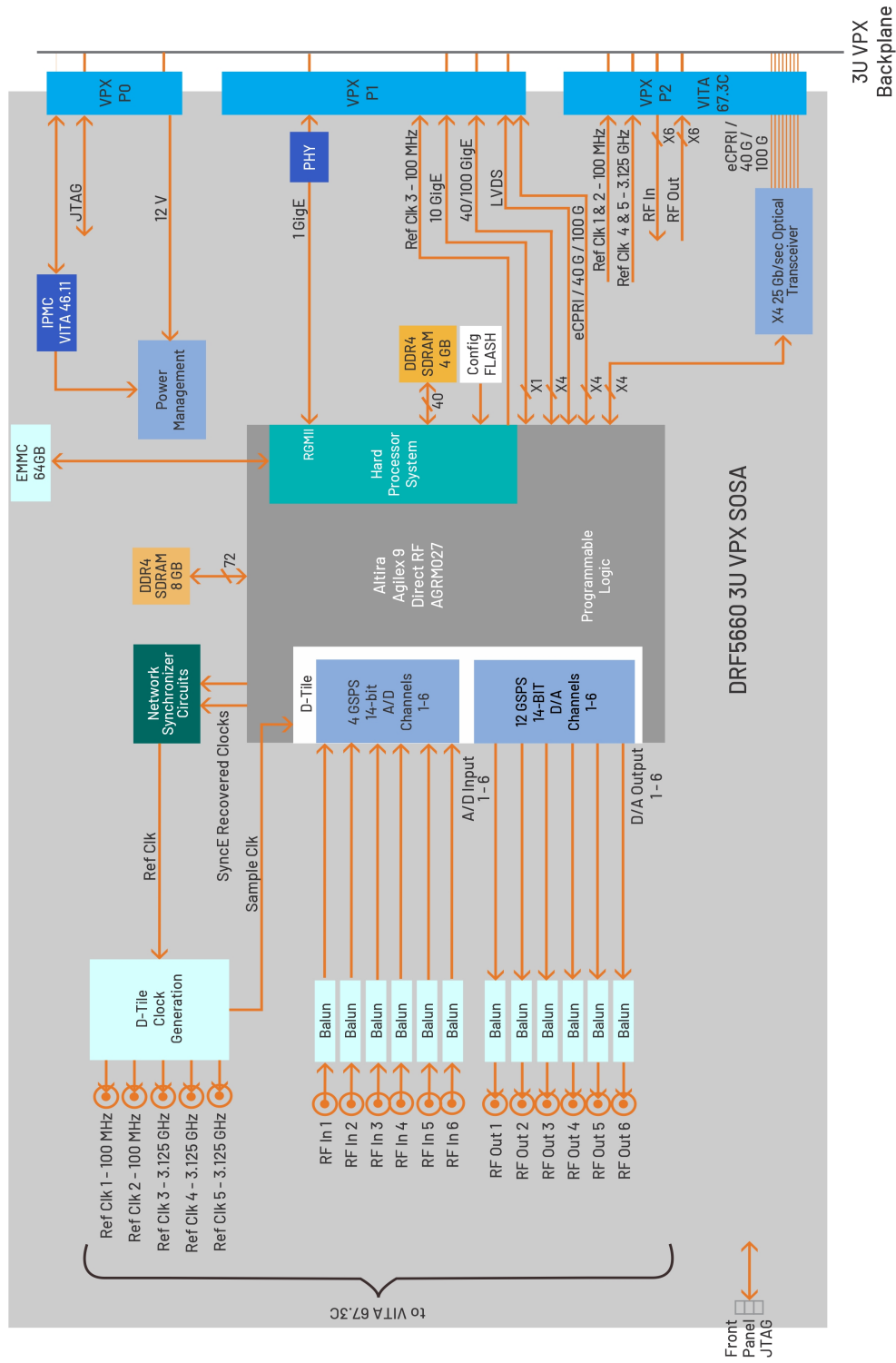
Complementing the Agilex 9's on-chip resources are the DRF5660's 12 GBytes of DDR4, a 10 GigE interface, a 40 GigE interface, two 100G Synchronous Ethernet connections over both optical and copper interfaces, as well as general-purpose serial and parallel signal paths to the FPGA. The DRF5660's sophisticated clocking hardware enables 5G ORAN network applications with eCPRI support and synchronization over SyncE and IEEE-1588.

### FEATURES

- Developed in alignment with the SOSA™ Technical Standard
- Incorporates Intel Agilex 9 Direct RF AGRM027
- 12 GB of DDR4 SDRAM
- 1 GigE Interface
- 10 GigE Interface
- 40 GigE Interface
- Optional VITA 67.3C optical interface for gigabit serial communication
- Dual 100 G synchronous Ethernet interfaces
- Compatible with several VITA standards including: VITA 46, VITA 48, VITA 67.3C, and VITA 65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled
- Board Support Package (BSP) for software development

DRF5660 BLOCK DIAGRAM

Click on a block for more information.



## BOARD ARCHITECTURE

The DRF5660 board design places the Agilex 9 as the cornerstone of the architecture. All control and data paths are accessible by the programmable logic and processing system. A full suite of Mercury-developed IP and software functions utilize this architecture to provide data capture, waveform generation, and interface solutions for many of the most common application requirements.

### A/D CONVERTER STAGE

The analog interface accepts analog RF inputs on six coax connectors located within a VITA 67.3C connector. These inputs are transformer-coupled into the Agilex 9's D-Tile. Inside the Agilex 9, the analog signals are routed to six 4 GSPS, 14-bit A/D converters.

The A/D digital outputs are delivered into the programmable logic and processor system for signal processing, data capture or for routing to other resources.

### D/A CONVERTER STAGE

The Agilex 9's six D/A converters accept baseband real or complex data streams from the FPGA's programmable logic. The analog output of each of the 12 GSPS, 14-bit D/As is transformer-coupled to a coax connection located within a VITA 67.3C connector.

## CLOCKING AND SYNCHRONIZATION

The DRF5660 implements Synchronous Ethernet (SyncE) technology to receive a precise timing reference via the same network connectivity used for data traffic. On board the DRF5660, Network Synchronizer circuits extract low phase noise reference clocks from either of the unit's two 100 G SyncE links. In addition to internal RF sampling clocks of up to 12 GHz, five additional synchronous clock outputs are also produced for use in connected antenna units or other external equipment.

## MEMORY RESOURCES

The DRF5660 architecture supports 8 GBytes of DDR4 SDRAM memory accessible from the Programmable Logic. User-installed IP, together with the Mercury-supplied DDR4 controller core within the FPGA, can take advantage of the memory for custom applications. An additional 4 GByte bank of DDR4 SDRAM is available to the Quad-core ARM Cortex-A53 processor as program memory and storage.

## 1, 10 AND 40/100 GIGE INTERFACE

The DRF5660 includes 1, 10 and 40/100 GigE interfaces for control and data transfers. These interfaces are independent of the optical 100 GigE interfaces. The 1 GigE interface provides a direct connection to the ARM processor.

### EXPANDABLE I/O

The DRF5660 supports four 25 Gb/sec full duplex optical lanes to the VITA 67.3C connector. An additional four 25 Gb/sec full duplex copper lanes are also available on the VPX P1 expansion plane. These two interfaces can support 100 G Synchronous Ethernet or other protocols, enabling a high-speed data streaming path between boards.

### EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. Mercury's BSP includes the board's core functionality deployed on the FPGA that can be edited using Intel's Quartus® Prime Software.

## SPECIFICATIONS

### Field Programmable Gate Array

Type: Intel Agilex 9 SoC FPGA AGRM027

### Agilex 9 RF Signal Chain

Analog Inputs

- Quantity: 6
- Connector: VITA 67.3C
- Input Type: Transformer-coupled (0.1 to 7.125 GHz)

A/D Converters

- Quantity: 6
- Sampling Rate: 4 GSPS
- Resolution: 14 bits

Analog Outputs

- Quantity: 6
- Connector: VITA 67.3C
- Output Type: Transformer-coupled (0.1 to 6 GHz)

D/A Converters

- Quantity: 6
- Sampling Rate: 12 GSPS
- Resolution: 14 bits

Reference Clock

- Source: Switchable between on-board synthesizer, external source, sync bus (used for multiboard sync)
- Connector Type: VITA 67.3C (for external source)

Gate/Trigger:

- Source: Programmable through software or external source
- Connector Type: VITA 67.3C (for external source)
- Level: LVCMOS

**Hard Processing System**

Quad-core ARM Cortex-A53:

- Quantity: 4
- Speed: Up to 1.2 GHz (~2 speed grade)
- -1 Speed: Up to 1.35 GHz (future availability)

Processor I/O:

- 64 GB eMMC memory module
- Trusted Platform Module (TPM)
- Clock Programming Interfaces
- Interface: 1 GigE, UART

**FPGA I/O**

Interface: AISG RS485 and LVDS

- Quantity: 1 Pair
- Type: RS485 and LVDS
- Location: VPX-P1

Interface: 1 PPS

- Type: LVDS
- Location: VPX-P1

Interface: SYSREF Request

- Type: LVDS
- Location: VPX-P1

Interface: 10 GigE

- Location: VPX-P1

Interface: 40 GigE (100 GigE capable)

- Location: VPX-P1
- Quantity: 4 full duplex lanes

Interface: 100 GigE

- Location: VPX-P1
- Quantity: 4 full duplex lanes

Interface: Optical

- Quantity: 4 full duplex lanes
- Connector: VITA 67.3C
- Speed: 25 Gb/sec
- Laser: 850 nm
- Protocol: Factory-installed dual 100 GigE UDP IP cores provides greater than 24 GB/sec data transfers, other protocols supported with user installed IP

**JTAG**

Location: VPX-P0 or front panel

**Memory**

- Type: DDR4 SDRAM
- Quantity: 8 GB, 40 bit
- Size: (each bank) 8 GB; 72-bit FPGA

FPGA Configuration FLASH:

- Type: QSPI NOR Flash
- Size: 2 x 1 Gbit
- 64 GB eMMC Memory

**Environmental**

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

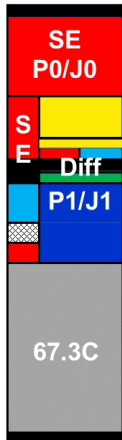
Dimensions: VPX board

- Depth: 170.61 mm (6.717 in)
- Height: 100 mm (3.937 in)
- Weight: Approximately 14 oz (400 grams)

**OpenVPX Compatibility**

The DRF5660 is compatible with the following module profile, as defined by the VITA 65 OpenVPX Specification:

SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-12



**ORDERING INFORMATION**

Model	Description
DRF5660	3U VPX SOSA aligned 6-channel A/D and D/A board with Intel Agilex™ 9 Direct RF



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