Jade 54851

2-channel 500 MHz A/D with DDC, 2-channel 800 MHz D/A 3U VPX board with Kintex UltraScale FPGA

Complete radar and software radio interface solution

- Radar and communication receiver and transmitter
- Electronic Warfare transponder
- Waveform signal generator
- Wideband data acquisition
- Remote monitoring
- Sensor interfaces

The Jade® 54851 is a 2-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

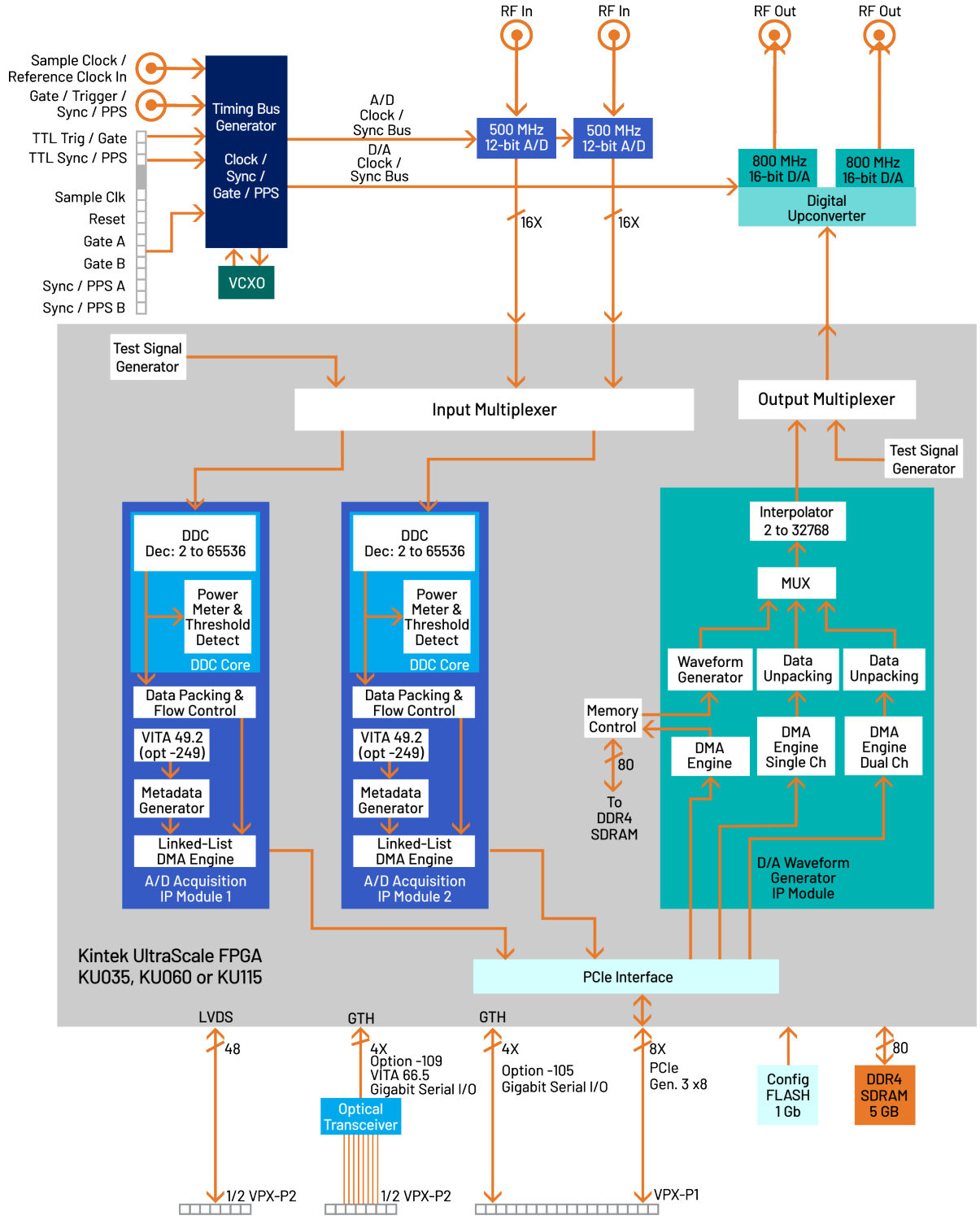
It includes two A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, two DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the 54851 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

FEATURES

- Xilinx® Kintex® UltraScale™ FPGA
- Supports VITA-49.2 VITA Radio Transport standard
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- One DUC (digital converter)
- Two 800 MHz 16-bit D/As
- 5 GB of 2400 MHz DDR4 SDRAM
- Sample clock synchronization to an an external reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express interface (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS port and gigabit serial connections for custom FPGA I/O
- Compatible with VITA-46, VITA-48 and VITA-65 (OpenVPX™ Specification)
- Optional 400 MHz 14-bit A/Ds
- Ruggedized and conduction-cooled versions
- Navigator Design Suite for software and custom IP development

54851 BLOCK DIAGRAM

Click on a block for more information.



54851 BLOCK DIAGRAM

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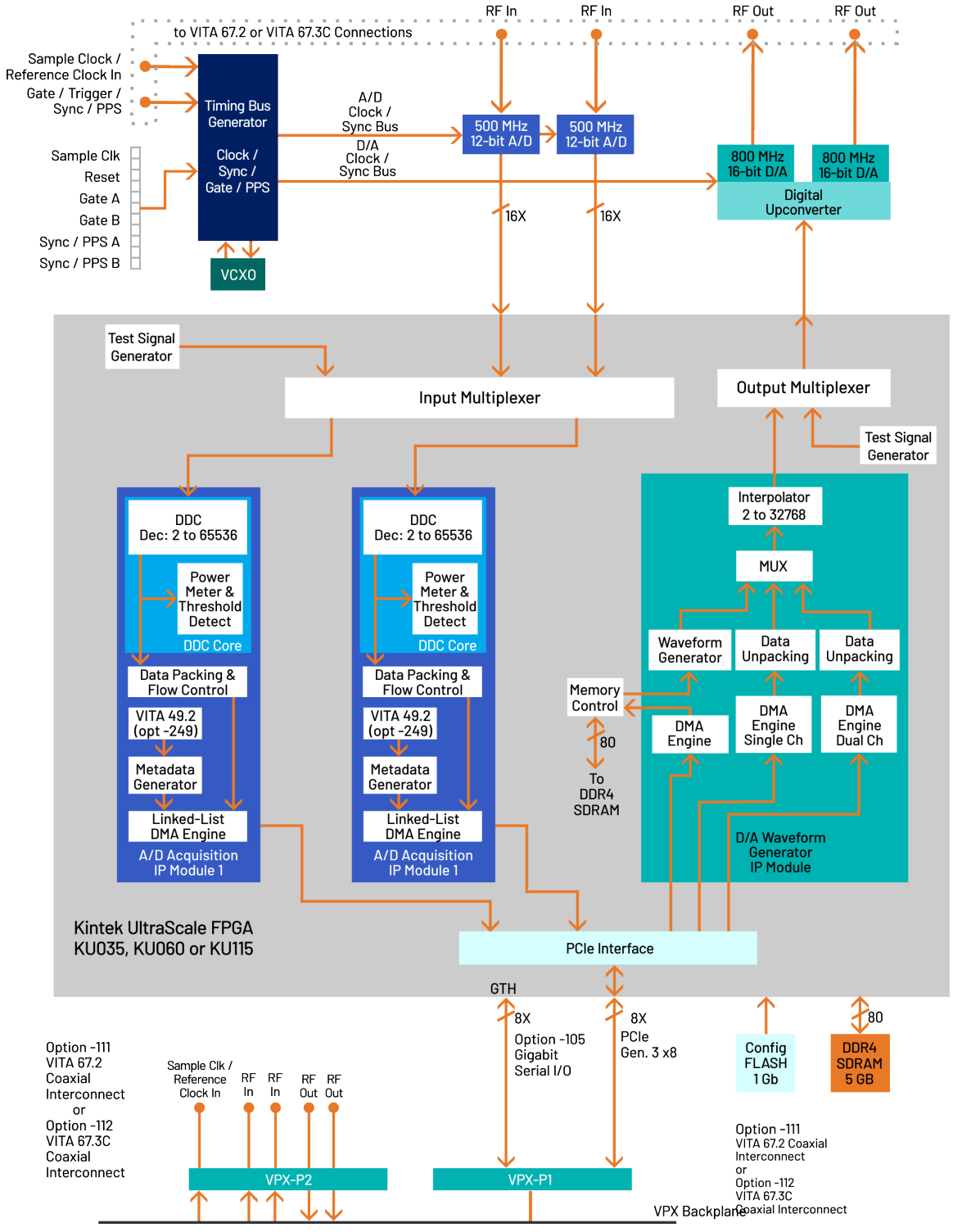


THE JADE ARCHITECTURE

Evolved from the proven designs of Mercury's Cobalt® and Onyx® families, Jade® raises the processing performance while lowering the overall power requirements by building on the Xilinx family of Kintex UltraScale FPGAs. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions as well as providing an ideal platform for user-created intellectual property (IP).

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces.

XILINX KINTEX ULTRASCALE FPGAS

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs: KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

A/D CONVERTER STAGE

The board's analog interface accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters. Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be factory-installed instead of the ADS5463. The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other module resources.

A/D ACQUISITION IP MODULES

The 54851 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP CORES

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*fs/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of fs/N.

D/A WAVEFORM PLAYBACK IP MODULE

The 54851 factory-installed functions include a sophisticated D/A Waveform Playback IP module. It allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

VITA 49.2 RADIO TRANSPORT STANDARD

VITA 49.2 is a data transport protocol for conveying digitized signal information among signal acquisition/generation and processing elements in a communication, radar or similar system. The 54851 implements the VITA 49 packet format for the ADC/DDC data being transferred to the host memory via DMA.

VITA 49.2 packet elements always supported are:

- Signal Data Packet Type
- Stream Identifier
- Integer Seconds Timestamp
- Fractions Seconds Timestamp
- Trailer

Programmable elements are:

- Packet Size
- Stream Identifier
- Trailer

The Timestamp is automatically inserted from the metadata engine. After initialization an externally applied 1 PPS pulse will increment the Integer Seconds Timestamp. A division of the sample clock will increment the fractional seconds timestamp and this count is reset by the 1 PPS pulse.

VITA 49 packets sent via DMA to the DAC/DUC for output will have the header, stream ID, timestamp and trailer removed leaving only the signal data to be transmitted.

DIGITAL UPCONVERTER AND D/A STAGE

A Texas Instruments DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

CLOCKING AND SYNCHRONIZATION

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

MEMORY RESOURCES

The 54851 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Mercury-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI EXPRESS INTERFACE

The 54851 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

VPX-P2 INTERFACE OPTIONS

When purchased with option -110, the 54851 supports the emerging VITA 66.5 standard and provides four optical duplex lanes to a mating VITA 66.5 backplane connector. With the installation of a serial protocol like 10 or 40 Gigabit Ethernet in the FPGA, the VITA 66.5 interface enables high bandwidth communications between boards or chassis independent of the PCIe interface.

Options -111 and -112 provide analog signal routing through the VPX backplane. Both options replace front panel connectors for RF In, RF Out, Sample Clock/ Reference Clock In and Gate/Trigger/ Sync/PPS In with coax signals that pass through the backplane for connections to other boards or chassis. Option -111 is compatible with VITA 67.2 and option -112 is compatible with VITA 67.3C.

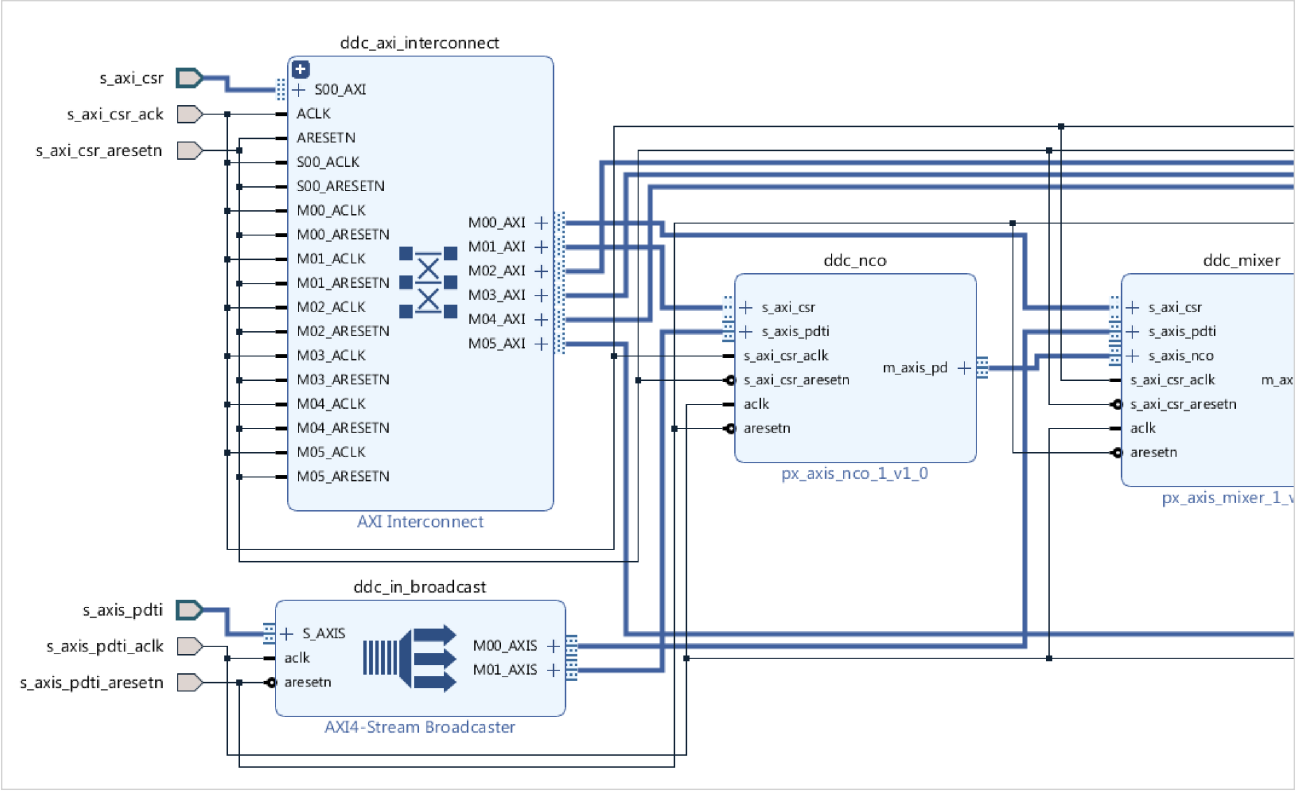
NAVIGATOR DESIGN SUITE

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into the factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

The **Navigator FPGA Design Kit (FDK)** for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Jade product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Jade design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations.

Navigator FDK includes an IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.

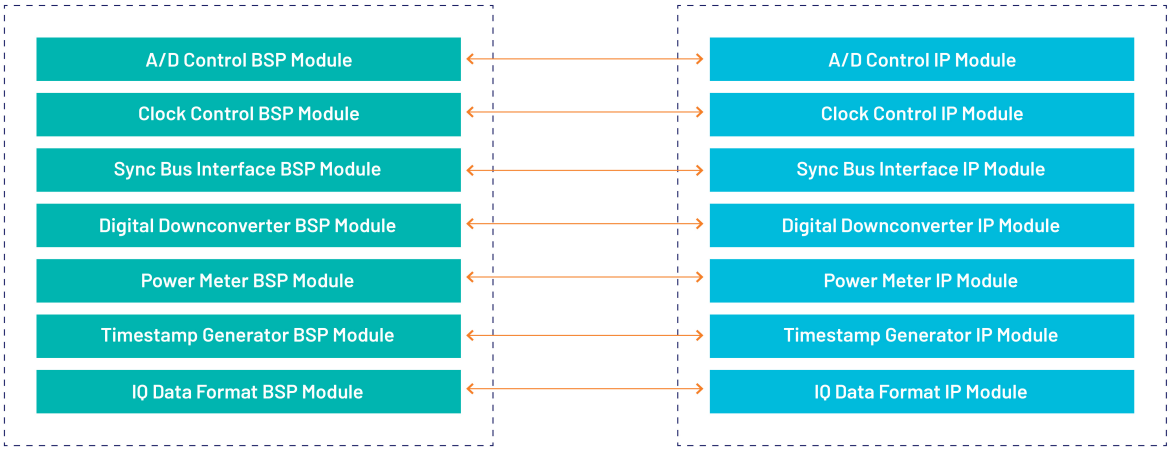
The **Navigator Board Support Package (BSP)** provides software support for Jade boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA. The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.



Navigator IP FPGA Design viewed in IP Integrator

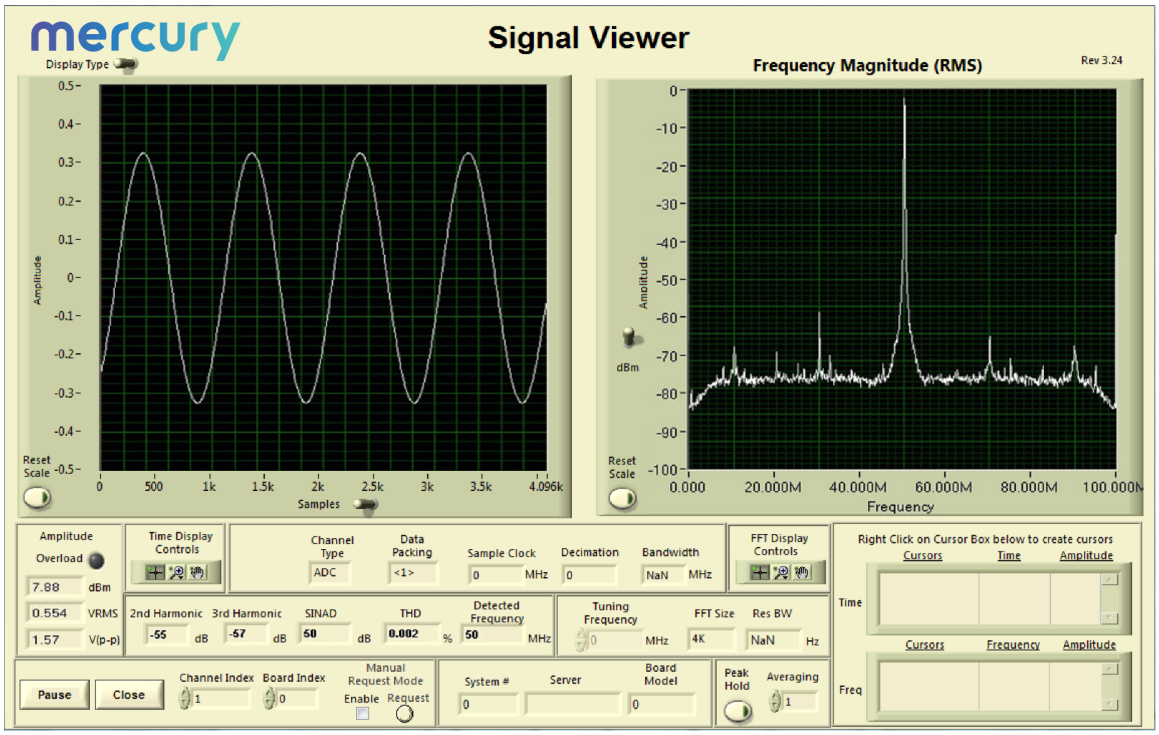
NAVIGATOR BOARD SUPPORT PACKAGE

NAVIGATOR FPGA DESIGN KIT



Because all Jade boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the **Signal Viewer**, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Jade board and Navigator BSP and start viewing analog signals immediately.



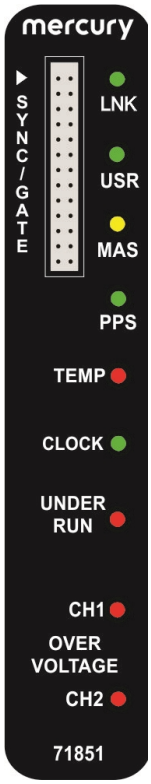
FRONT PANEL CONNECTIONS

The front panel includes six SSMC coaxial connectors for clock, PPS, and analog/digital input signals, and a 26-pin Sync Bus input/output connector. The front panel also includes nine LEDs.

- **Sync Bus Connector:** The 26-pin µSync connector, labeled **SYNC/GATE**, provides clock, sync, and gate input/output pins for the Low-Voltage Positive Emitter-Coupled Logic (LVPECL) Sync Bus.
- **Link LED:** The green **LNK** LED indicates the link speed when a valid link has been established over the PCIe interface, as follows: Gen 1 - LED blinks slowly (less than once per second); Gen 2 - LED blinks about once per second; Gen 3 - LED will be constantly on.
- **User LED:** The green **USR** LED is for user applications.
- **Master LED:** The yellow MAS LED illuminates when the 54851 is the Sync Bus Master. When only a single 54851 is used, it must be a Master.
- **PPS LED:** The green **PPS** LED illuminates when a valid PPS signal is detected. The LED will blink at the rate of the PPS signal.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature voltage sensors on the PCB.
- **Clock LED:** The green **CLK** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.
- **Clock Input Connector:** One SSMC coaxial connector, labeled **CLK**, for input of an external sample clock.
- **Trigger Input Connector:** One SSMC coaxial connector, labeled **TRIG**, for input of an external trigger.
- **Analog Output Connectors:** Two SSMC coaxial connectors, labeled **OUT 1** and **OUT 2**: one for each DAC5688 output channel.
- **Analog Input Connectors:** Two SSMC coaxial connectors, labeled **IN 1** and **IN 2**: one for each ADC input channel.
- **DAC Underrun LED:** One red underrun **UR** LED for the D/A output. This LED illuminates when the DAC5688 FIFO is out of data.
- **ADC Overload LEDs:** There are two red **OV** (overload) LEDs: one for each A/D input. Each LED indicates either an analog input overload in the associated ADS5463 (or ADS5474), or an ADC FIFO overrun.

FRONT PANEL CONNECTIONS: OPTIONS -111 AND -112

The front panel includes a 26-pin Sync Bus connector for input/output of timing and analog signals. The front panel also includes ten LEDs. See VPX P2 for RF and clock signals.



- **Sync Bus Connector:** The 26-pin front panel connector, labeled **SYNC/GATE**, provides clock, sync, and gate input/output pins for the LVPECL Sync Bus.
- **Link LED:** The green **LNK** LED blinks when a valid link has been established over the PCIe interface.
- **User LED:** The green **USR** LED is for user applications.
- **Master LED:** The yellow **MAS** LED illuminates when this is the Sync Bus Master. When only a single model is used, it must be a Master.
- **PPS LED:** The green **PPS** LED illuminates when a valid PPS signal is detected. The LED will blink at the rate of the PPS signal.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the PCB.
- **Clock LED:** The green **CLK** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.
- **D/A Underrun LED:** There is one red **UR** (underrun) LED for the D/A output. This LED illuminates when the DAC5688 FIFO is out of data.
- **CH LEDs:** There are two red **CH1** and **CH2** LEDs: one for each A/D input. Each LED indicates either an analog input overload in the associated ADS5485, or an A/D FIFO overrun.

SPECIFICATIONS

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +5 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard)

Type: Texas Instruments ADS5463

Sampling Rate: 20 MHz to 500 MHz

Resolution: 12 bits

A/D Converters (option -014)

Type: Texas Instruments ADS5474

Sampling Rate: 20 MHz to 400 MHz

Resolution: 14 bits

Digital Downconverters

Quantity: Two channels

Decimation Range: 2x to 65,536x in three stages of 2x to 32x and one fixed stage of 2x

LO Tuning Freq. Resolution: 32 bits, 0 to f_s

LO SFDR: >120 dB

Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: 16-bit coefficients, 24-bit output, user-programmable coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters

Type: Texas Instruments DAC5688

Input Data Rate: 250 MHz max.

Output IF: DC to 400 MHz max.

Output Signal: 2-channel real or 1-channel with frequency translation

Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation

Resolution: 16 bits

Digital Interpolator Core

Interpolation Range: 2x to 32,768x in one stage of 2x to 256x and one stage of 2x to 128x

Total Interpolation Range (D/A and interpolator core combined)

2x to 262,144x

Front Panel Analog Signal Outputs

Output: Transformer-coupled, front panel female SSMC connectors

Transformer: Coil Craft WBC4-6TLB

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources

On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 3, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus

26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Kintex UltraScale XCKU035-2

- Option -084: Xilinx Kintex UltraScale XCKU060-2
- Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O

Option -104: provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O (not available with options -111 and -112)

Option -105: provides an 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols (gigabit link to 4X when combined with option -110).

Option -110: VITA 66.5 interface provides optical 4X duplex lanes

Option -111: VITA 67.2: RF In, RF Out, Sample Clock/Reference Clock In and Gate/Trigger/Sync/PPS In

Option -112: VITA 67.3C: RF In, RF Out, Sample Clock/Reference Clock In and Gate/Trigger/Sync/PPS In

Memory

Type: DDR4 SDRAM

Size: 5 GB

Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: VPX board

- Depth: 170.61 mm (6.717 in)
- Height: 100 mm (3.937 in)

Weight: Approximately 14 oz (400 grams)

ORDERING INFORMATION

Model	Description
54851	2-channel 500 MHz A/D with DDC, 2-channel 800 MHz D/A 3U VPX board with Kintex UltraScale FPGA

Options:	
-014	400 MHz, 14-bit A/Ds
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O
-110	VITA 66.5 optical interface
-111	VITA 67.2: RF In, RF Out and Sample Clock/Reference Clock In
-112	VITA 67.3C: RF In, RF Out and Sample Clock/Reference Clock In
-249	VITA 49-2 support
-702	Air-cooled, Level 2
-763	Conduction-cooled, Level 3

Contact Mercury for compatible option combinations and complete specifications of rugged and conduction-cooled versions. Options may change, so be sure to contact Mercury for the latest information.

ACCESSORY PRODUCTS

Model	Description
2171	Cable Kit: SSMC to SMA

DEVELOPMENT SYSTEMS

Mercury offers development systems for Jade products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Jade boards. Please contact Mercury to configure a system that matches your requirements.

FORM FACTORS

Jade products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Jade Model 71851 XMC (2-Channel 500 MHz A/D with DDC and 2-Channel 800 MHz D/A with DUC, Kintex UltraScale FPGA) has the following variants:

Model	
52851	3U VPX board (single XMC)
54851	3U VPX board (single XMC with optical/backplane RF)
57851	6U VPX board (single XMC)
58851	6U VPX board (dual XMC)
71851	XMC module
78851	PCIe board (single XMC)

LIFETIME SUPPORT FOR JADE PRODUCTS

Mercury offers worldwide customers shorter development time, reliable, rugged solutions for a variety of environments, reduced costs, and mature software development tools. We offer free lifetime support from our engineering staff, which customers can depend on through phone and email, as well as software updates. Take advantage of our 40 years of experience in delivering high-performance radar, communications, SIGINT, EW, and data acquisition MIL-Aero solutions worldwide.

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