# Cobalt 52663

## 1100-channel GSM channelizer with quad A/D 3U VPX board with Virtex-6 FPGA

**Complete GSM channelizer with analog IF interface**

- Four 180 MHz 16-bit A/Ds
- Two banks of 375 DDCs for upper GSM
- Two banks of 175 DDCs for lower GSM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization

**The 52663 is a four-channel, high-speed A/D converter with 1100 GSM DDCs (digital downconverters). It accepts IF signals from an RF tuner.** It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

The 52663 includes four A/Ds and four banks of DDCs. Channelizer data and control signals flow across the PCI Express Gen. 2 native interface, providing peak rates of up to 2 GB/sec.

### THE COBALT ARCHITECTURE

The Cobalt® Architecture connects all of the board's data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four DMA controllers, PCIe interface, gating, and triggering.

The 52663 is a complete, full-featured subsystem, ready to use with no additional FPGA development required.

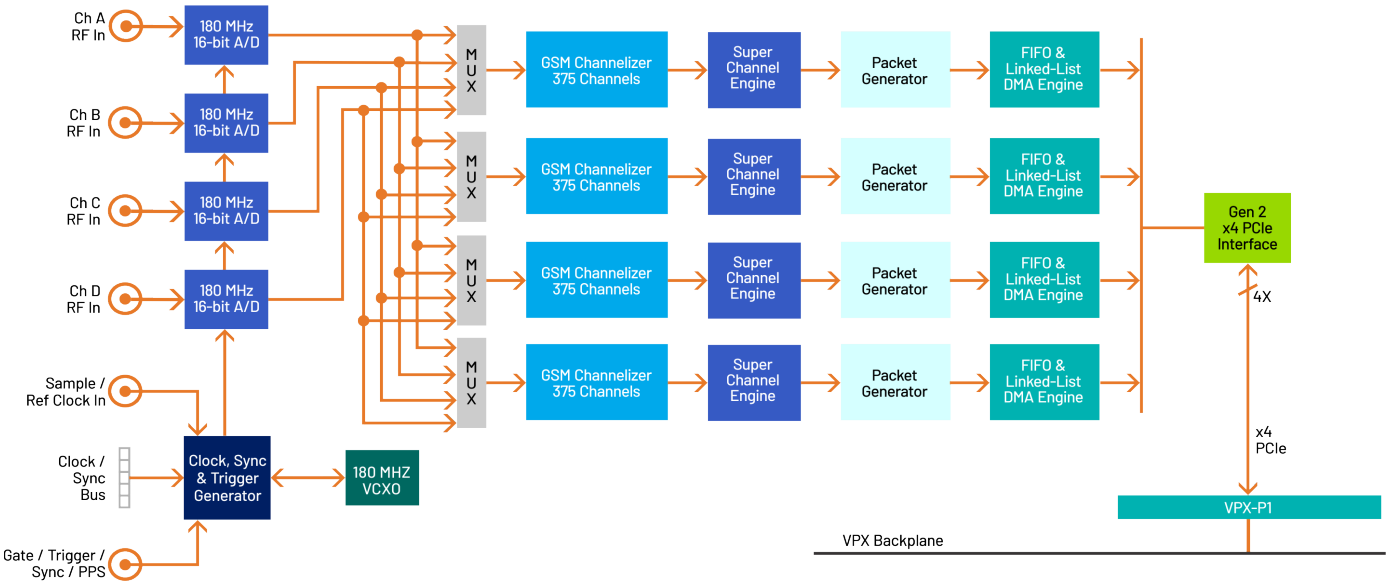
### A/D CONVERTER STAGE

The board's analog interface accepts four analog IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

## 52663 BLOCK DIAGRAM

Click on a block for more information.




## CLOCKING AND SYNCHRONIZATION

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator accepts an external 180 MHz sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52663's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

## GSM CHANNELIZER CORES

The 52663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers.

The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to the 71663, these GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the 52663 A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must ensure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, thereby producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

### CHANNELIZER OUTPUT FORMATTING

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 4 GB/sec peak rate of PCIe Gen 2 x8 interface.

To mitigate this situation, every four DDC channels are frequency-mutliplexed into a single “superchannel”. This is allowed because of the 4x oversampling, and results in a reduction of the aggregate PCIe traffic by a factor of 4 to 2.383 GB/sec, which is now well within the capability of the PCIe Gen 2 x8 interface.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bit I + 26-bit Q.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank contains only three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across PCIe. There are four superchannel mask words, one for each bank.

### SUPERCHANNEL PACKETS AND HEADERS

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data “payload” samples can be identified and recovered by the host.

### PCI EXPRESS INTERFACE

Model 52663 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x4, the interface includes four DMA controllers for efficient packet transfers from each of the four DDC banks to system memory.

The PCIe interface is also used as the programming interface for all status and control between the 52663 and host.

## READYFLOW

Mercury provides ReadyFlow® BSPs (Board Support Packages) for all Cobalt, Onyx, and Flexor products. Available for both Linux and Windows, these packages:

- Provide a path for quick start-up through application completion
- Allow programming at high, intermediate and low levels to meet various needs
- Are illustrated with numerous examples
- Include complete documentation and definitions of all functions
- Include library and example source code.

ReadyFlow BSPs contain C-language examples that can be used to demonstrate the capabilities of Cobalt, Onyx, and Flexor products. These programming examples will help you get an immediate start on writing your own application. They provide sample code that is known to work, giving you a means of verifying that your board set is operational.

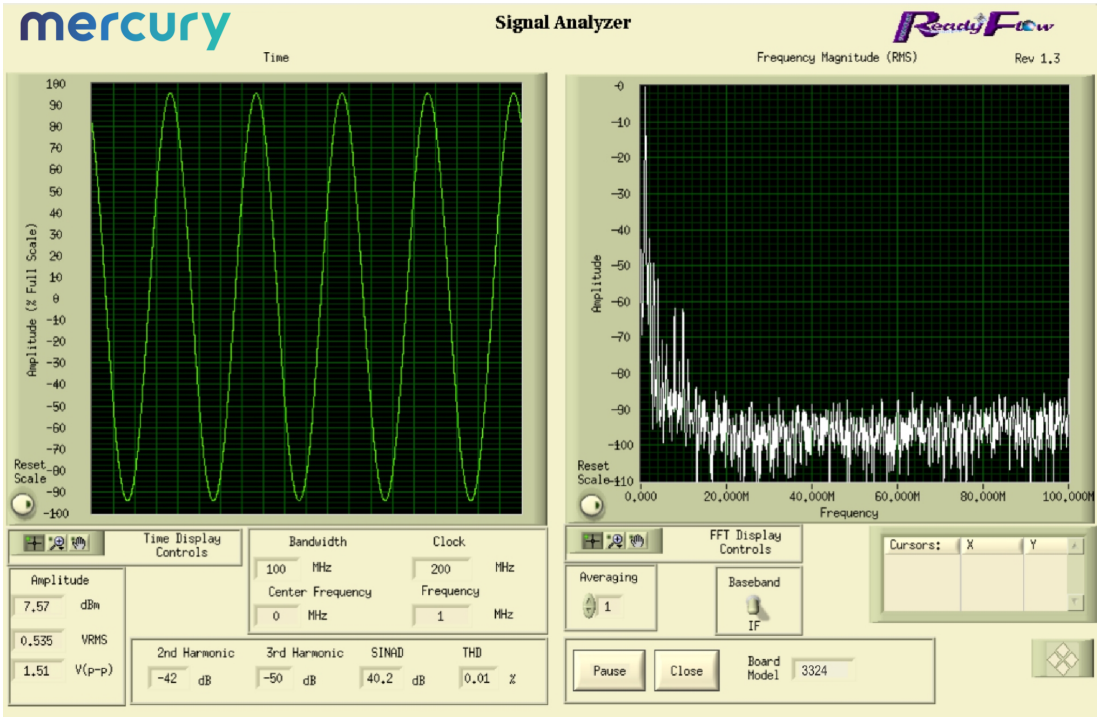
## COMMAND LINE INTERFACE

The Command Line Interface provides access to pre-compiled executable examples that operate the hardware right out of the box, without the need to write any code. Board-specific hardware operating arguments can be entered in the command line to control parameters: number of channels to enable, sample clock frequency, data transfer size, reference clock frequency, reference clock source, etc.

The Command Line Interface can be used to call an example application from within a larger user application to control the hardware, and parameter arguments are passed to the application for execution. Functions that control data acquisition automatically save captured data to a pre-named host file or are routed to the Signal Analyzer example function for display.

## SIGNAL ANALYZER

When used with the Command Line Interface, the Signal Analyzer allows users to immediately start acquiring and displaying A/D data. A full-featured analysis tool, the Signal Analyzer displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD, and SINAD. Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals.



## GATEFLOW

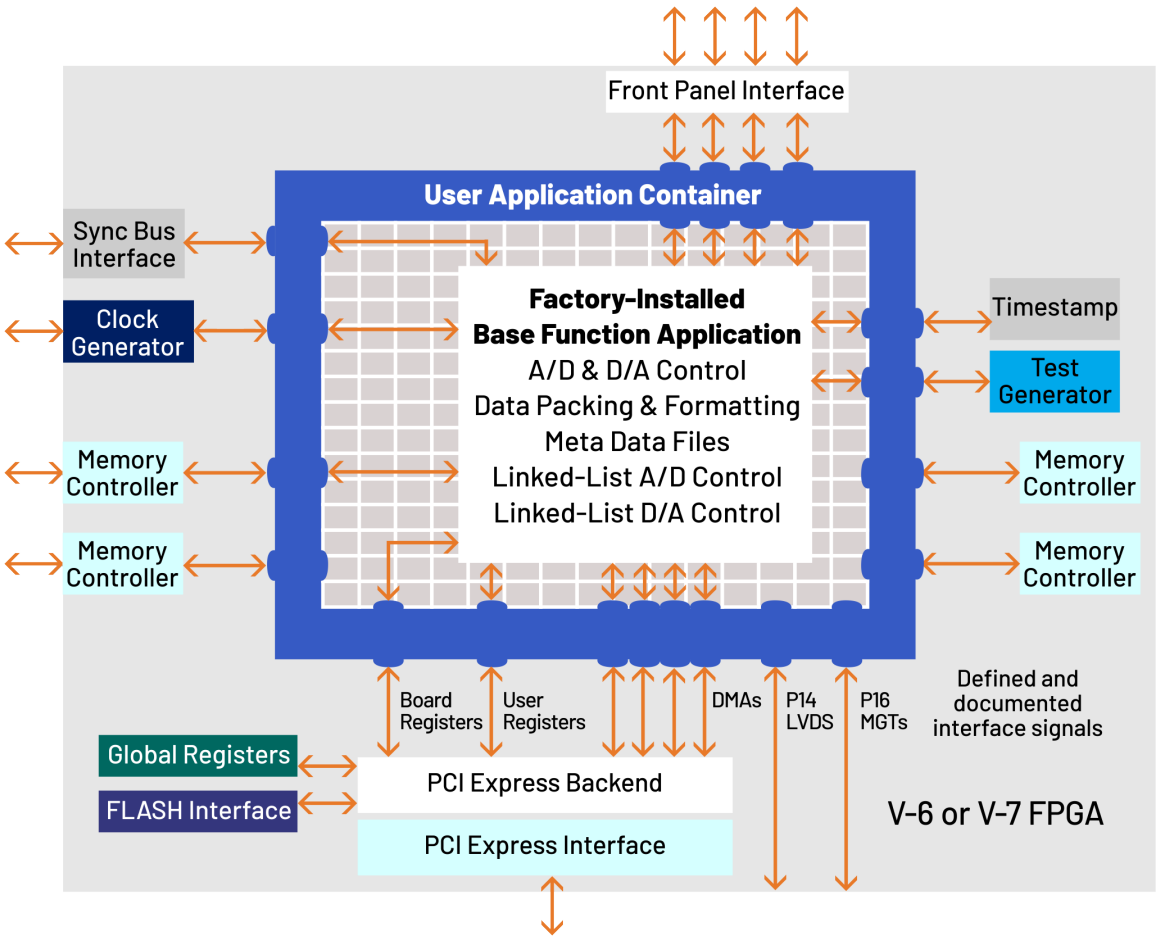
The GateFlow® FPGA Design Kit (FDK) allows the user to modify, replace and extend the standard installed functions in the FPGA to incorporate special modes of operation, new control structures, and specialized signal-processing algorithms.

The Cobalt (Virtex-6), Onyx (Virtex-7), and Flexor (Virtex-7) architectures configure the FPGA with standard factory-supplied interfaces including memory controllers, DMA engines, A/D and D/A interfaces, timing and synchronization structures, triggering and gating logic, time stamping and header tagging, data formatting engines, and the PCIe interface. These resources are connected to the User Application Container using well-defined ports that present easy-to-use data and control signals, effectively abstracting the lower-level details of the hardware.

### The User Application Container

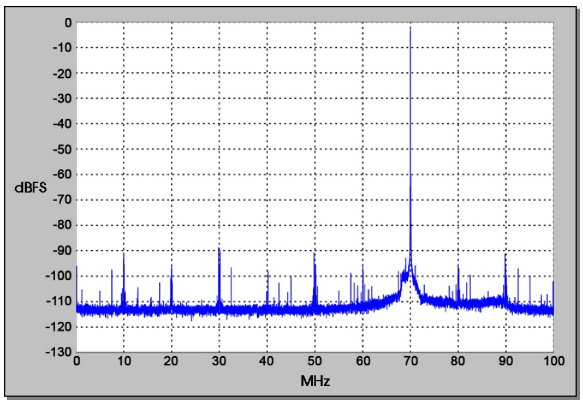
Shown below is the FPGA block diagram of a typical Cobalt, Onyx or Flexor module. The User Application Container holds a collection of different installed IP modules connected to the various interfaces through the standard ports surrounding the container. The specific IP modules for each product are described in further detail in the datasheet of that product.

The GateFlow FDK provides a complete Xilinx's ISE or Vivado project folder containing all the files necessary for the FPGA developer to recompile the entire project with or without any required changes. VHDL source code for each IP module provides excellent examples of how the IP modules work, how they might be modified, and how they might be replaced with custom IP to implement a specific function.



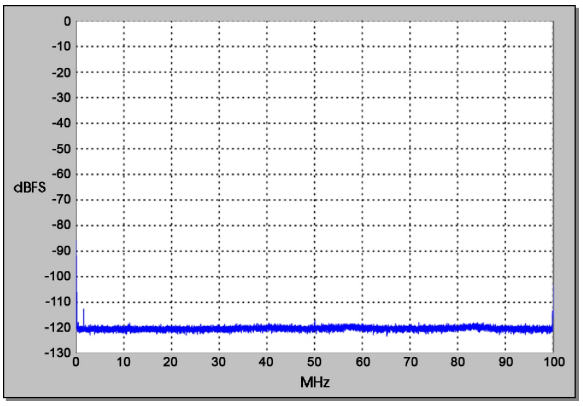
## A/D PERFORMANCE

### Spurious Free Dynamic Range



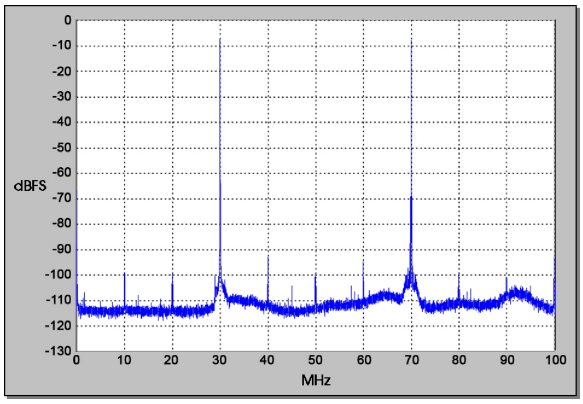

$f_{in}$ = 70 MHz, $f_s$ = 200 MHz, Internal Clock

### Spurious Pick-up



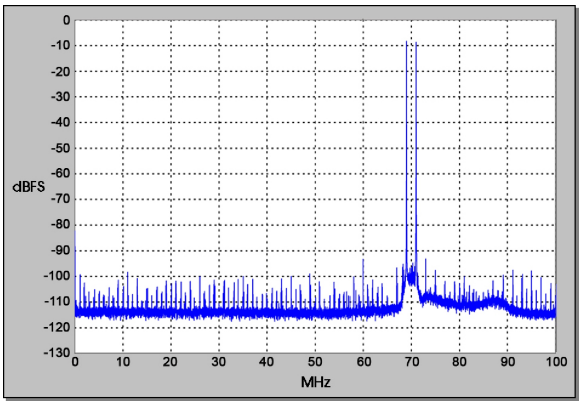

$f_s$ = 200 MHz, Internal Clock

### Two-Tone SFDR



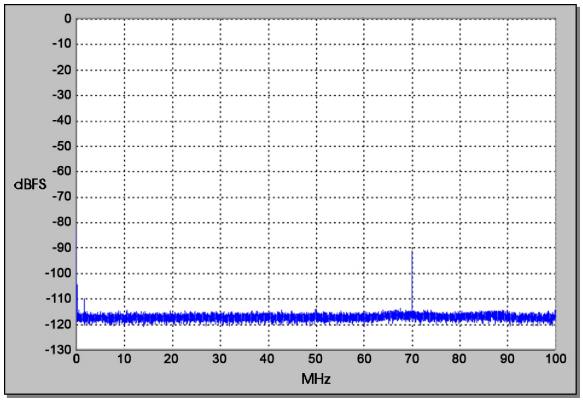

$f_1$ = 30 MHz, $f_2$ = 70 MHz, $f_s$ = 200 MHz

### Two-Tone SFDR



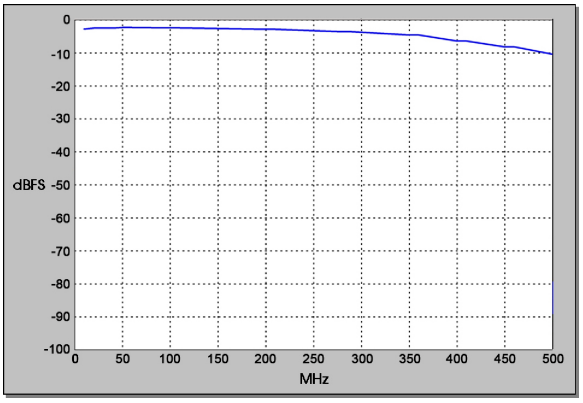

$f_1$ = 69 MHz, $f_2$ = 71 MHz, $f_s$ = 200 MHz

### Adjacent Channel Crosstalk




$f_{in}$ Ch2 = 70 MHz, $f_s$ = 200 MHz, Ch 1 shown

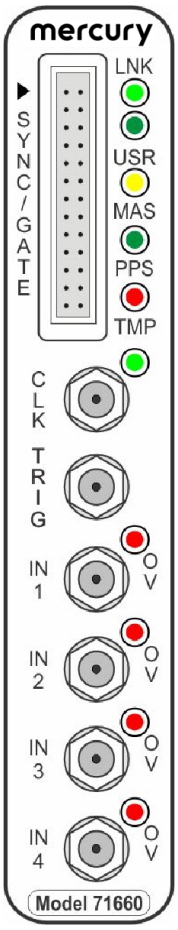
### Input Frequency Response




$f_s$ = 200 MHz, Internal Clock

## FRONT PANEL CONNECTIONS

The XMC front panel includes six SSMC coaxial connectors, and a 26-pin µSync Bus connector for input/output of timing and analog signals. The front panel also includes ten LEDs.




- **Sync Bus Connector:** The 26-pin Sync Bus front panel connector labeled **SYNC/GATE** provides clock, sync and gate input/output pins for the Low-Voltage Positive Emitter-Coupled Logic (LVPECL) Sync Bus. When the board is a bus master, these pins output LVPECL Sync Bus signals to other slave units. When the board is a bus Slave, these pins input LVPECL signals from a bus Master.
- **Link LED:** The green **LNK** LED illuminates when a valid link has been established over the PCIe interface.
- **USR LED:** The green **USR** LED is for user applications.
- **Master LED:** the yellow **MAS** LED illuminates when this board is the Sync Gus Master. When only a single board is used, it must be a Master.
- **PPS LED:** the green **PPS** LED illuminates when a valid PPS sign is detected. The LED will blink at the rate of the PPS signal.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the PCB.
- **Clock LED:** The green **CLK** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.
- **Clock Input Connector:** One SSMC coaxial connector, labeled **CLK** for the input of an external sample clock.
- **Trigger Input Connector:** The front panel has one SSMC coaxial connector, labeled **TRIG**, for input of an external trigger.
- **Analog Input Connectors:** Four SSMC coaxial connector, labeled **IN 1, IN 2, IN 3,** and **IN 4** for analog signal inputs , one for each ADC input channel.
- **ADC Overload LEDs:** There are four red **OV** LEDs, one for each A/D input. Use the applicable ADC Date Control Register to select the signal source for each OV LED, either an overload detection in the associated ADS5485, or an ADC FIFO overrun.

## SPECIFICATIONS

### Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

### A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

### Sample Clock Sources

On-board clock synthesizer

### Clock Synthesizer

Clock Source: Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 10 MHz system reference

### External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference

### Timing Bus

26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/ trigger and sync/PPS inputs

### External Trigger Input

Type: Front panel female SSMC connector, LVTTL

Function: Programmable functions include: trigger, gate, sync and PPS

### GSM Channel Banks

DDCs per bank: two banks of 175 DDCs and two banks of 375 DDCs

Overall bandwidth per bank: 35 MHz & 75 MHz for 175- & 375-channel banks

IF (Center) Freq: 45, 135 or 225 MHz

### DDC Channels

Channel Spacing: 200 kHz, fixed

DDC Center Freqs: IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187

DDC Channel Filter Characteristics

< 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)

> 18 dB attenuation at ±100 kHz

> 78 dB attenuation at ±170 kHz

> 83 dB attenuation at ±600 kHz

> 93 dB attenuation at ±800 KHz

> 96 dB attenuation at > ±3 MHz

DDC Output Rate $f_s$: Resampled to 180 MHz*13/2160 = 1.0833333 MS/sec

DDC Data Output Format: 24 bits I + 24 bits Q

### Superchannels

Content: Four consecutive DDC channels are frequency-offset from each other and then summed together

Frequency Offsets for each DDC:

First: $-f_s/4$ (-270.8333 kHz)

Second: 0 Hz

Third: $+f_s/4$ (+270.8333 kHz)

Fourth: $+f_s/2$ (+541.666 kHz)

Superchannel Sample Rate: $f_s$

Superchannel Output Format: 26 bits I + 26 bits Q

Number of Superchannels per Bank: 175-Channel banks: 44; 375-Channel banks: 94

### Field Programmable Gate Array

Xilinx Virtex-6 XC6VSX315T

### PCI Express Interface

PCI Express Bus: Gen. 2: x8

### Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

### Physical

Dimensions: Standard 3U VPX

- Depth: 170.6 mm (6.717 in.)
- Height: 100 mm (3.94 in.)

Weight: VPX Carrier: 110 grams (3.9 oz.); XMC Module: Approximately 14 oz. (400 grams)

## ORDERING INFORMATION

| Model | Description |
|---|---|
| 52663 | 1100-Channel GSM Channelizer with Quad A/D - VPX |

Contact Mercury for availability of rugged and conduction-cooled versions.

## ACCESSORY PRODUCTS

| Model | Description |
|---|---|
| 2171 | Cable Kit: SSMC to SMA |

## FORM FACTORS

Cobalt products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Cobalt Model 71663 XMC (1100-Channel GSM Channelizer wih Quad A/D) has the following variants:

| Model | |
|---|---|
| 52663 | 3U VPX board (single XMC) |
| 57663 | 6U VPX board (single XMC) |
| 58663 | 6U VPX board (dual XMC) |
| 71663 | XMC module |
| 78663 | PCIe board (single XMC) |

## DEVELOPMENT SYSTEMS

Mercury offers development systems for Cobalt products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Cobalt boards. Please contact Mercury to configure a system that matches your requirements.

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