Cobalt 57690/58690

One or two L-band RF tuners, 2- or 4-channel 200 MHz A/D 6U VPX board with Virtex-6 FPGA

Complete radar and software radio interface solution

- Radar and software radio receiver
- Communications receiver
- Analog signal interface for data recording
- Wideband data acquisition
- Remote monitoring
- Sensor interfaces

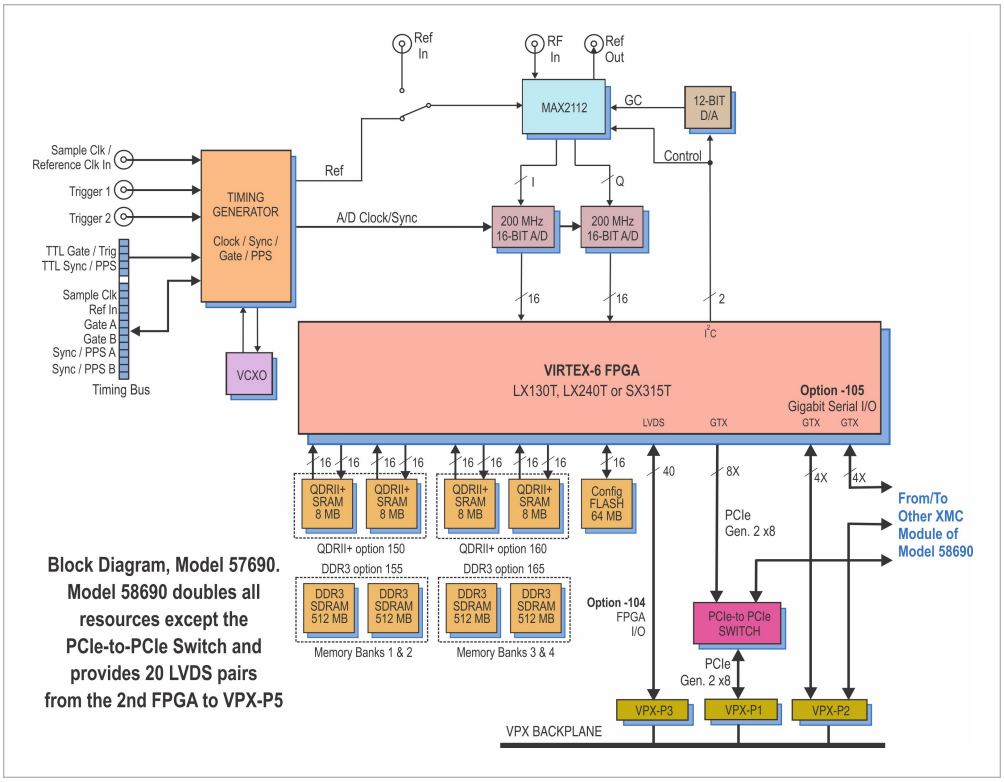
The 57690 and 58690 consist of one or two 71690 XMC modules mounted on a VPX carrier board. The 57690 is a 6U board with one 71690 module while the 58690 is a 6U board with two XMC modules rather than one.

These models include one or two L-Band RF tuners, two or four A/Ds and four or eight banks of memory.

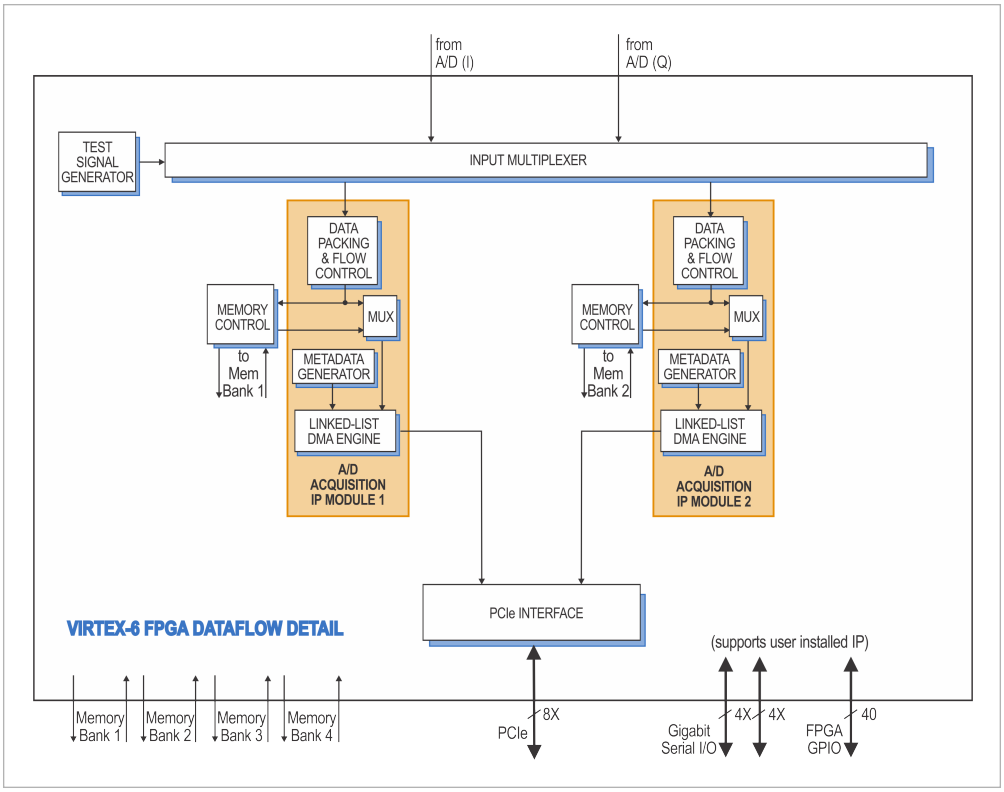
FEATURES

- One or two L-Band tuners accept RF signals from 925 MHz to 2175 MHz
- One or two programmable LNAs boost LNB (low-noise block) antenna signal levels with up to 60 dB gain
- One or two programmable analog downconverters provide I + Q baseband signals with bandwidths ranging from 4 to 40 MHz
- Two or four 200 MHz 16-bit A/Ds
- Supports Xilinx® Virtex®-6 LXT and SXT FPGA
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 MB or 64 MB of QDRII+ SRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

BLOCK DIAGRAMS



Block Diagram, Model 57690. Model 58690 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5



THE COBALT ARCHITECTURE

The Cobalt® Architecture features a Xilinx Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions in these models include two or four A/D acquisition IP modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. The GateFlow FPGA Design Kits include all of the factory-installed modules as document source code. Developers can integrate their own IP with the factory-installed functions or use the GateFlow kit to completely replace the IP with their own.

XILINX VIRTEX-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

A/D CONVERTER STAGES

The analog baseband I and Q analog tuner outputs are then applied to two or four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGAs for signal processing, data capture or for routing to other board resources.

A/D ACQUISITION MODULES

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

A/D CLOCKING AND SYNCHRONIZATION

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/ trigger signals within the module. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave modules, supporting synchronous sampling and sync functions across all connected modules.

MEMORY RESOURCES

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

The factory-installed A/D acquisition modules use memory banks 1 & 2. Banks 3 & 4 can be optionally installed to support custom user-installed IP within the FPGA .

PCI EXPRESS INTERFACE

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

RF TUNER STAGES

One or two front panel SSMC connectors accept L-Band signals between 925 MHz and 2175 MHz from the antenna LNBs (low noise blocks). The Maxim MAX2112 tuners directly convert these L-Band signals to baseband using broadband I/Q downconverters.

The devices include RF variable-gain LNAs (low noise amplifiers), PLL (phase-locked loops) synthesized local oscillators, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizers lock their VCOs to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNAs offer a programmable linear gain range of 60 dB.

The integrated lowpass filters with variable bandwidths provide bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

READYFLOW

Mercury provides ReadyFlow® BSPs (Board Support Packages) for all Cobalt, Onyx, and Flexor products. Available for both Linux and Windows, these packages:

- Provide a path for quick start-up through application completion
- Allow programming at high, intermediate and low levels to meet various needs
- Are illustrated with numerous examples
- Include complete documentation and definitions of all functions
- Include library and example source code.

ReadyFlow BSPs contain C-language examples that can be used to demonstrate the capabilities of Cobalt, Onyx, and Flexor products. These programming examples will help you get an immediate start on writing your own application. They provide sample code that is known to work, giving you a means of verifying that your board set is operational.

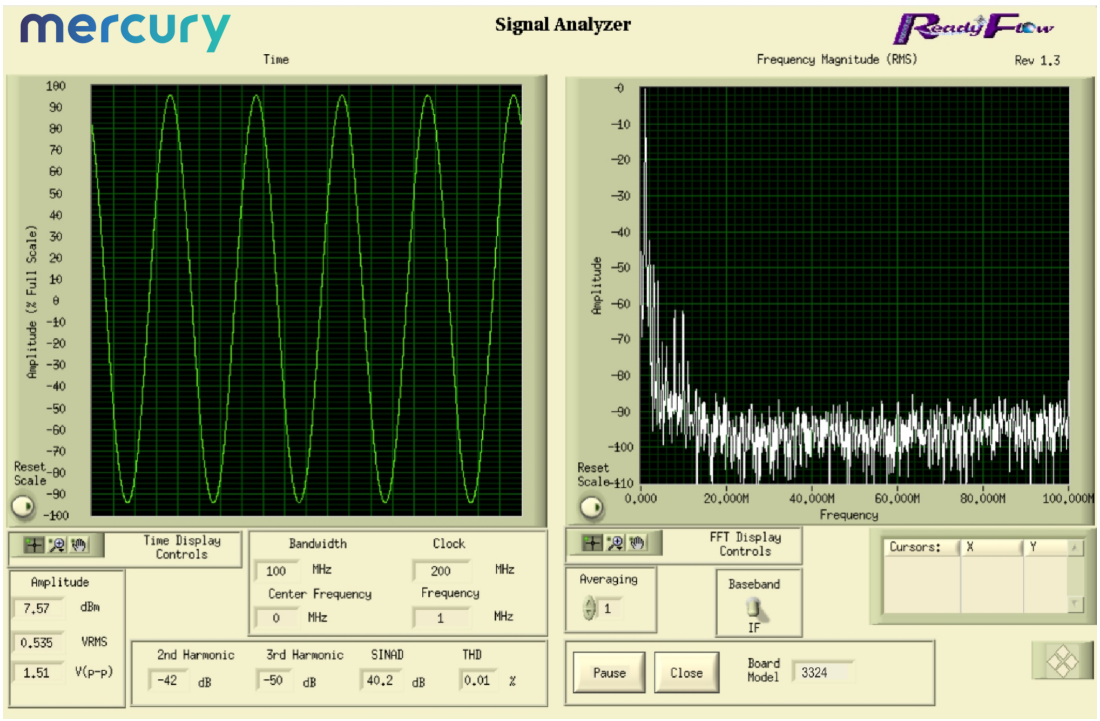
COMMAND LINE INTERFACE

The Command Line Interface provides access to pre-compiled executable examples that operate the hardware right out of the box, without the need to write any code. Board-specific hardware operating arguments can be entered in the command line to control parameters: number of channels to enable, sample clock frequency, data transfer size, reference clock frequency, reference clock source, etc.

The Command Line Interface can be used to call an example application from within a larger user application to control the hardware, and parameter arguments are passed to the application for execution. Functions that control data acquisition automatically save captured data to a pre-named host file or are routed to the Signal Analyzer example function for display.

SIGNAL ANALYZER

When used with the Command Line Interface, the Signal Analyzer allows users to immediately start acquiring and displaying A/D data. A full-featured analysis tool, the Signal Analyzer displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD, and SINAD. Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals.



GATEFLOW

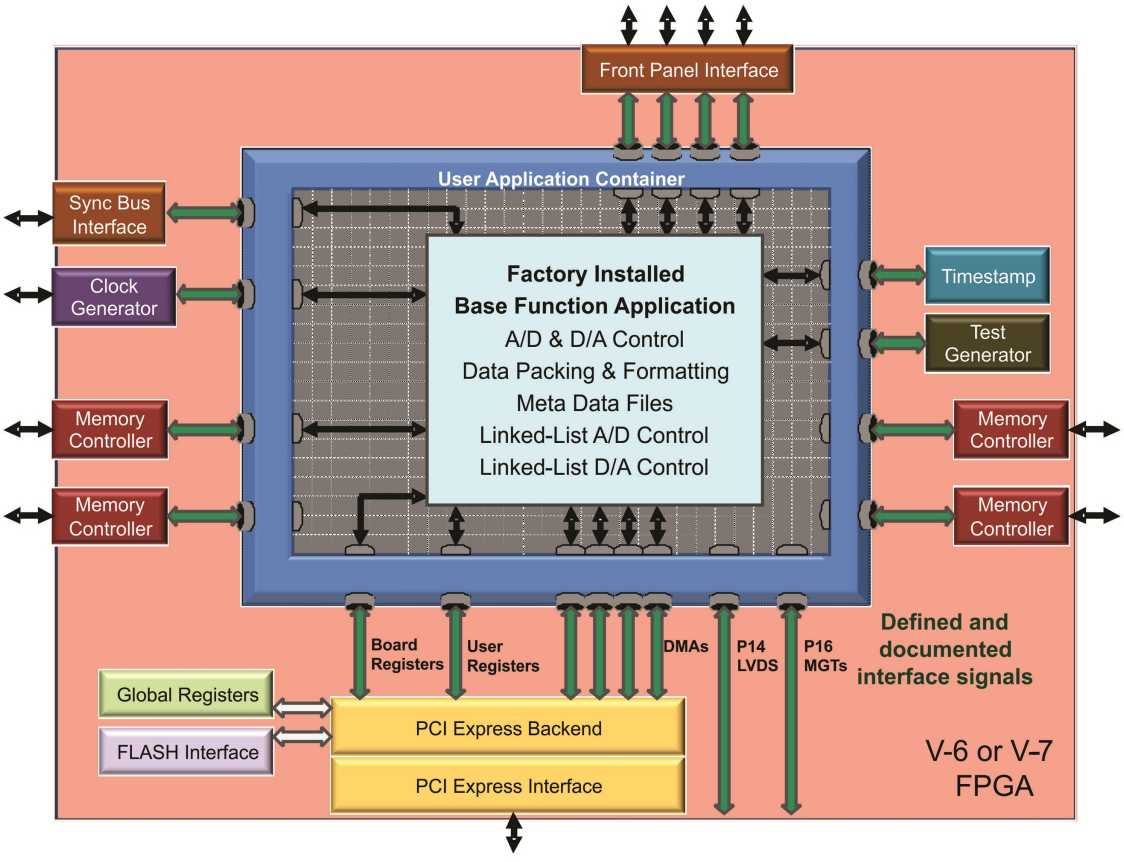
The GateFlow® FPGA Design Kit (FDK) allows the user to modify, replace and extend the standard installed functions in the FPGA to incorporate special modes of operation, new control structures, and specialized signal-processing algorithms.

The Cobalt (Virtex-6), Onyx (Virtex-7), and Flexor (Virtex-7) architectures configure the FPGA with standard factory-supplied interfaces including memory controllers, DMA engines, A/D and D/A interfaces, timing and synchronization structures, triggering and gating logic, time stamping and header tagging, data formatting engines, and the PCIe interface. These resources are connected to the User Application Container using well-defined ports that present easy-to-use data and control signals, effectively abstracting the lower-level details of the hardware.

The User Application Container

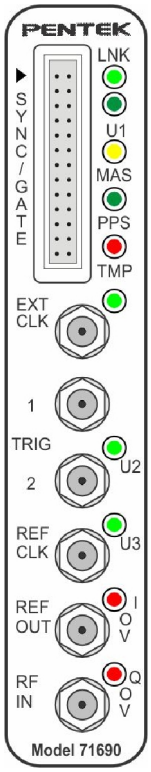
Shown below is the FPGA block diagram of a typical Cobalt, Onyx or Flexor module. The User Application Container holds a collection of different installed IP modules connected to the various interfaces through the standard ports surrounding the container. The specific IP modules for each product are described in further detail in the datasheet of that product.

The GateFlow FDK provides a complete Xilinx's ISE or Vivado project folder containing all the files necessary for the FPGA developer to recompile the entire project with or without any required changes. VHDL source code for each IP module provides excellent examples of how the IP modules work, how they might be modified, and how they might be replaced with custom IP to implement a specific function.



FRONT PANEL CONNECTIONS

The XMC front panel includes six SSMC coaxial connectors, and a 26-pin µSync connectors for clock, trigger, and analog input/output of timing and analog signals. The front panel also includes ten LEDs.



- **Sync Bus Connector:** The 26-pin Sync Bus front panel connectors labeled **SYNC/GATE** provides sync and gate input/output pins for the Low-Voltage Positive Emitter-Coupled Logic (LVPECL) Sync Bus.
- **Link LED:** The green **LNK** LED blinks when a valid link has been established over the PCIe interface.
- **User LEDs:** There are three green LEDs labeled **U1, U2** and **U3** for user applications. Use the LED Control Register USER LED SRC bits to select the signal source for these LEDs.
- **Master LED:** The yellow **MAS** LED illuminates when this model is the Sync Bus Master.
- **PPS LED:** The green **PPS** LED illuminates when a valid PPS signal is detected. The LED will blink at the rate of the PPS signal.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the PCB.
- **Clock LED:** The green **CLK** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.
- **External Clock Connector:** The front panel has one SSMC coaxial connector, labeled **EXT CLK** for input of an external sample clock. The external clock input can be used as the sample clock signal for the A/D converters.
- **Trigger Input Connectors:** Two SSMC coaxial connectors, labeled **TRIG 1** and **2** are for input of an external trigger or gate signals. The external trigger signal must be a LVTTL signal.
- **Reference Clock Input Connector:** One SSMC coaxial connector for a tuner reference clock input, labeled **REF CLK.**
- **Reference Clock Output Connector:** One SSMC coaxial connector for a tuner reference clock output, labeled **REF OUT**.
- **Analog Signal Input Connector:** One SSMC coaxial connector for RF analog signal input, labeled **RF IN.**
- **ADC Overload LEDs:** Two red overload LEDs, one for each A/D channel: **I OV** is for the ADS5485 associated with I data processing, **Q OV** is for the ADS5485 associated with the Q data processing.

SPECIFICATIONS

57690: One RF tuner, two A/Ds;
58690: Two RF tuners, four A/Ds

Front Panel Analog Signal Inputs (1 or 2)

Connector: Front panel female SSMC

Impedance: 50 ohms

L-Band Tuners (1 or 2)

Type: Maxim MAX2112

Input Frequency Range: 925 MHz to 2175 MHz

Monolithic VCO Phase Noise: -97 dBc/Hz at 10 kHz

Fractional-N PLL Synthesizer: $freq_{VCO} = (N.F) \times freq_{REF}$ where integer N = 19 to 251 and fractional F is a 20-bit binary value

PLL Reference ($freq_{REF}$): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz

LNA Gain: 0 to 65 dB, controlled by a programmable 12-bit D/A converter*

Baseband Amplifier Gain: 0 to 15 dB, in 1 dB steps*

*Usable Full-Scale Input Range: -50 dBm to +10 dBm

Baseband Low Pass Filter: Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution

A/D Converters (2 or 4)

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

Sample Clock Sources (1 or 2)

On-board timing generator/synthesizer

A/D Clock Synthesizers (1 or 2)

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

Timing Generator External Clock Inputs (1 or 2)

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus: 26-pin front panel connector LVPECL bus includes, clock/ sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/ PPS inputs

External Trigger Inputs (2 or 4)

Quantity: 2

Type: Front panel female SSMC connector, LVTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)

- Standard: Xilinx Virtex-6 XC6VLX130T
- Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O

- Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, 57690; P3 and P5, 58690
- Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, 57690; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, 58690

Memory Banks (1 or 2)

- Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI Express Interface

PCI Express Bus: Gen. 1 or 2: x4 or x8

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions:

- Depth: 171 mm (6.717 in.)
- Height: 100 mm (3.937 in.)

Weight: VPX Carrier: 110 grams (3.9 oz)

ORDERING INFORMATION

Model	Description
57690	L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - 6U VPX
58690	Dual L-Band RF Tuner with 4-Channel 200 MHz A/D and two Virtex-6 FPGAs - 6U VPX

Options	Description
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and P3 connector, 57690; P3 and P5 connectors, 58690
-105	Gigabit link between the FPGA and P2 connector, 57690; gigabit links from each FPGA to P2 connector, 58690
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
-702	Air-cooled, Level 2
-763	Conduction-cooled, Level 3

*This option is always required. Contact Mercury for compatible option combinations.

ACCESSORY PRODUCTS

Model	Description
2171	Cable Kit: SSMC to SMA

DEVELOPMENT SYSTEMS

Mercury offers development systems for Cobalt products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Cobalt boards. Please contact Mercury to configure a system that matches your requirements.

FORM FACTORS

Cobalt products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Cobalt Model 71690 XMC (L-Band RF Tuner and 2-Channel 200 MHz A/D with Virtex-6 FPGA) has the following variants:

Model	
52690	3U VPX board (single XMC with optical/backplane RF)
57690	6U VPX board (single XMC)
58690	6U VPX board (dual XMC)
71690	XMC module
78690	PCIe board (single XMC)

LIFETIME SUPPORT FOR COBALT PRODUCTS

Mercury offers worldwide customers shorter development time, reliable, rugged solutions for a variety of environments, reduced costs, and mature software development tools. We offer free lifetime support from our engineering staff, which customers can depend on through phone and email, as well as software updates. Take advantage of our 40 years of experience in delivering high-performance radar, communications, SIGINT, EW, and data acquisition MIL-Aero solutions worldwide.

Corporate Headquarters
50 Minuteman Road
Andover, MA 01810 USA
+1 978.967.1401 tel
+1 866.627.6951 tel
+1 978.256.3599 fax

International Headquarters
Mercury International
Avenue Eugène-Lance, 38
PO Box 584
CH-1212 Grand-Lancy 1
Geneva, Switzerland
+41 22 884 5100 tel

Learn more

Visit: mrcy.com/go/MP57690

For technical details, contact:
mrcy.com/go/CF57690