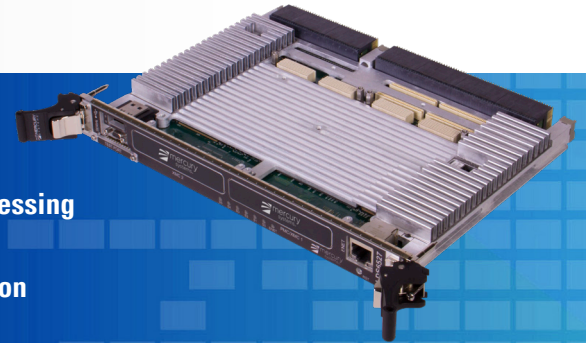


## EnsembleSeries™ LDS6527

6U OpenVPX SBC powered by 12-core server-class Xeon D processor

- Intel Xeon D family SoC processor with AVX2
- 40 Gb/s InfiniBand or Ethernet fabrics
- Integrated Gen3 PCIe switching infrastructure for on/off-board co-processing
- Dual mezzanine sites
- Optional MOTS+ rugged packaging for extreme environmental protection
- VITA 65 compliant



EnsembleSeries™ LDS6527 family of single board computers (SBCs) combine a powerful, 12-core server-class Xeon D processor, Mellanox CX-3 bridged Ethernet or InfiniBand high bandwidth switching, and configurable mezzanine I/O. Each SBC has a next-gen architecture that blends the computational power of an AVX2-enabled Xeon D processor with fast InfiniBand or 40Gb/s Ethernet data paths and the versatility of mezzanine-mounted I/O. This scalable computing architecture is well aligned to EW, next-gen radar, complex IMINT, sensor fusion and artificial intelligence (AI) applications.

### Optional MOTS+

The EnsembleSeries LDS6527 family of SBCs has options for modified off the shelf plus (MOTS+) packaging for extreme durability. MOTS+ configurations leverage enhanced commercial components, board fabrication rules, and subsystem design techniques for extra ruggedness and withstand extreme temperature cycles better than other rugged designs. Please contact Mercury directly for MOTS+ configurations.

### Intel Xeon D Family Server-Class Processor

EnsembleSeries LDS6527 SBCs features a 64-bit Xeon D family processor that is protected and cooled by Mercury's 5th generation of server-class packaging, which has previously been deployed in the full

spectrum of Mercury LDS and HDS 6U OpenVPX processing modules.

The D family of Xeon processors includes a system on chip (SoC) approach, combining the processor and the Intel platform controller hub (PCH) function within a single device. With two high-speed DDR4-2133 memory controllers, the Xeon processor is supported with 16GB-32GB of RAM. Significant PCIe interface capabilities are built in to the chip, which enable data interfaces both on-board and off-board.

The on-device PCH functionality enables the EnsembleSeries LDS6527 to access additional I/O, including USB and SATA on the backplane. The D family of Xeon processors has dual 10 Gigabit Ethernet interfaces, enabling backplane access for sensor data or additional inter-processor communication, as well as support for the AVX 2.0 instruction set, that boosts floating-point algorithm performance and is portable to future Intel architectures.

### High Speed Fabric Interfaces

EnsembleSeries LDS6527 SBCs complement Mercury's other OpenVPX modules that feature dual Mellanox ConnectX-3 host adaptors for data plane communications. Bridging between the native Gen3 PCIe interfaces on the Intel processor and the OpenVPX data plane, the ConnectX-3 can be configured to support InfiniBand (DDR or FDR10 rates) or 10/40 Gb/s Ethernet as the data protocol

*Mercury Systems is a leading commercial provider of secure processing subsystems designed and made in the USA. Optimized for customer and mission success, Mercury's solutions power a wide variety of critical defense and intelligence programs.*



## PCIe Architecture

EnsembleSeries LDS6527 SBCs provides a single Gen3 PCIe switch for both on-board switching and off-board expansion. This switch complex provides an x8 PCIe interface to each of the two VITA-compliant XMC sites, as well as an x4 connection to a PCIe to PCI-X® bridge for the single PMC site. This enables the mezzanine sites to operate at full bandwidth, optimizing the flow of I/O into the processing subsystem.

Externally, the LDS6527 implements a full Gen3 x16 PCIe connection to the OpenVPX expansion plane on the P2 VPX connector, and a Gen x8 PCIe connection to P5 as well. These expansion plane interfaces enable its compatibility with Mercury's GPU or FPGA based co-processing modules. These configuration options let the module effectively act as an upstream/downstream PCIe switch to allow the "chaining" of PCIe devices.

## Mezzanine Card Flexibility

EnsembleSeries LDS6527 SBCs provide two mezzanine sites: one PMC/ XMC and one XMC-only. Each of the standard mezzanine sites may be configured with off-the-shelf mezzanine cards to bring additional I/O into the system for processing or control. PMC cards are supported with a 32-bit or 64-bit PCI/PCI-X interface at up to 133 MHz on the PMC/XMC site, with PMC user-defined I/O mapped to the backplane. XMCs are supported with x8 PCIe on the J15/J25 connector per the VITA 42.3 standard. There are 16 differential pairs and 38 single-ended signals of XMC user I/O mapped to the backplane via the J16/J26 connector.

The LDS6527 utilizes VITA 61 XMC connectors for Gen3 PCIe signal integrity and greater ruggedness.

## Multiple I/O Options

In addition to the flexibility offered via the on-board mezzanine sites, EnsembleSeries LDS6527 SBCs have a variety of additional built-in I/O options:

- One 10/100/1000BASE-T Gigabit Ethernet connection can be routed to the front-panel on air-cooled configurations or to the backplane.
- One additional 10/100/1000BASE-T Gigabit Ethernet connection is routed to the backplane.
- Two 1000BASE-BX SERDES Ethernet connections are routed to the backplane per the OpenVPX control plane specification.
- Two additional 10GBASE-KR SERDES Ethernet connections are routed to the backplane
- One TIA-232 serial port is routed to the front-panel on air-cooled configurations, or to the backplane on conduction-cooled configurations. When routed to the backplane, the serial interface can be configured for either TIA-232 or TIA-422 signaling.
- One front-panel USB 3.0 interface is available on air-cooled configurations.

- Two backplane USB interfaces are available (one 2.0, one 3.0) with both air-cooled and conduction-cooled configurations.
- Two SATA interfaces to the backplane are provided to interface with storage devices.
- Eight GPIO lines act as discrete I/O usable as input, output, or to generate interrupts on the module.
- Several additional bussed signals enhance the functionality of the LDS6527 module.

## System Management

EnsembleSeries LDS6527 SBCs implements full compliance to advanced system management functionality architected in the OpenVPX (VITA 46.11) standard to enable remote monitoring, alarm management, and hardware revision and health status. Using the standard I2C bus and intelligent platform management controller (IPMC) protocol, the on-board system management block implements the IPMC. This allows LDS6527 SBCs to:

- Read sensor values
- Read and write sensor thresholds, allowing an application to react to thermal, voltage or current variations that exceed those thresholds
- Reset the entire SBC
- Power up/down the entire SBC
- Retrieve SBC field replaceable unit (FRU) information
- Be managed remotely by a chassis management controller at the system level, such as implemented on Mercury's 6U OpenVPX chassis or system management modules

## VPX-REDI

The VPX (VITA 46) standard defines 6U and 3U board formats with a modern high-performance connector set capable of supporting today's high-speed fabric interfaces. VPX is most attractive when paired with the ruggedized enhanced design implementation standard — REDI (VITA 48). EnsembleSeries LDS6527 SBCs packaged as conduction-cooled/Air Flow-By options are VPX-REDI compliant, with air-cooled variants in the same VPX form factor available for less rugged environments.

Targeted primarily for harsh-environment embedded applications, VPX-REDI offers extended mechanical configurations supporting higher functional density, such as two-level maintenance (2LM). 2LM allows maintenance personnel to replace a failed module and restore the system to an operational state in a limited time period.

## Air Flow-By

Air-cooled chassis require filters to remove contaminants from their cooling air streams. Mercury's Air Flow-By technology eliminates filtration with the most elegant cooling solution available within a sealed and rugged package. Air Flow-By technology is resilient, boosts SWaP

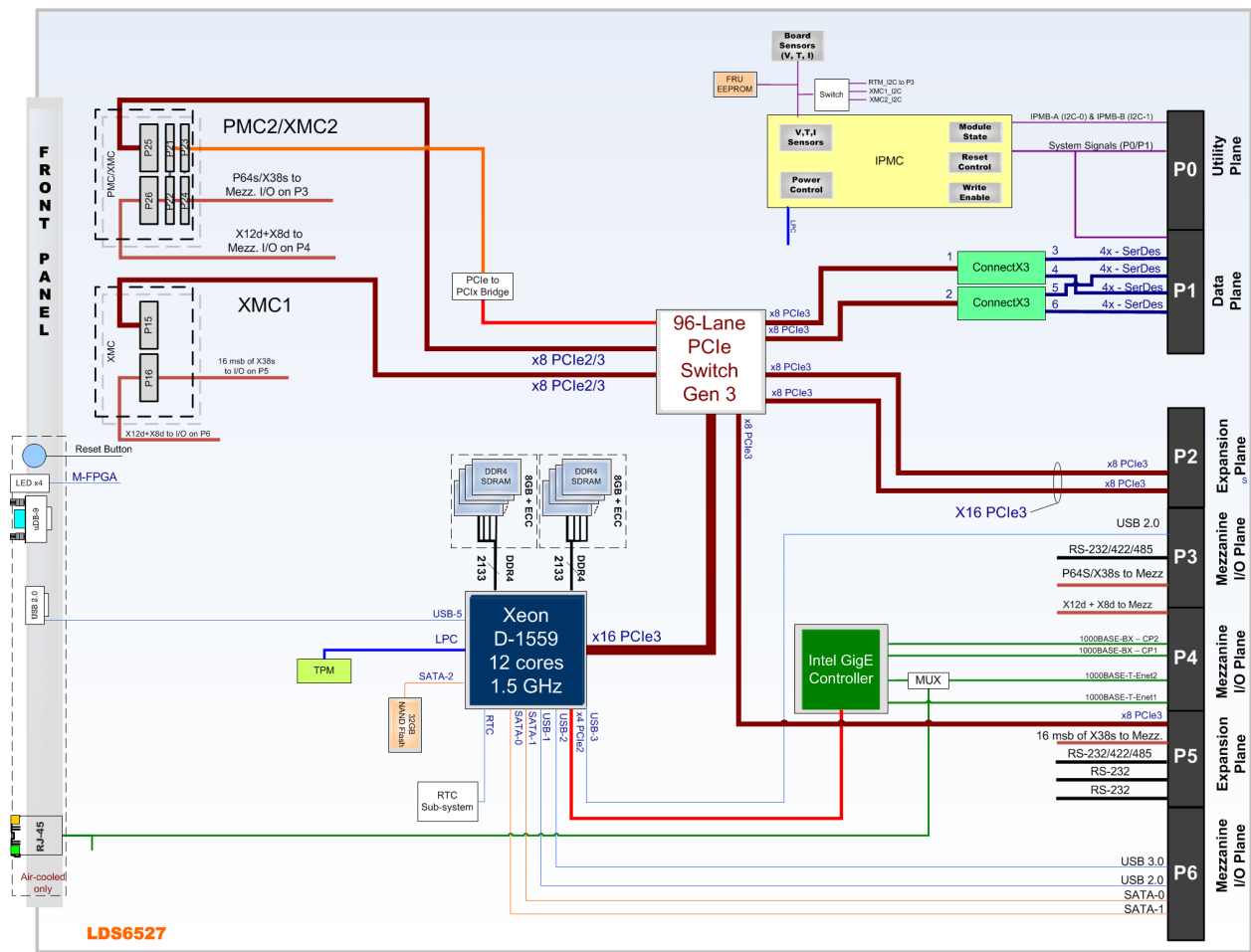


Figure 1. LDS6527 functional block diagram

performance, reduces operating temperature, extends MTBF by an order of magnitude and enables the most powerful processing solutions.

## Additional Features

EnsembleSeries LDS6527 SBCs provide all the features typically found on a single-board computer. In addition to the sophisticated management subsystem and switched fabric interconnect, LDS6527 SBCs provide users with a toolkit enabling many different application use cases. Features include:

- Real-time clock with granularity to 1ms and time measurement of up to 30 years
- General-purpose timers for synchronization
- Watchdog timer to support processor interrupt or reset
- Multiple boot paths, including netboot, USB boot and boot from SATA or the on-board 32 GB flash device.

## Open Software Environment

Mercury leverages over 35 years of multicomputer software expertise, including recent multicore processor expertise, across its many platforms. This strategy is fully applied to EnsembleSeries LDS6527 SBCs. The same Linux® development and run-time environment is implemented

on LDS6527 SBCs as on other Intel-based Mercury EnsembleSeries building blocks. Off-the-shelf open software such as OFED, OpenMPI and MultiCore Plus™ are fully supported.

## Mercury Sensor Processing Ecosystem

Modern sensor compute subassemblies are customized assemblies of interoperable building blocks built to open standards. Mercury's hardware and software portfolio of building blocks are physically and electrically interoperable as defined by international industrial standards, including VITA's OpenVPX standards. Our subsystems are designed from a suite of sophisticated open architecture building blocks that are combined and scaled to meet a broad range of advanced sensor chain processing requirements.

Mercury subsystems may include analog, digital and mixed-signal receiver modules, single-board computers and signal processing payload modules. Payloads may have acquisition, digitization, processing, and exploitation and dissemination elements and include FPGA, CPU, GPU or ADC/DAC technology, and be made up of multiple subsystems developed to multiple standards, including OpenVPX and others such as ATCA, ATX/E-ATX, or VME/VXS.

## Specifications

### Processor

Single Intel 12-core, 64 bit, Xeon D-1559 at 1.5 GHz

Threads per core: 2 (24 total per CPU)

Processor support

AVX2, 256 bit vector engine incorporating

Fused multiple-add (FMA)

Memory

16GB-32GB DDR4-2133

PCIe Gen 3 (x8)

### Built-in options

For extra MOTS ruggedness, please refer to Mercury's "[Environmental Protections for Operation at the Tactical Edge](#)" for specific ruggedness levels and cooling options.

### Intelligent Platform Management Interface (IPMI)

On-board IPMI controller

Voltage and temperature monitor

Geographical address monitor

Power/reset control

On-board FRU EEPROM interface

FPGA, CPU and CPLD interfaces

### Data Plane PCIe to Switched Fabric Bridge

Dual Mellanox ConnectX-3 VPI host adapters

Support DDR/FDR10 InfiniBand or 10/40 Gb/s Ethernet protocols

### OpenVPX Multi-Plane Architecture

System management via IPMB-A and IPMB-B links on P0 management plane

Full x16 or dual x8 Gen3 PCIe expansion plane to P2 connector; x8 Gen3 PCIe to P5 connector

Dual 1000BASE-BX Ethernet control plane

### PMC/XMC Sites

Mezzanine sites 1 PMC/XMC and 1 XMC

PCI-X to PCIe bridge Connects PMC site to on-board

PMC PCI support 33 and 66 MHz

PMC PCI-X support 66, 100, and 133 MHz

PMC user-defined I/O from J14 to backplane

PCIe XMC sites per VITA 42.3 with XMC user-defined I/O from Jn6 to backplane

### Additional I/O Capabilities

One RS-232 serial interface to front-panel (air-cooled) or backplane (conduction cooled)

Configurable for RS-232 or RS-422 signaling when routed to backplane

One additional RS-232/RS-422 serial interface to backplane

One front-panel USB 2.0 interface (air-cooled configurations only)

One USB 2.0 interface to backplane

One USB 3.0 interface to backplane

Two SATA interfaces to backplane

Eight single-ended GPIO interfaces to backplane

System signals to backplane NVMRO, chassis test

Environmental bypass, memory clear

### Mechanical

Extended MOTS ruggedness – Consult factory

6U OpenVPX - 1.0" slot pitch except some Air Flow-Through configurations

OpenVPX and VPX-REDI

### Compliance

OpenVPX system standard encompasses VITA 46.0, 46.3, 46.4, 46.6, 46.11

VITA 65 module profile

MOD6-PAY-4F1Q2U2T-12.2.1-n, where n can vary based on ConnectX-3 configuration

SLT6-PAY-4F1Q2U2T-10.2.1

SLT6-PAY-4F1Q2U2T-10.2.6

SLT6-PAY-4F1Q2U2T-10.2.1

VITA 61 (High-speed XMC connectors)

VITA 46.11 (System management)

VITA 48/48.1/48.2/48.4/48.7 (REDI)

InfiniBand, PCIe, 10/40 Gigabit Ethernet

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