Jade 54891

L-band RF tuner, 2-channel 400 MHz A/D 3U VPX board with Kintex UltraScale FPGA

Enhances SATCOM and communications applications

- Maxim MAX2121 L-Band RF tuner boosts output bandwidth to 123 MHz
- Dual 400 MHz 14-bit A/Ds capture full signal bandwidth
- Improved signal quality with integrated digital downconverters
- Navigator ® Design Suite speeds development and custom IP integration

The Jade® 54891 3U VPX board is an L-Band RF tuner with two 400 MHz A/Ds based on the high-density Xilinx Kintex UltraScale FPGA. The 54891 is designed for connection directly to SATCOM or communications system L-band signals.

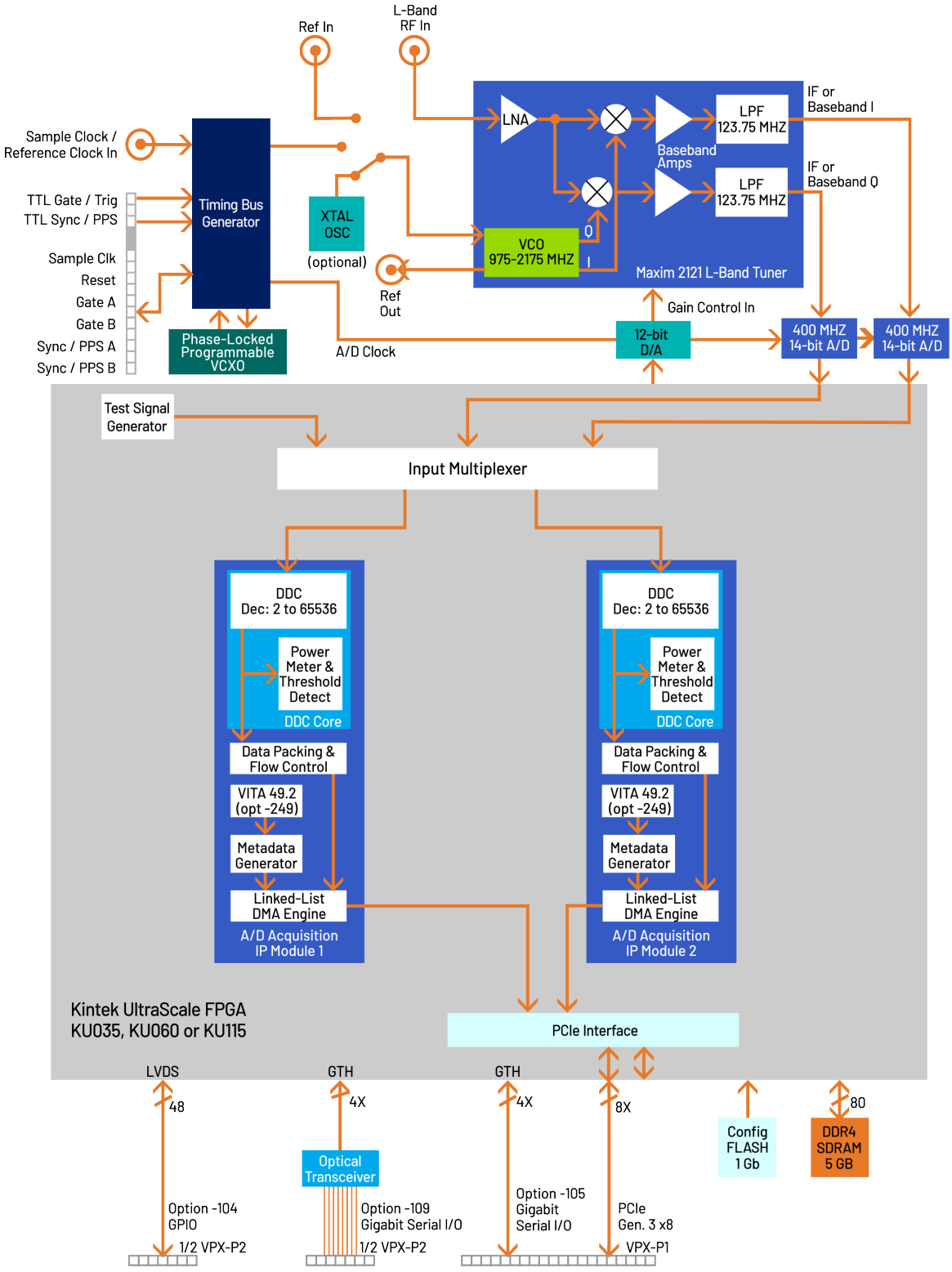
A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). With its programmable LNA, the Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q analog downconverter followed by 123 MHz low pass anti-aliasing filters. The two analog tuner outputs are digitized by two Texas Instruments ADS5474 400 MHz 14-bit A/D converters to capture the full 123 MHz bandwidth.

FEATURES

- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNA handles L-Band input signal levels from -50 dBm to +10 dBm
- Programmable analog downconverter provides IF or I+Q baseband signals at frequencies up to 123 MHz
- Two 400 MHz 14-bit A/Ds digitize IF or I+Q signals synchronously
- Two FPGA-based multiband DDCs (digital downconverters)
- Xilinx® Kintex® UltraScale™ FPGA
- Five GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Clock/sync bus for multimodule synchronization
- Optional LVDS port and gigabit serial connections for custom FPGA I/O
- Optional optical interface for data streaming
- Navigator Design Suite for software and custom IP development

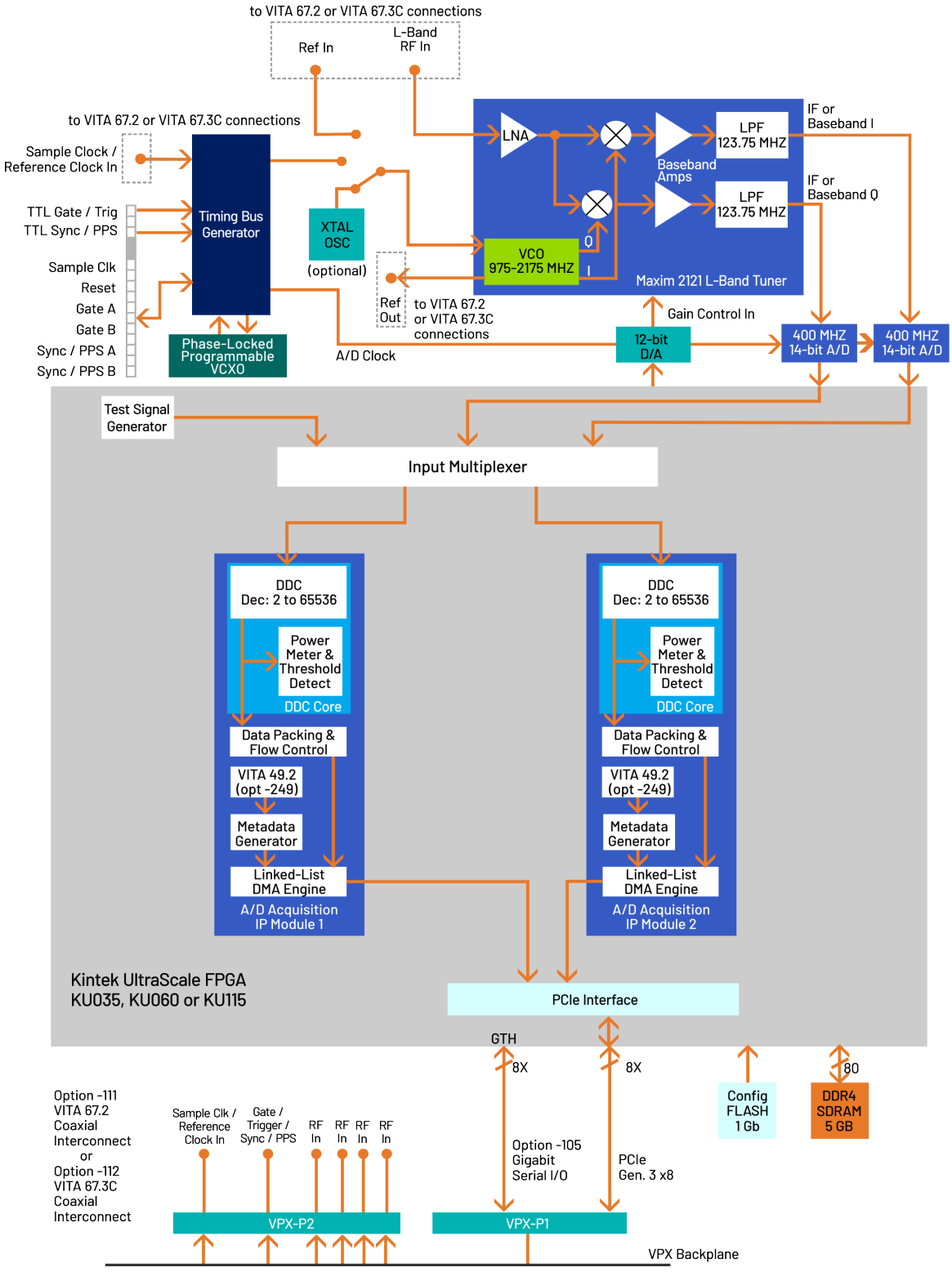
54891 BLOCK DIAGRAM

Click on a block for more information.



54891 BLOCK DIAGRAM (OPTIONS -111 AND -112 SHOWN.)

Click on a block for more information.



THE JADE ARCHITECTURE

Evolved from the proven designs of Mercury's Cobalt® and Onyx® families, Jade® raises the processing performance while lowering the overall power requirements by building on the Xilinx family of Kintex UltraScale FPGAs. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions as well as providing an ideal platform for user-created intellectual property (IP).

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions include A/D acquisition modules for simplifying data capture and tagging, DDCs (digital downconverters), an RF tuner controller, and specialized DMA engines for efficient data transfers between the board and a host computer.

Additional IP includes: a clock and synchronization generator; a test signal generator, and a PCIe interface. These factory-installed applications enable the to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

XILINX KINTEX ULTRASCALE FPGAS

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs: KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

RF TUNER STAGE

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). The Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA, a PLL (phase-locked loop) synthesized local oscillator, quadrature (I+Q) downconverting mixers, output low pass filters, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to one of three selectable frequency references: the timing generator output, an external reference input between 12 and 30 MHz, or an on-board crystal oscillator.

Together, the RF LNA and baseband amplifiers accommodate input signal levels from –50 dBm to +10 dBm. The integrated low pass filter has a 3 dB bandwidth of 123.75 MHz.

For best performance, the analog outputs of the MAX2121 should be used in the IF mode instead of the analog baseband I+Q mode. In this case, the IF signal is digitized by the A/D converter and then delivered to the DDC to produce perfectly balanced digital I+Q complex samples, 16 bits each.

A/D CONVERTERS AND DDCS

The two analog tuner outputs are digitized by two Texas Inst. ADS5474 400 MHz 14-bit A/D converters. Another benefit of using the preferred IF analog output mode is that two independent A/D and DDC channels are now available for digitizing and downconverting two signals with different center frequencies and bandwidths.

A/D ACQUISITION IP MODULES

The 54891 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, or a test signal generator. Each acquisition module has a DMA engine for efficiently moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP CORES

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation

setting, supporting two different output bandwidths. Decimations can be set from 2 to 65,536 to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

A/D CLOCKING & SYNCHRONIZATION

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/ trigger signals within the module. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave modules, supporting synchronous sampling and sync functions across all connected boards.

MEMORY RESOURCES

The 54891 architecture includes a 5 GB bank of DDR4 SDRAM memory. This resource is used by the board's built-in functions for data storage and buffering, but can also be used for custom applications. The Navigator FDK provides a memory controller as well as guidance on the most efficient use of the memory when creating IP functions.

PCI EXPRESS INTERFACE

The 54891 includes an industry standard interface fully compliant with PCI Express Gen. 1, 2, and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

3U VPX INTERFACE

The 54891 complies with the VITA 65.0 3U VPX specification. In addition to supporting PCIe Gen. 3, x8 on the VPX P1 connector, option -105 adds up to 8 more gigabit serial lanes connected directly to the FPGA for supporting user-installed protocols.

The 54891 offers flexible analog and digital interface options for the VPX-P2 to meet system-specific requirements.

Option -104 provides 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

When purchased with option -109, the 54891 supports the emerging VITA 66.5 standard and provides four optical duplex lanes to a mating VITA 66.5 backplane connector. With the installation of a serial protocol like 10 or 40 Gigabit Ethernet in the FPGA, the VITA 66.5 interface enables high-bandwidth communications between boards or chassis independent of the PCIe interface.

See Specifications for the OpenVPX Profile

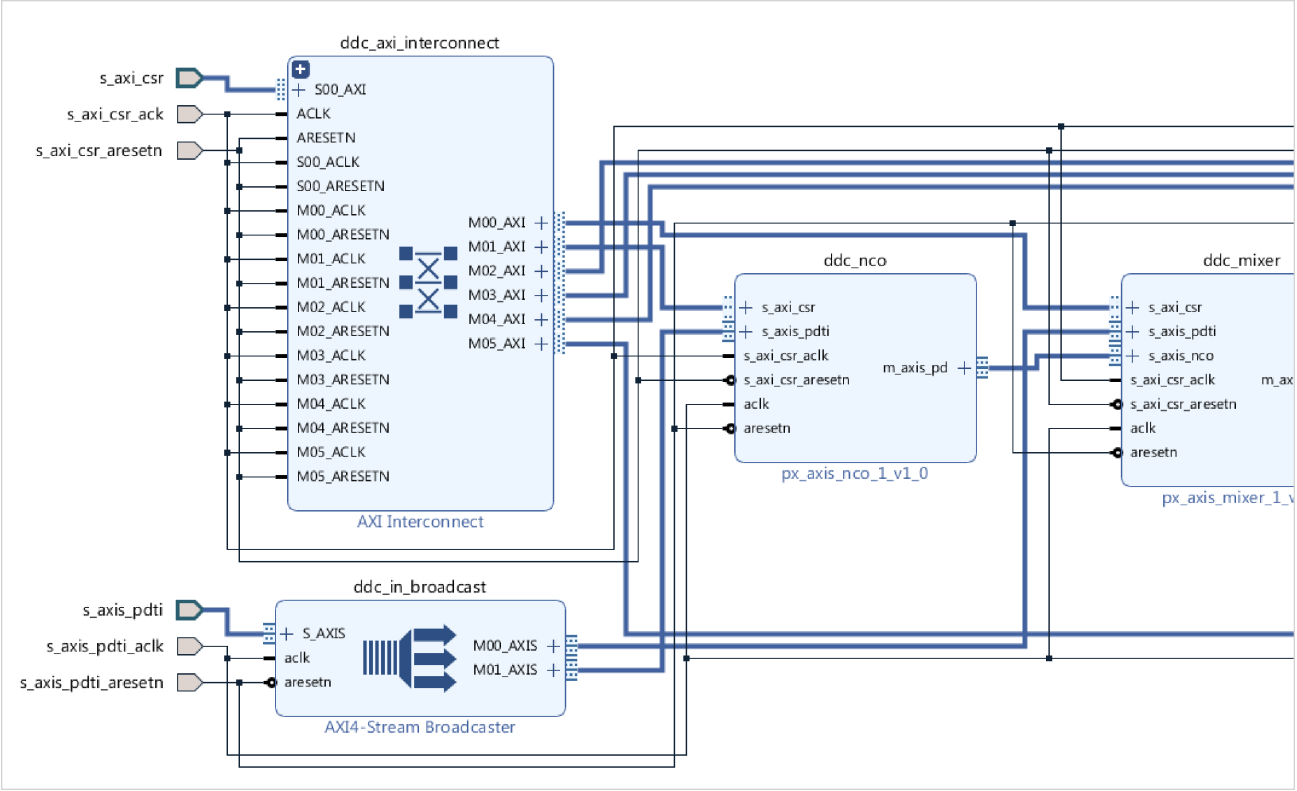
NAVIGATOR DESIGN SUITE

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into the factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

The **Navigator FPGA Design Kit (FDK)** for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Jade product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Jade design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations.

Navigator FDK includes an IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.

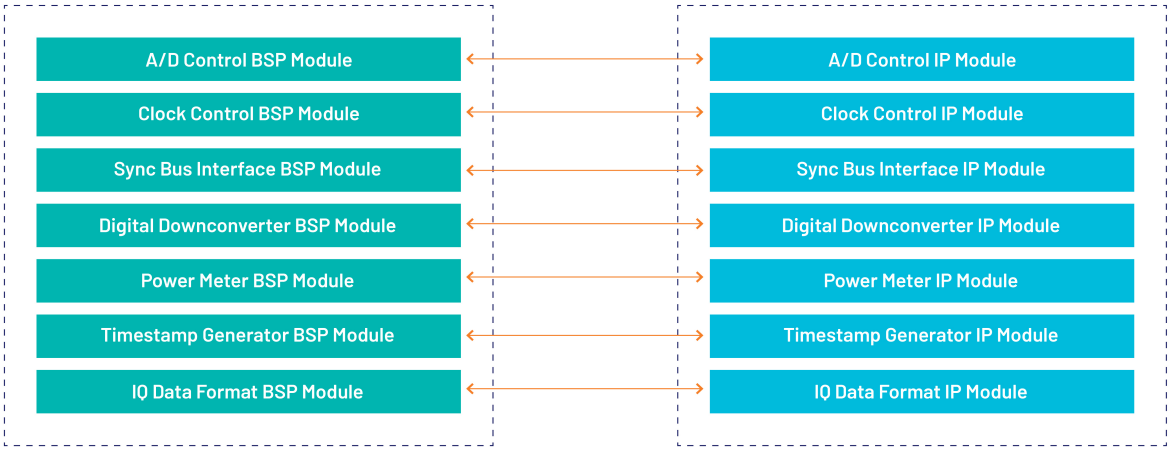
The **Navigator Board Support Package (BSP)** provides software support for Jade boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA. The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.



Navigator IP FPGA Design viewed in IP Integrator

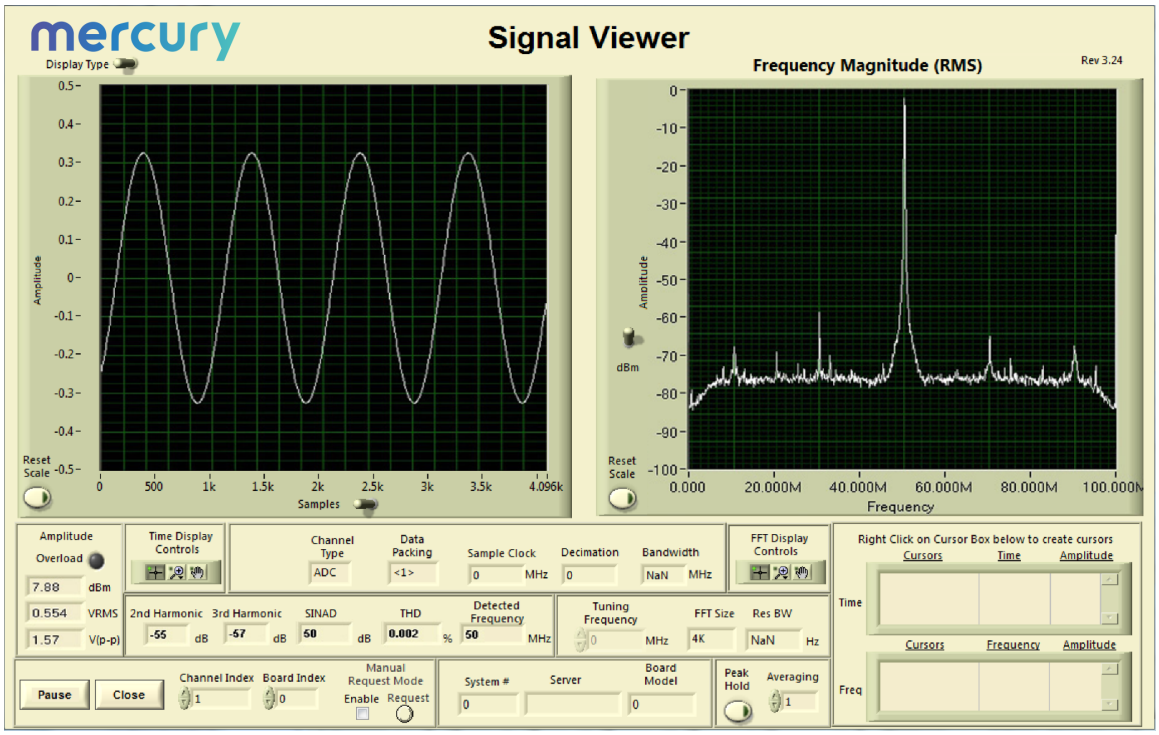
NAVIGATOR BOARD SUPPORT PACKAGE

NAVIGATOR FPGA DESIGN KIT



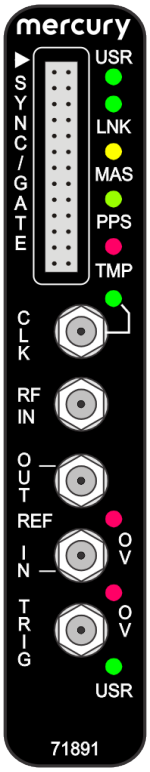
Because all Jade boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the **Signal Viewer**, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Jade board and Navigator BSP and start viewing analog signals immediately.



FRONT PANEL CONNECTIONS

The XMC front panel includes five SSMC coaxial connectors and a 26-pin Sync Bus connector for input/output of clock, trigger and analog signals. The front panel also includes nine LEDs.



- **Sync Bus Connector:** The 26-pin Sync Bus front panel connector, labeled **SYNC/GATE**, provides clock, sync, and gate input/output pins for the LVPECL Sync Bus.
- **User LED:** The green **USR** LED is for user applications.
- **Link LED:** The green **LNK** LED blinks when a valid link has been established over the PCIe interface.
- **MAS LED:** The yellow **MAS** LED illuminates when this model is the Sync Bus Master.
- **PPS LED:** The green **PPS** LED illuminates when a valid PPS signal is detected. The LED will blink at the rate of the PPS signal.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the PCB.
- **Clock Input Connector:** One SSMC coaxial connector, labeled **CLK**, for input of an external sample clock.
- **Clock LED:** The green **CLK** LED illuminates when a valid sample clock signal is detected.
- **Reference Clock Input Connector:** One SSMC coaxial connector for a RF analog signal input, labeled **RF IN.**
- **Reference Clock Output Connector:** One SSMC coaxial connector for a tuner reference clock output, labeled **REF OUT.**
- **Analog Signal Input Connector:** One SSMC coaxial connector, labeled **REF IN**, is for a tuner reference clock input.
- **ADC Overload LEDs:** Two red **OV** (overload) LEDs for each A/D channel.
- **Trigger Input Connector:** The SSMC coaxial connector labeled **TRIG** is for input of an external trigger or gate signal. The signal must be a LVTTL signal.
- **User LED:** One green **USR** LED for user applications.

SPECIFICATIONS

Front Panel Analog Signal Inputs

Connector: Front panel female SSMC

Impedance: 50 ohms

L-Band Tuner

Type: Maxim MAX2121

Input Frequency Range: 925 MHz to 2175 MHz

Monolithic VCO Phase Noise: –97 dBc/Hz at 10 kHz

Fractional-N PLL Synthesizer: freqVCO = (N.F.) x $freq_{REF}$ where integer N = 19 to 251 and fractional F is a 20-bit binary value

PLL Reference ($freq_{REF}$): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz

LNA Gain: 60 dB range, controlled by a programmable 12-bit D/A converter

Usable Full-Scale Input Range: –50 dBm to +10 dBm

Baseband Low Pass Filter: 3 dB cutoff frequency: 123.75 MHz

A/D Converters

Type: Texas Instruments ADS5474

Sampling Rate: 10 MHz to 400 MHz

Resolution: 14 bits

Sample Clock Sources

On-board timing generator/synthesizer

A/D Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

Timing Generator External Clock Input

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus

26-pin front panel connector LVPECL bus includes, clock/ sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/ PPS inputs

External Trigger Input

Quantity: 2

Type: Front panel female SSMC connector, LVTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Kintex UltraScale XCKU035-2

- Option -084: Xilinx Kintex UltraScale XCKU060-2
- Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O

- Option -104: provides 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- Option -105: provides an 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols (gigabit link is 4X when combined with option 109)
- Option -109: VITA 66.5 interface provides optical 4X duplex lanes

Memory

Processing System:

Type: DDR4 SDRAM

Size: 5 GB each

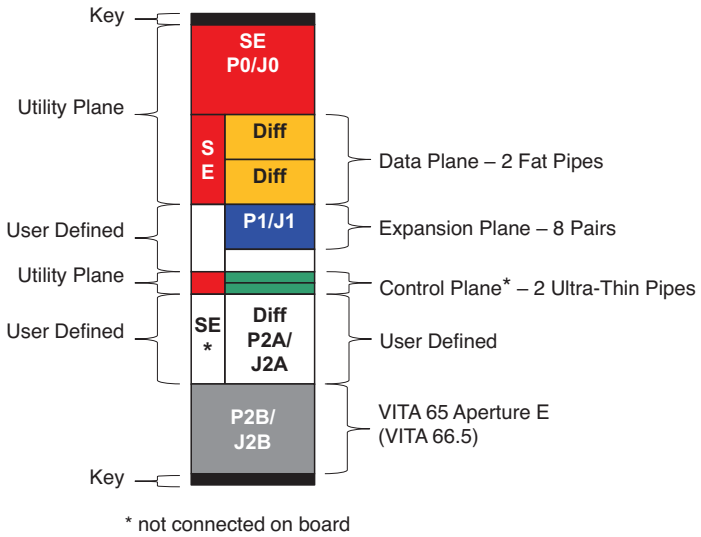
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

PCI Express Bus: PCI Express Bus: Gen. 1, 2 or 3: x8

OpenVPX Profile

The 54891 is compatible with multiple OpenVPX profiles. Profile for standard and option 109 shown below.



* not connected on board

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: 3U VPX board

- Depth: 170.61 mm (6.717 in)
- Height: 100 mm (3.937 in

Weight: Approximately 15.9 oz (450 grams)

ORDERING INFORMATION

Model	Description
54891	L-band RF tuner, 2-channel 400 MHz A/D 3U VPX board with Kintex UltraScale FPGA

Options:	
-014	400 MHz, 14-bit A/Ds
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-100	27 MHz crystal for MAX2121
-104	LVDS FPGA I/O through VPX P2
-105	Gigabit serial FPGA I/O through VPX P1
-109	VITA 66.5: Optical 4X duplex lanes
-702	Air-cooled, Level 2
-763	Conduction-cooled, Level 3

Contact Mercury for compatible option combinations and complete specifications of rugged and conduction-cooled versions. Options may change, so be sure to contact Mercury for the latest information.

ACCESSORY PRODUCTS

Model	Description
2171	Cable Kit: SSMC to SMA

DEVELOPMENT SYSTEMS

Mercury offers development systems for Jade products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Jade boards. Please contact Mercury to configure a system that matches your requirements.

FORM FACTORS

Jade products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Jade Model 71891 XMC (L-Band RF Tuner and 2-Channel 400 MHz A/D with Kintex UltraScale FPGA) has the following variants:

Model	
54891	3U VPX board (single XMC with optical/backplane RF)
57891	6U VPX board (single XMC)
58891	6U VPX board (dual XMC)
71891	XMC module
78891	PCIe board (single XMC)

Corporate Headquarters
50 Minuteman Road
Andover, MA 01810 USA
+1 978.967.1401 tel
+1 866.627.6951 tel
+1 978.256.3599 fax

International Headquarters
Mercury International
Avenue Eugène-Lance, 38
PO Box 584
CH-1212 Grand-Lancy 1
Geneva, Switzerland
+41 22 884 5100 tel

Learn more

Visit: mrcy.com/go/MP54891

For technical details, contact:
mrcy.com/go/CF54891

MADE IN USA