Jade 5585

3U VPX SOSA aligned 8-channel 250 MHz A/D board with Virtex UltraScale+ HBM FPGA

Complete radar and software radio interface

- Wideband data acquisition
- Multichannel, multiboard synchronization for high channel count systems
- High-bandwidth memory, FPGA logic and DSP density make this board a single-slot 3U VPX processing powerhouse

The 5585 SOSA aligned 3U OpenVPX board is an 8-channel, high-speed data converter with programmable DDCs (digital down-converters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

Ample data transfer bandwidth and flexibility are provided by a range of board interfaces including 1 GigE, 10 GigE, 40 GigE, dual 100 GigE and PCIe with installation of Mercury or user-supplied IP. The Virtex UltraScale+ HBM's on-chip high-bandwidth memory coupled with the FPGA's logic and DSP density enable the 5585 to be a single-slot SOSA aligned 3U VPX data acquisition and processing powerhouse.

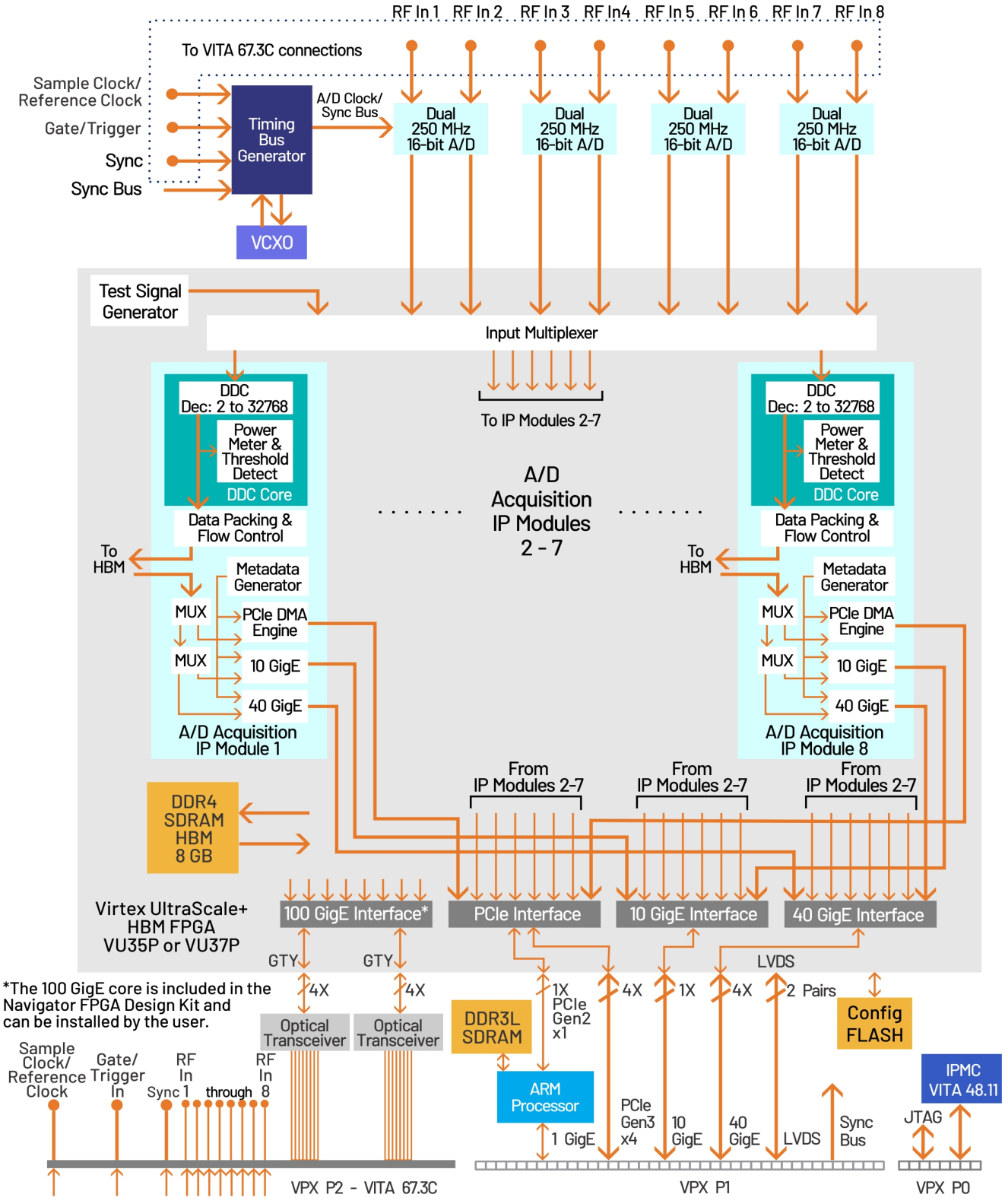
FEATURES

- Exceptional dynamic range and analog signal integrity
- Features Xilinx Virtex UltraScale+ HBM FPGAs
- Eight 250 MHz 16-bit A/Ds
- 10 GigE Interface
- 40 GigE Interface
- Dual 100 GigE UDP interface
- Optional VITA 67.3C optical interface for backplane gigabit serial communication
- Compatible with several VITA standards including: VITA 46, VITA 48.11, VITA 67.3C and VITA 65 (OpenVPX™ System Specification)
- Navigator Design Suite for software and custom IP development

SOSA™
Sensor Open Systems Architecture

5585 BLOCK DIAGRAM

Click on a block for more information.



BOARD ARCHITECTURE

The 5585 board design places the Virtex UltraScale+ FPGA as the cornerstone of the architecture. The FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 5585 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core; a controller for all data clocking and synchronization functions; a test signal generator; and interfaces to PCIe, 10 and 40 GigE. An optional 8-lane optical interface is also available and provides a dual 100 GigE interface with an IP core included with the Navigator FPGA Design Kit and installed by the user. These complete the factory-installed functions and enable the 5585 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. The Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the factory-installed functions or use the Navigator kit to completely replace the Mercury IP with their own.

XILINX VIRTEX ULTRASCALE+ HBM FPGA

The 5585 features the VU37P Virtex UltraScale+ HBM. The FPGA's 8 GB of on-chip HBM SDRAM supports memory bandwidth of up to 460 GB/s. This represents better than a 20X throughput increase over traditional, external DDR4 SDRAM. This increased performance addresses the ever-accelerating memory requirements of high bandwidth, high computation applications. Additional resources include 9024 DSP slices, 2.8 million system logic cells and 32.7 Gb/s GTY gigabit serial transceivers.

A/D CONVERTER STAGE

The front end accepts eight analog HF or IF inputs from the VITA 67.3 C connector with transformer coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16- bit A/D converters. The digital outputs are delivered into the Virtex UltraScale+ HBM FPGA for signal processing or routing to other module resources.

A/D ACQUISITION IP MODULES

The 5585 features eight A/D Acquisition IP Modules for easily capturing and transferring data. Each module can receive data from any of the eight A/Ds, or a test signal generator and move the acquired data off board over 10 GigE, 40 GigE or PCIe.

For each transfer, the acquisition module can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP CORES

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved, including one A/D driving all DDCs or each of the A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to fs, where fs is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 32,768, providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*fs/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of fs/N.

CLOCKING AND SYNCHRONIZATION

An on-board timing bus generator uses a programmable frequency synthesizer to generate the sample clock and all required timing signals, enabling the board to operate with no additional clocks required. For applications that require an external sample clock, the 5585 can receive the full rate sample

clock through one of the VITA 67.3C connections, or in an alternate mode, a reference clock can be received on this connection and used to lock the on-board sample clock to a house reference. A multifunction gate/trigger input is also available on one of the VITA 67.3C connections for external control of data acquisition as well as a sync input signal for resetting counters and clocks on the board.

For larger systems requiring multi-board synchronization, a multisignal sync bus interface is provided on the VPX P1 connector. This interface includes the reference clock, the gate/trigger input, and the sync signal The Model 5503 High-Speed Synchronizer and Distribution 3U VPX Board is available as a programmable clocking and sync source for these high-channel-count systems.

ARM PROCESSOR

The 5585's on-board ARM processor provides a path to reprogram the FPGA through 1 GigE. This is ideal for applications that might need to dynamically change FPGA functionality during deployment. The processor runs Linux.

INTEGRATED PLATFORM MANAGEMENT CONTROLLER

The 5585 uses an Integrated Platform Management Controller (IPMC) to provide a fully compliant and flexible management solution for Field Replaceable Units (FRU) that support the VITA 46.11 standard required by HOST and SOSA architectures. The IPMC provides a standardized implementation of FRU management interfaces, control signals and sensor monitoring.

The IPMC provides the Chassis Manager and higher-level System Management Software (SMS) access to FRU information, FRU control signals and sensor monitoring functions so that they can identify, activate/de-activate, reset and monitor the health of the card and take appropriate system control actions.

The IPMC also provides a low-level path for configuration management and FRU maintenance through both IPMI messages and a Maintenance Port (MP) serial interface. The maintenance port provides a terminal mode command-line interface and supports monitoring, data uploads and FRU-level troubleshooting.

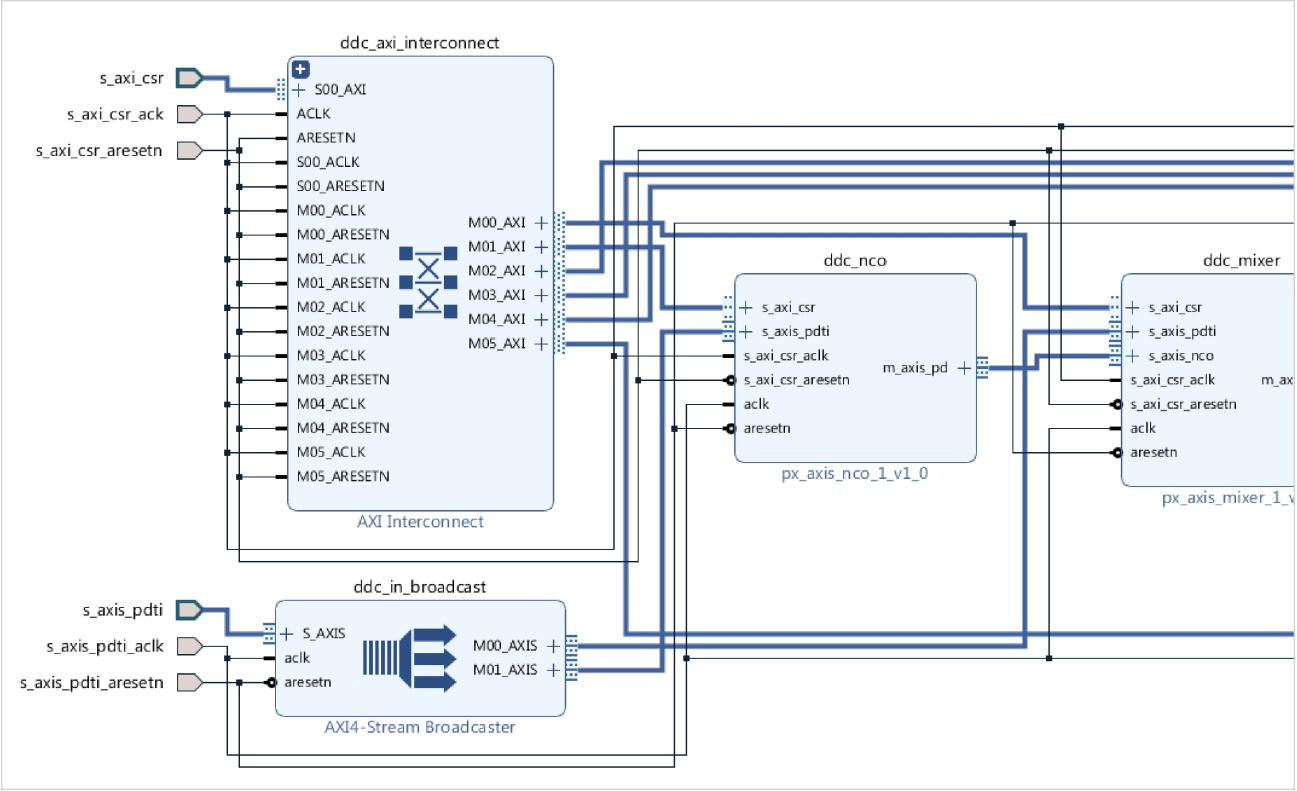
NAVIGATOR DESIGN SUITE

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into the factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

The **Navigator FPGA Design Kit (FDK)** for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Jade product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Jade design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations.

Navigator FDK includes an IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.

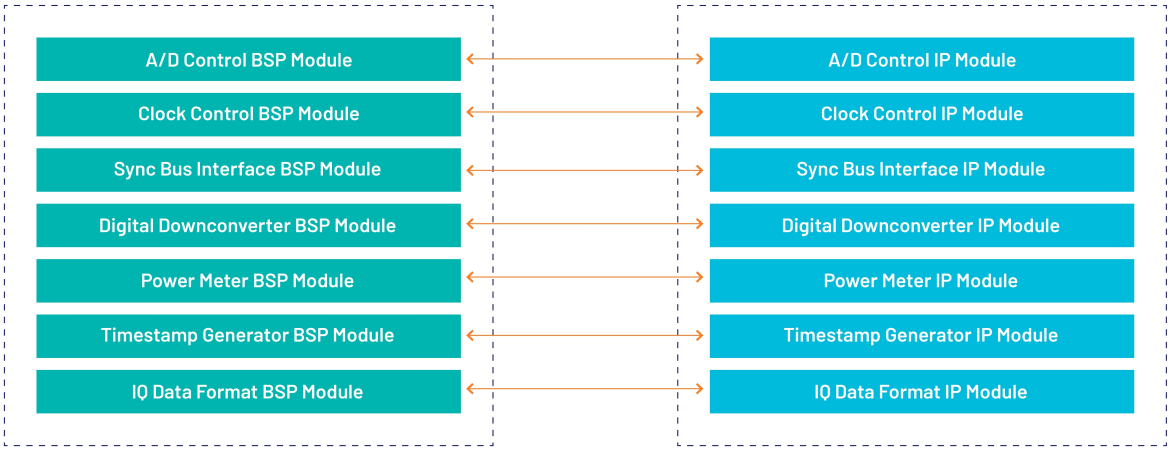
The **Navigator Board Support Package (BSP)** provides software support for Jade boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA. The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.



Navigator IP FPGA Design viewed in IP Integrator

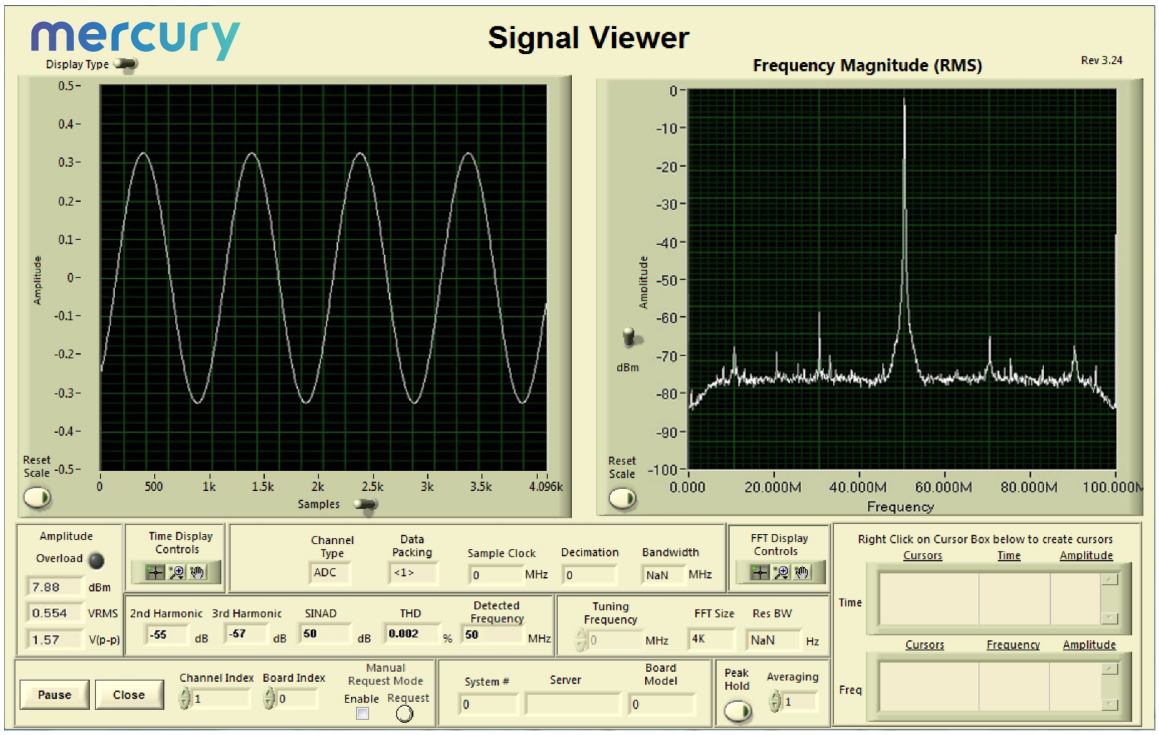
NAVIGATOR BOARD SUPPORT PACKAGE

NAVIGATOR FPGA DESIGN KIT



Because all Jade boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the **Signal Viewer**, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Jade board and Navigator BSP and start viewing analog signals immediately.



SPECIFICATIONS

Analog Inputs

Quantity: 8

Connector: VITA 67.3C

Input Type: Transformer-coupled

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +4 dBm into 50 ohms

3 dB Passband: 300 MHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS42LB69

Sampling Rate: 10 MHz to 250 MHz

Resolution: 16 bits

Digital Downconverters (FPGA IP)

Quantity: Eight channels

Decimation Range: 2x to 32,768x in three stages of 2x to 32x

LO Tuning Freq. Resolution: 32 bits, 0 to fs

LO SFDR: >108 dB

Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: 18-bit coefficients, 24-bit output, user-programmable coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Source

On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz) or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz, received through the VITA 67.3C connector

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

Gate/Trigger In

Connector: VITA 67.3C

Level: LVTTL

Sync In

Connector: VITA 67.3C

Level: TTL

ARM Processor

Type: 64-bit Cortex-A53 core

Speed: 800 MHz

Memory: 4 Gb DDR3L SDRAM

Ethernet: 1 GigE on VPX-P1

Field Programmable Gate Array

Type: Xilinx Virtex UltraScale+ HBM XCVU37P

Speed: (standard) -1 speed grade

- Option -002: -2 speed grade

System Logic Cells: 2,852k

HBM DRAM: 8 GBytes

Total Block RAM: 70.9 Mb

UltraRAM: 270.0 Mb

DSP Slices: 9,024

FPGA I/O

Interface: GPIO

- Quantity: 2 pairs
- Type: LVDS
- Location: VPX-P1

Interface: 10 GigE

- Location: VPX-P1

Interface: 40 GigE

- Location: VPX-P1

Interface: Optical (Option -108)

- Quantity: 8 full duplex lanes
- Speed: 28 Gb/sec
- Laser: 850 nm
- Location: VITA 67.3C (VPX-P2)

Interface: PCI-Express

- Type: Gen 1, 2, or 3: x4
- Location: VPX-P1

FPGA Configuration FLASH:
2x 1 Gbit QSPI

Environmental

Option -763: L3a (conduction-cooled)

- Operating Temp: 0° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: VPX board

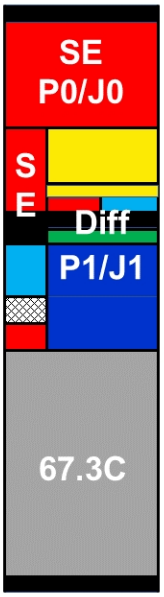
- Depth: 170.61 mm (6.717 in)
- Height: 100 mm (3.937 in)

Weight: TBD

OpenVPX Compatibility

The 5585 is compatible with the following module profile, as defined by the VITA 65 OpenVPX Specification:

SLT3-PAY-1F1U1S1S1U2F1H-14.6.11-12



ORDERING INFORMATION

Model	Description
5585	8-channel 250 MHz A/D SOSA aligned 3U VPX board with Virtex UltraScale+ HBM FPGA

Options:	
-002	-2 FPGA speed grade, -1 standard
-089	XCVU37P FPGA
-108	VITA 67.3C 8X optical interface
-114	VITA 67.3C with 8 A/D, External Clock/Reference, Trigger, Sync connections installed
-214	Alternate RF pin-out configuration
-763	Conduction-cooled, Level L3
Contact Mercury for compatible option combinations and complete specifications of rugged and conduction-cooled versions.	

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