Jade 57141A/58141A

1- or 2-channel 6.4 GHz A/D, 2- or 4-channel 3.2 GHz A/D, 4-channel 6.4 GHz D/A 6U VPX boards with Kintex UltraScale FPGA

Complete radar and software radio interface solution

- Radar and communication receiver and transmitter
- Electronic Warfare transponder
- Waveform signal generator
- Wideband data acquisition
- Remote monitoring
- Sensor interfaces

Jade® 57141A and 58141A consist of one or two 71141A XMC modules mounted on a VPX carrier board. The 57141A is a 6U board with one 71141A module while the 58141A is a 6U board with two XMC modules rather than one.

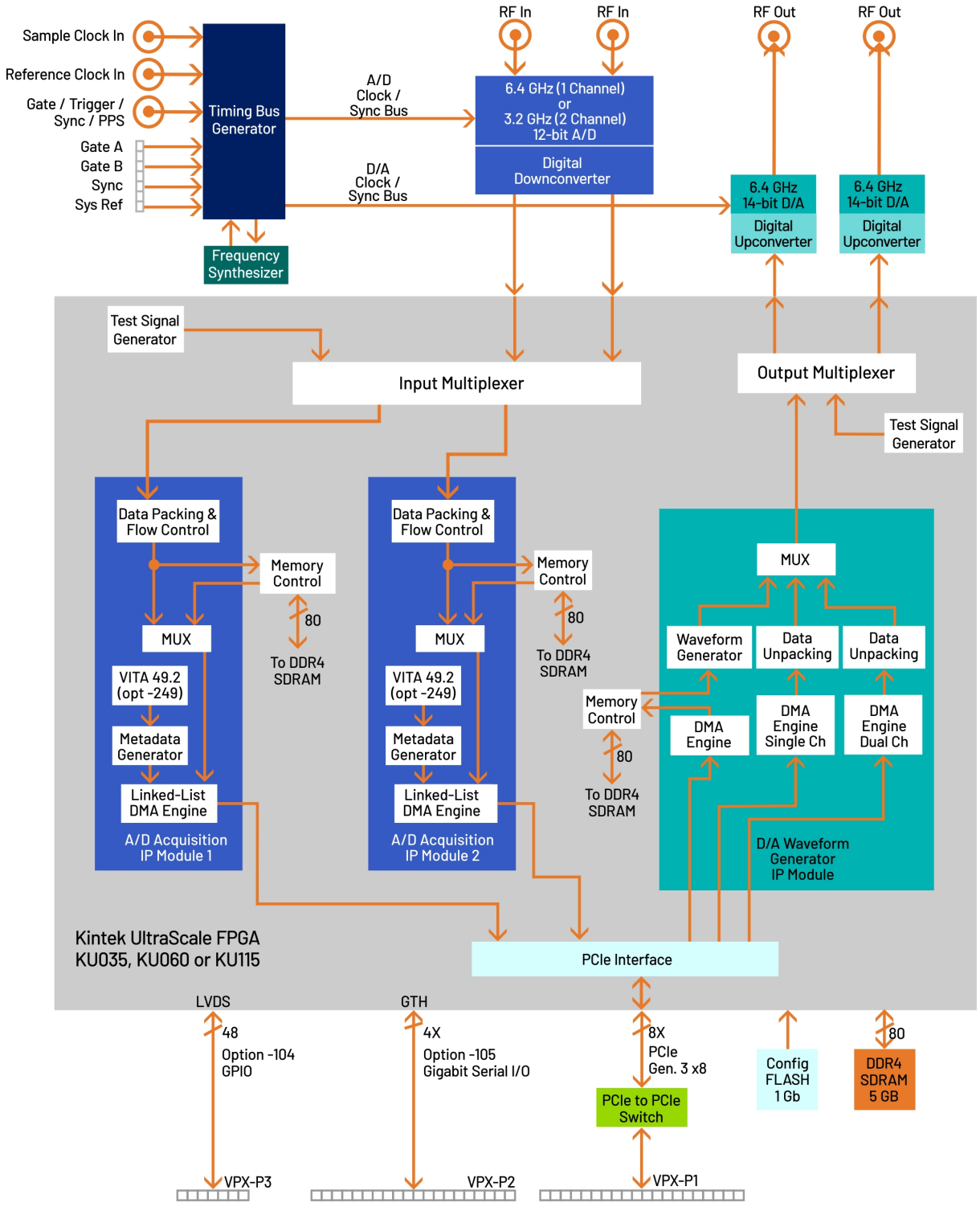
They include two or four A/Ds, complete multiboard clock and sync sections, large DDR4 memories, two or four DDCs, two or four DUCs and two or four D/As. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGAs for custom digital I/O.

FEATURES

- Xilinx® Kintex® UltraScale™ FPGA
- One- or two-channel mode with 6.4 GHz, 12-bit A/D
- Two- or four-channel mode with 3.2 GHz, 12-bit A/Ds
- Programmable DDCs (digital downconverters)
- Two- or four-channel 6.4 GHz, 14-bit D/As
- Programmable DUCs (digital upconverters)
- 5 GB of 2400 MHz DDR4 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express interface (Gen. 1, 2 & 3) up to x8
- Optional LVDS port and gigabit serial connections for custom FPGA I/O
- Compatible with VITA-46, VITA-48 and VITA-65 (OpenVPX™ Specification)
- Ruggedized and conduction-cooled versions
- Navigator Design Suite for software and custom IP development

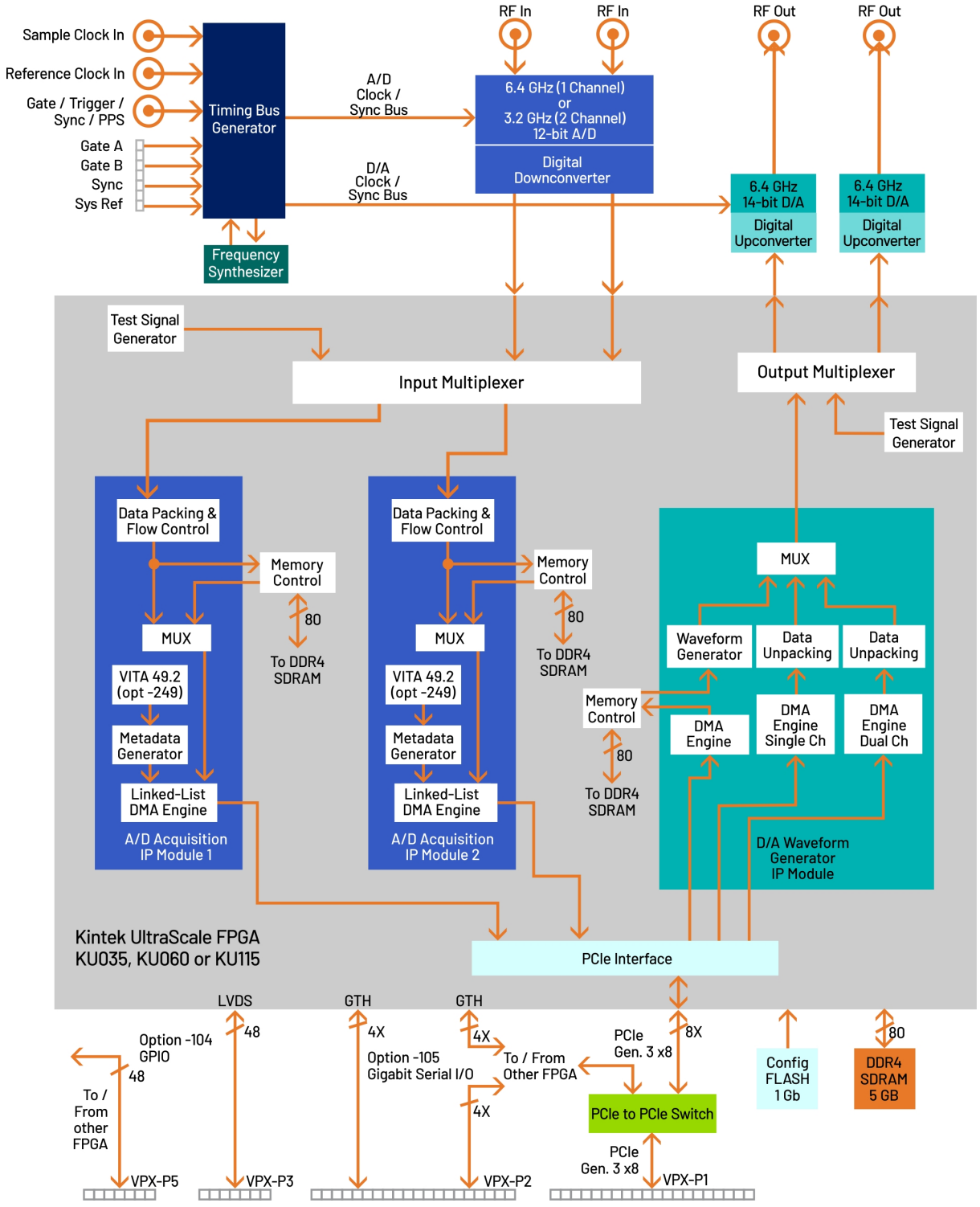
57141A BLOCK DIAGRAM

Click on a block for more information.



58141A BLOCK DIAGRAM

Block diagram shows half of the 58141A. All resources are actually double of what is shown except for the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5.



THE JADE ARCHITECTURE

Evolved from the proven designs of the Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces.

XILINX KINTEX ULTRASCALE FPGAS

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs: KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

A/D CONVERTER STAGE

The board's analog interface accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer-coupling into a Texas Instruments ADC12DJ3200 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 6.4 GHz and an input bandwidth of 7.9 GHz; or, in dual-channel mode with a sampling rate of 3.2 GHz and input bandwidth of 8.1 GHz.

The A/D built-in digital down-converters (DDCs) support 2x decimation in real output mode and 4x, 8x, or 16x decimation in complex output mode. The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other module resources.

A/D ACQUISITION IP MODULES

These models feature two or four A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP modules have associated 5 or 10 GB of DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A WAVEFORM GENERATOR IP MODULE

These models support factory-installed functions which include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the D/As waveforms stored in either on-board memory or off-board host memory.

DIGITAL UPCONVERTER AND D/A STAGE

A Texas Instruments DAC38RF82 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals. It delivers real or quadrature (I+Q) analog outputs to the dual 14-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC38RF82 acts as a dual interpolating 14-bit D/A. In both modes the DAC38RF82 provides interpolation factors from 1x to 24x.

CLOCKING AND SYNCHRONIZATION

These models accept a sample clock via front panel SSMC connectors. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. The Model 5792 high-speed sync board can be used to drive the sync bus to synchronize multichannel systems.

MEMORY RESOURCES

The architecture supports 5 or 10 GB bank of DDR4 SDRAM memory. User-installed IP along with the Mercury-supplied DDR4 controller core(s) within the FPGA can take advantage of the memory for custom applications.

PCI EXPRESS INTERFACE

The 57141A & 58141A include industry standard interface fully compliant with PCI Express Gen. 1, 2, and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

6U VPX INTERFACE

The 57141A & 58141A comply with the VITA 65.0 6U VPX specification. In addition to supporting PCIe Gen. 3, x8 on the VPX P1 connector, option -105 adds additional gigabit serial lanes for supporting user-installed protocols. On the 57141A option -105 installs four lanes from the FPGA to the P2 connector. On the 58141A the option installs four lanes from each of the FPGAs to the P2 connector and an additional four lanes between the FPGAs.

The 57141A & 58141A offer flexible interface options for the VPX-P3 and -P5 to meet system-specific requirements.

On the 57141A option -104 installs 24 pairs of LVDS connections between the first FPGA to the P3 connector. On the 58141A the option installs an addition 24 pairs between the second FPGAs and the P5 connector.

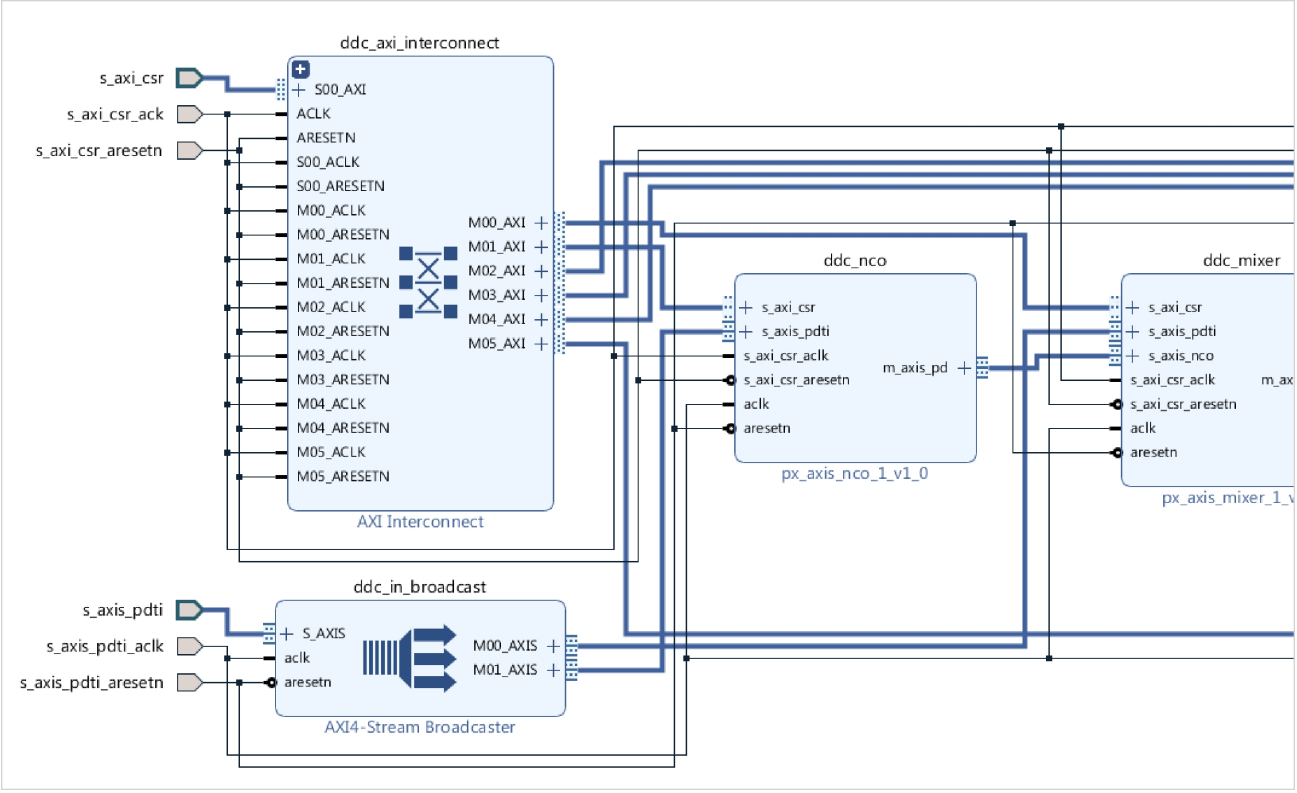
NAVIGATOR DESIGN SUITE

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into the factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

The **Navigator FPGA Design Kit (FDK)** for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Jade product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Jade design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations.

Navigator FDK includes an IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.

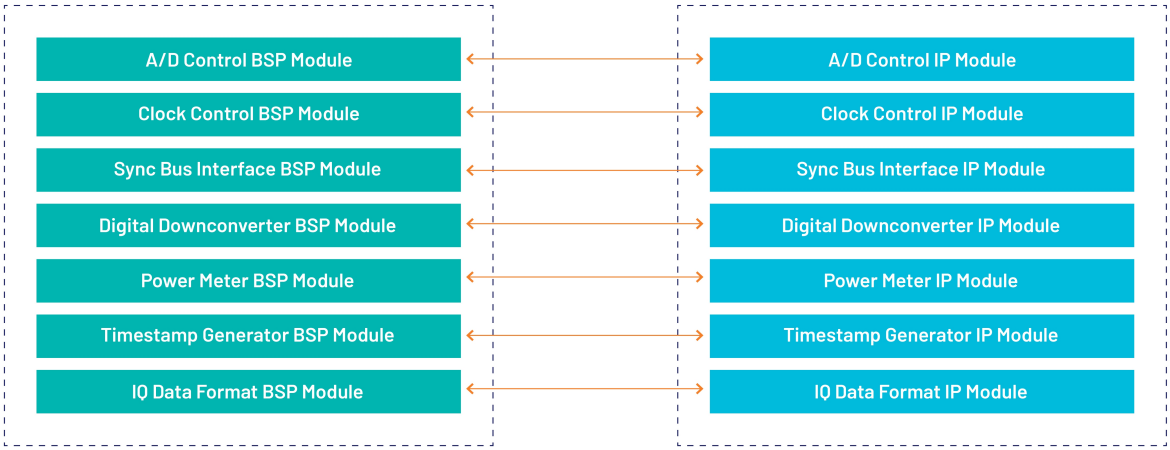
The **Navigator Board Support Package (BSP)** provides software support for Jade boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA. The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.



Navigator IP FPGA Design viewed in IP Integrator

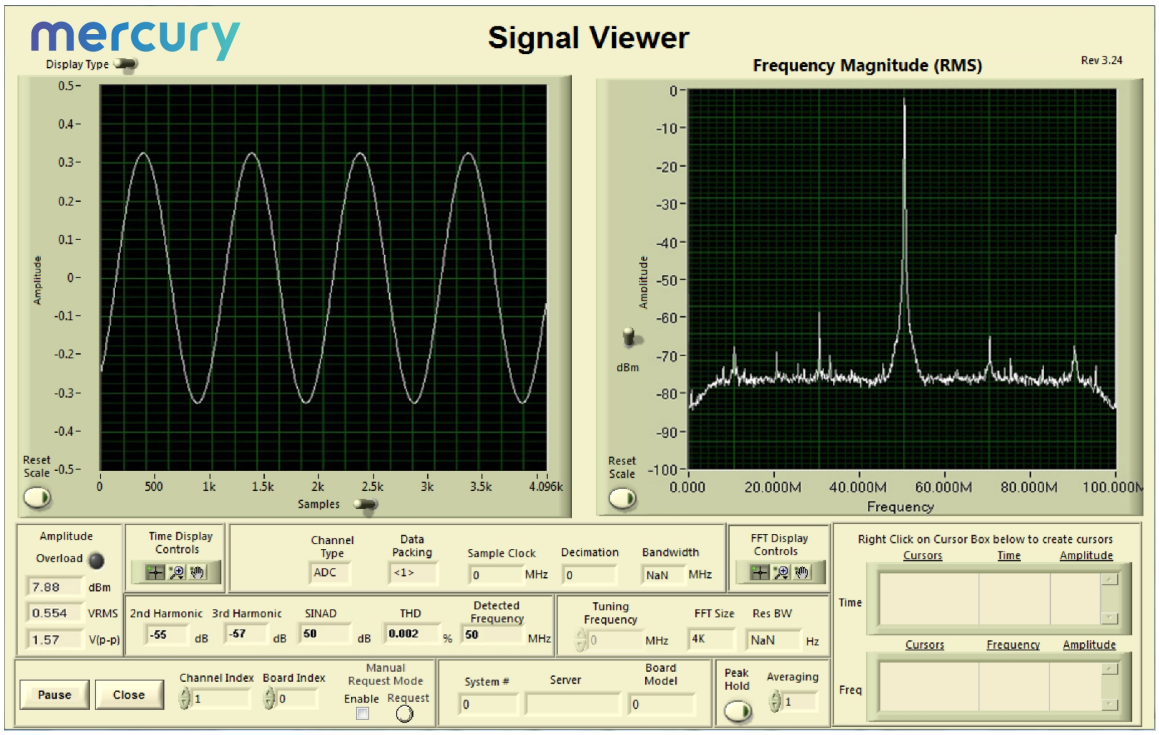
NAVIGATOR BOARD SUPPORT PACKAGE

NAVIGATOR FPGA DESIGN KIT



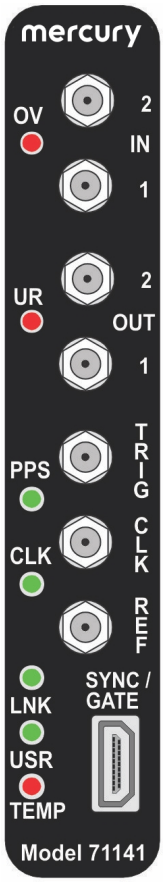
Because all Jade boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the **Signal Viewer**, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Jade board and Navigator BSP and start viewing analog signals immediately.



FRONT PANEL CONNECTIONS

The front panel includes seven SSMC coaxial connectors for input/output of analog RF, clock, and trigger, signals, and a 12-pin Sync Bus input connector. The front panel also includes seven LED indicators.



- **ADC Overload LED:** There is one red **OV** (overload) LED for all ADC inputs. This LED indicates either an overload detection in one of the ADC12DJ3200s, or an ADC FIFO overrun.
- **Analog Input Connectors:** Two SSMC coaxial connectors, labeled **In 1** and **IN 2**: one for each ADC input channel.
- **DAC Underrun LED:** One red underrun **UR** LED for both DAC outputs. This LED illuminates when the DAC38RF82 FIFO is out of data.
- **Analog Output Connectors:** Two SSMC coaxial connectors, labeled **OUT 1** and**OUT 2**: one for each DAC38RF82 output channel.
- **PPS LED:** The green **PPS** LED illuminates when a valid PPS signal is detected. The LED will blink at the rate of the PPS signal.
- **Trigger Input Connector:** One SSMC coaxial connector, labeled **TRIG**, for input of an external trigger.
- **Clock LED:** The green **CLK** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.
- **Clock Input Connector:** One SSMC coaxial connector, labeled **CLK**, for input of an external sample clock.
- **Reference Clock Input Connector:** The SSMC coaxial connector, labeled **REF**, for input of an external reference clock.
- **Link LED:** The green **LNK** LED indicates the link speed when a valid link has been established over the PCIe interface, as follows: Gen 1 - LED blinks slowly (less than once per second); Gen 2 - LED blinks about once per second; Gen 3 - LED will be constantly on.
- **Sync Bus Connector:** The 19-pin µSync front panel connector, labeled **SYNC/GATE**, provides sync and gate input signals for A/D and D/A Processing.
- **User LED:** The green **USR** LED is for user applications.
- **Over Temperature LED:** The red TMP LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the PCB.

SPECIFICATIONS

Model 57141A One A/D; Model 58141A Two A/Ds

Front Panel Analog Signal Inputs (2 or 4)

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converters (1 or 2)

Type: ADC12DJ3200

Sampling Rate: Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz

Resolution: 12 bits

Input Bandwidth: single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz

D/A Converters (2 or 4)

Type: Texas Instruments DAC38RF82

Output Sampling Rate: 6.4 GHz.

Resolution: 14 bits

Sample Clock Source (1 or 2)

Front panel SSMC connector

Timing Bus (1 or 2)

19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input (1 or 2)

Type: Front panel female SSMC connector, LVTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)

Standard: Xilinx Kintex UltraScale XCKU035-2

Option -084: Xilinx Kintex UltraScale XCKU060-2

Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O

Option -104: provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57141A; P3 and P5 connectors, Model 58141A.

Option -105: provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols.

Memory (1 or 2)

Type: DDR4 SDRAM

Size: 5 or 10 GB

Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: VPX board

- Depth: 233.35 mm (9.187 in)
- Height: 170.60 mm (6.717 in)

Weight: Approximately 14 oz (400 grams)

ORDERING INFORMATION

Model	Description
57141A	1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - 6U VPX
58141A	2-Ch. 6.4 GHz or 4-Ch. 3.2 GHz A/D, 4-Ch. 6.4 GHz D/A, 2 ea. UltraScale FPGAs - 6U VPX

Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-105	Gigabit serial FPGA I/O
-702	Air-cooled, Level 2
-763	Conduction-cooled, Level 3

Contact Mercury for compatible option combinations and complete specifications of rugged and conduction-cooled versions. Options may change, so be sure to contact Mercury for the latest information.

ACCESSORY PRODUCTS

Model	Description
2171	Cable Kit: SSMC to SMA

Model	Description
5792/5892	System Synchronizer and Distribution Board
5794/5894	High-Speed Clock Generator
9192	Rackmount high-speed system synchronizer

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Learn more

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