Cobalt 57671/58671

4- or 8-channel 1.25 GHz D/A with DUC, extended interpolation 6U VPX boards with Virtex-6 FPGA

Complete radar and software radio interface solution

- Radar and software radio transmitter
- Communications transmitter
- Electronic Warfare transponder
- Waveform signal generator
- Sensor interfaces

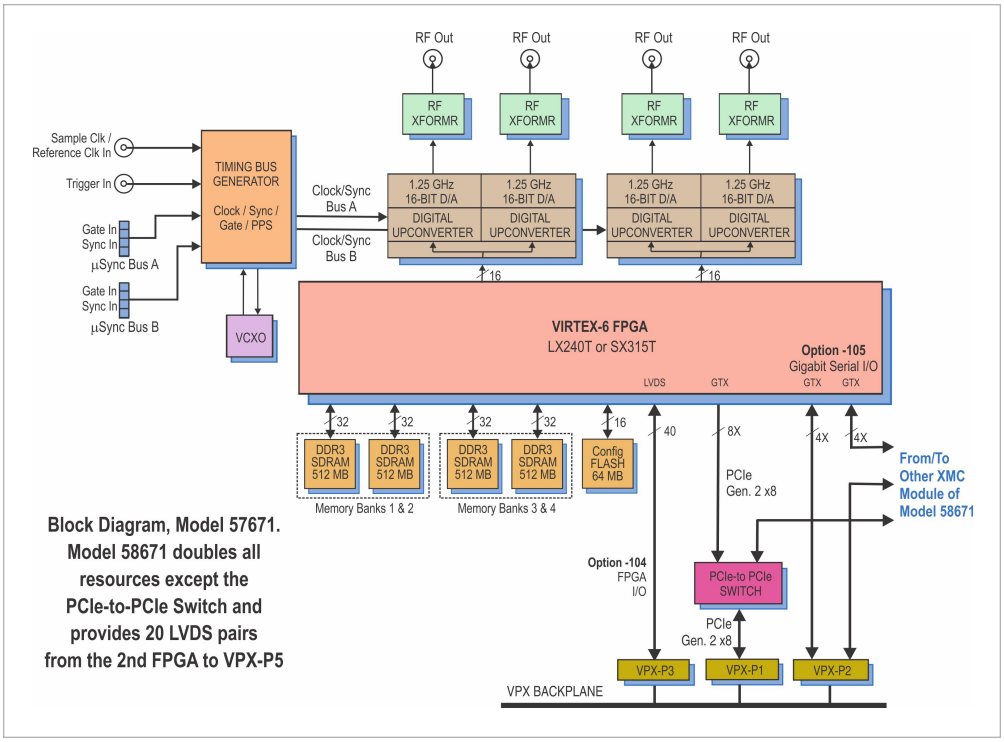
Cobalt 57671 and 58671 consist of one or two 71671 XMC modules mounted on a VPX carrier board. The 57671 is a 6U board with one 71671 module while the 58671 is a 6U board with two XMC modules rather than one.

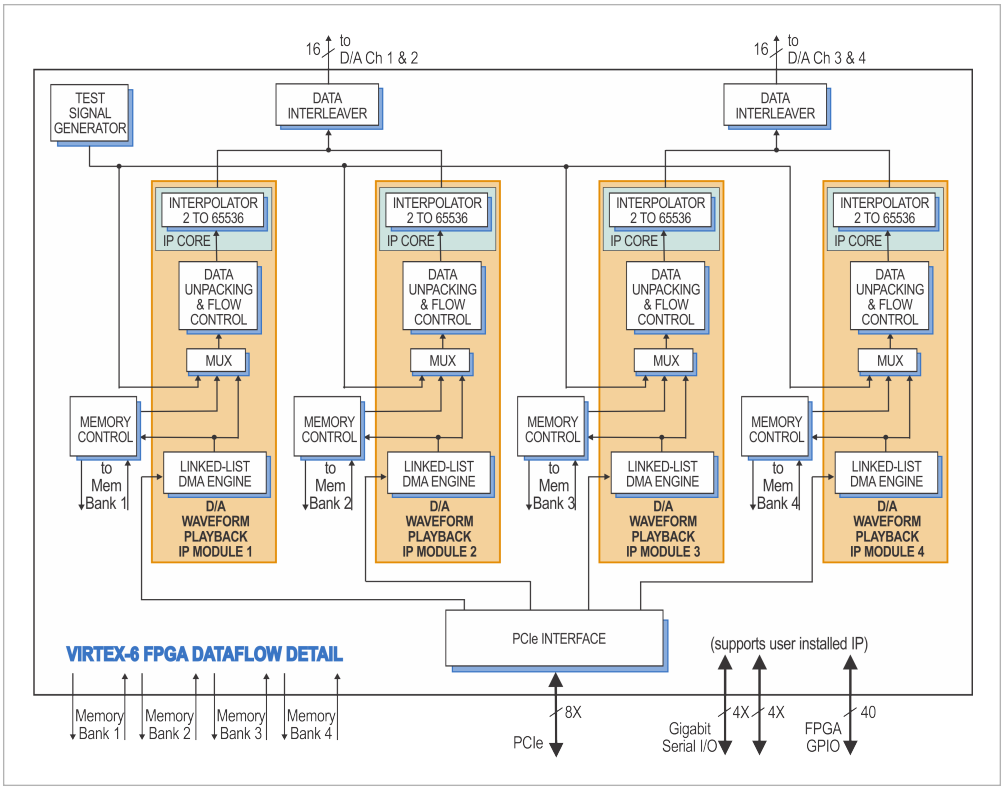
These models include four or eight D/As with a wide range of programmable interpolation factors, four or eight DUCs, and four or eight banks of memory.

FEATURES

- Supports Xilinx® Virtex®-6 LXT and SXT FPGA
- Four or eight 1.25 GHz 16-bit D/As
- Four or eight DUCs (digital upconverters)
- Extended interpolation range from 2x to 1,048,576x
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 or 4 GB of DDR3 SDRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- Dual-or Quad µSync clock/ sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

BLOCK DIAGRAMS





THE COBALT ARCHITECTURE

The Cobalt® Architecture features a Xilinx Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions in these models include four or eight D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. The GateFlow FPGA Design Kits include all of the factory-installed modules as document source code. Developers can integrate their own IP with the factory-installed functions or use the GateFlow kit to completely replace the IP with their own.

XILINX VIRTEX-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

DIGITAL UPCONVERTER AND D/A STAGE

Two or four Texas Instruments DAC3484s provide four or eight DUCs (digital upconverters) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGAs and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. In addition to the DAC3484, these models feature an FPGA-based interpolation engine which adds two additional interpolation stages programmable from 2x to 256x. The combined interpolation results in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems. Analog outputs are through front panel SSMC connectors.

D/A WAVEFORM PLAYBACK IP MODULE

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. Four or eight linked list controllers support waveform generation to the four or eight D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/ gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4, as well as to the other four channels of Model 57671.

Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel. Up to 64 or 128 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.

CLOCKING AND SYNCHRONIZATION

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board's sync and trigger/gate signals. The Mercury model 9192 Cobalt Synchronizer can drive multiple 57671 µSync connectors enabling large, multichannel synchronous configurations.

MEMORY RESOURCES

The architecture of these models supports four or eight independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked-list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI EXPRESS INTERFACE

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

READYFLOW

Mercury provides ReadyFlow® BSPs (Board Support Packages) for all Cobalt, Onyx, and Flexor products. Available for both Linux and Windows, these packages:

- Provide a path for quick start-up through application completion
- Allow programming at high, intermediate and low levels to meet various needs
- Are illustrated with numerous examples
- Include complete documentation and definitions of all functions
- Include library and example source code.

ReadyFlow BSPs contain C-language examples that can be used to demonstrate the capabilities of Cobalt, Onyx, and Flexor products. These programming examples will help you get an immediate start on writing your own application. They provide sample code that is known to work, giving you a means of verifying that your board set is operational.

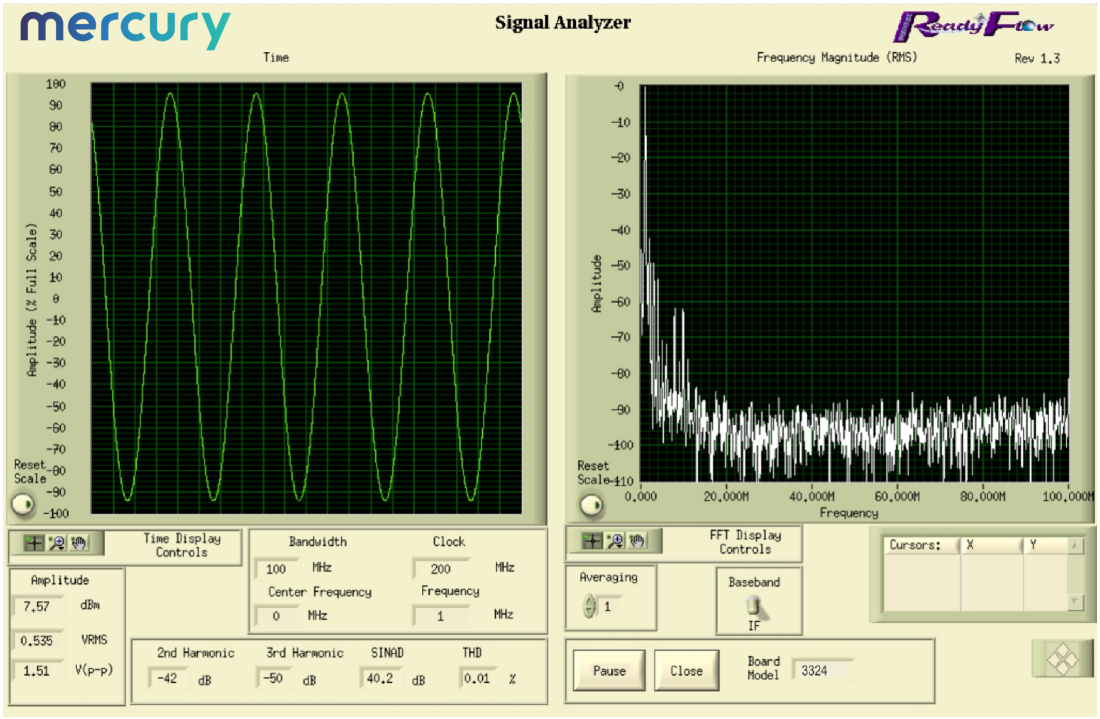
COMMAND LINE INTERFACE

The Command Line Interface provides access to pre-compiled executable examples that operate the hardware right out of the box, without the need to write any code. Board-specific hardware operating arguments can be entered in the command line to control parameters: number of channels to enable, sample clock frequency, data transfer size, reference clock frequency, reference clock source, etc.

The Command Line Interface can be used to call an example application from within a larger user application to control the hardware, and parameter arguments are passed to the application for execution. Functions that control data acquisition automatically save captured data to a pre-named host file or are routed to the Signal Analyzer example function for display.

SIGNAL ANALYZER

When used with the Command Line Interface, the Signal Analyzer allows users to immediately start acquiring and displaying A/D data. A full-featured analysis tool, the Signal Analyzer displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD, and SINAD. Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals.



GATEFLOW

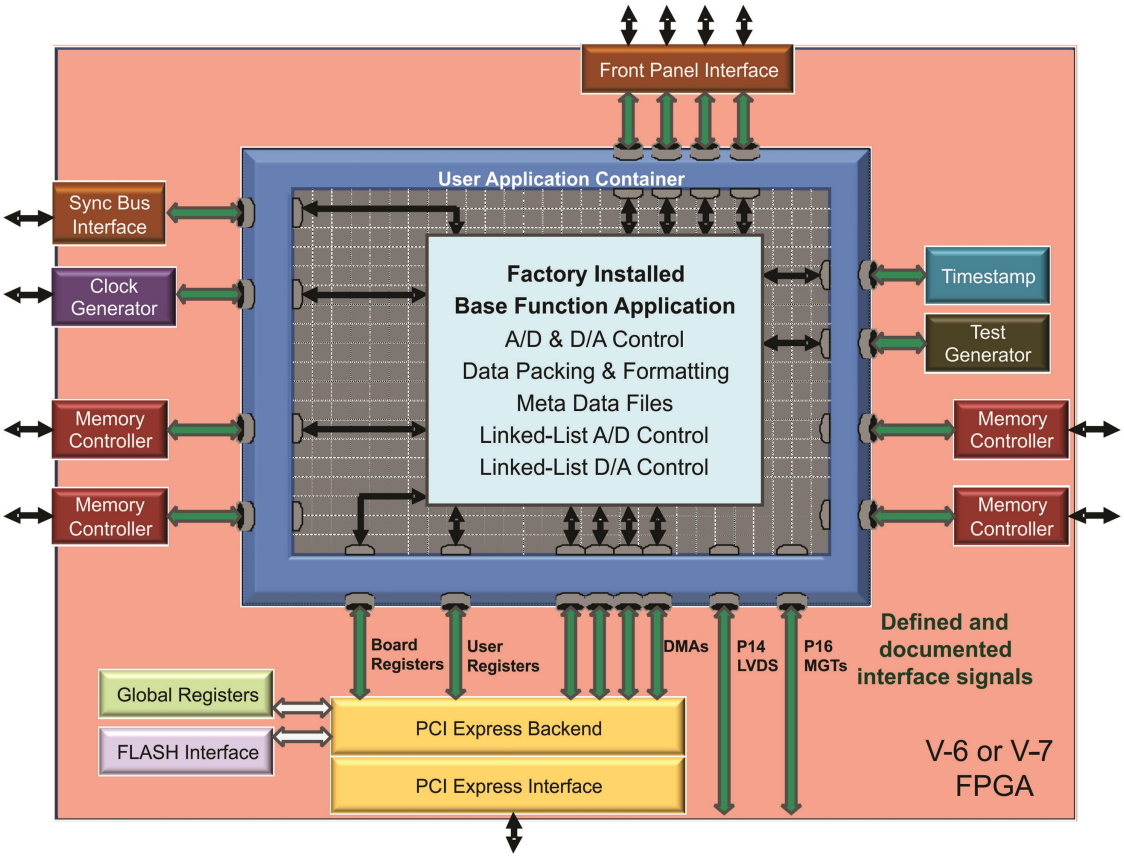
The GateFlow® FPGA Design Kit (FDK) allows the user to modify, replace and extend the standard installed functions in the FPGA to incorporate special modes of operation, new control structures, and specialized signal-processing algorithms.

The Cobalt (Virtex-6), Onyx (Virtex-7), and Flexor (Virtex-7) architectures configure the FPGA with standard factory-supplied interfaces including memory controllers, DMA engines, A/D and D/A interfaces, timing and synchronization structures, triggering and gating logic, time stamping and header tagging, data formatting engines, and the PCIe interface. These resources are connected to the User Application Container using well-defined ports that present easy-to-use data and control signals, effectively abstracting the lower-level details of the hardware.

The User Application Container

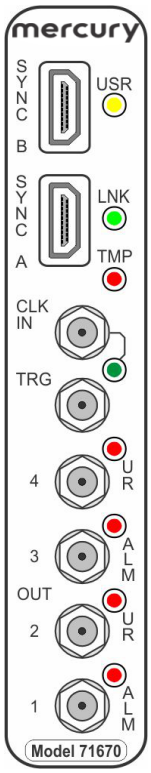
Shown below is the FPGA block diagram of a typical Cobalt, Onyx or Flexor module. The User Application Container holds a collection of different installed IP modules connected to the various interfaces through the standard ports surrounding the container. The specific IP modules for each product are described in further detail in the datasheet of that product.

The GateFlow FDK provides a complete Xilinx's ISE or Vivado project folder containing all the files necessary for the FPGA developer to recompile the entire project with or without any required changes. VHDL source code for each IP module provides excellent examples of how the IP modules work, how they might be modified, and how they might be replaced with custom IP to implement a specific function.



FRONT PANEL CONNECTIONS

The XMC front panel includes six SSMC coaxial connectors, and two 19-pin µSync connectors for input/output of timing and analog signals. The front panel also includes eight LEDs.



- **Sync Bus Connector:** The 19-pin Sync Bus front panel connectors labeled **SYNC A** and **SYNC B**, provides sync and gate inputs for DAC timing control. The **SYNC A** connector includes an external 2.5V CML sync clock input.
- **USR LED:** The green **USR** LED is for user applications.
- **Link LED:** The green **LNK** LED blinks when a valid link has been established over the PCIe interface.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the PCB.
- **Clock Input Connector:** One SSMC coaxial connector, labeled **CLK IN** for the input of an external sample or reference clock.
- **Clock LED:** The green **CLK IN** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.
- **Trigger Input Connector:** The front panel has one SSMC coaxial connector, labeled **TRG**, for input of an external gate or trigger TTL signal.
- **Analog Output Connectors:** Four SSMC coaxial connector, labeled **OUT 1, 2, 3,** and **OUT 4** for analog signal outputs , one for each DAC3484 output.
- **DAC Underrun LEDs:** There are two red **UR** underrun LEDs, one for each DAC3484 device. The **UR** LED next to **OUT 2** is for DAC3484 A; the **UR** LED next to **OUT 4** is for DAC3484 B. Each LED illuminates when the associated DAC Channel FIFO is out of data.
- **DAC Alarm LEDs:** The two red **ALM** alarms are for each DAC3484 device. The ALM LED next to **OUT 1** is for DAC3484 A; the ALM LED next to **OUT 3** is for DAC3484 B. Each LED illuminates when the associated DAC3484 Alarm output is active.

SPECIFICATIONS

57671: 4-Channel DUC, 4-channel D/A;
58671: 8-Channel DUC, 8-channel D/A

D/A Converters (4 or 8)

Type: Texas Instruments DAC3484

Input Data Rate: 312.5 MHz max.

Output Bandwidth: 250 MHz max.

Output Sampling Rate: 1.25 GHz max. with interpolation

Interpolation: 2x, 4x, 8x or 16x

Resolution: 16 bits

Digital Interpolator

Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Front Panel Analog Signal Outputs (4 or 8)

Quantity: Four D/A outputs

Output Type: Transformer-coupled, front panel female SSMC connectors

Full Scale Output: Programmable from -20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps

Full Scale Output Programming: 1.0x (G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizers (1 or 2)

Clock Source: Selectable from on-board programmable VCXO or front panel external clock

VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz

Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clocks (1 or 2)

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Inputs (1 or 2)

Type: Front panel female SSMC connector

Function: Programmable functions include: trigger, gate, sync and PPS

Timing Bus (1 or 2)

19-pin µSync bus connector includes sync and gate/trigger inputs, CML

Field Programmable Gate Arrays (1 or 2)

- Standard: Xilinx Virtex-6 XC6VLX240T-2
- Optional: Xilinx Virtex-6 XC6VSX315T-2

Custom I/O

- Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, 57671; P3 and P5, 58671
- Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, 57671; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, 58671

Memory Banks (1 or 2)

Four or eight 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI Express Interface

PCI Express Bus: Gen. 1 or Gen 2: x4 or x8

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions:

- Depth: 171 mm (6.717 in.)
- Height: 100 mm (3.937 in.)

Weight: VPX Carrier: 110 grams (3.9 oz)

ORDERING INFORMATION

Model	Description
57671	4-Channel 1.25 GHz D/A with DUC, extended interpolation and Virtex-6 FPGA - 6U VPX
58671	8-Channel 1.25 GHz D/A with DUC, extended interpolation and two Virtex-6 FPGAs - 6U VPX

Options	Description
-002*	-2 FPGA speed grade
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and P3 connector, 57671; P3 and P5 connectors, 58671
-105	Gigabit link between the FPGA and P2 connector, 57671; gigabit links from each FPGA to P2 connector, 58671
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
-702	Air-cooled, Level 2
-763	Conduction-cooled, Level 3

*This option is always required. Contact Mercury for compatible option combinations.

ACCESSORY PRODUCTS

Model	Description
2171	Cable Kit: SSMC to SMA
9192	Rackmount High-Speed System Synchronizer

DEVELOPMENT SYSTEMS

Mercury offers development systems for Cobalt products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Cobalt boards. Please contact Mercury to configure a system that matches your requirements.

FORM FACTORS

Cobalt products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Cobalt Model 71671 XMC (4-Channel 1.25 GHz, 16-bit D/A with DUC, Extended Interpolation, Virtex-6) has the following variants:

Model	
52671	3U VPX board (single XMC with optical/backplane RF)
57671	6U VPX board (single XMC)
58671	6U VPX board (dual XMC)
71671	XMC module
78671	PCIe board (single XMC)

LIFETIME SUPPORT FOR COBALT PRODUCTS

Mercury offers worldwide customers shorter development time, reliable, rugged solutions for a variety of environments, reduced costs, and mature software development tools. We offer free lifetime support from our engineering staff, which customers can depend on through phone and email, as well as software updates. Take advantage of our 40 years of experience in delivering high-performance radar, communications, SIGINT, EW, and data acquisition MIL-Aero solutions worldwide.

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