Jade 57800/58800

Coprocessor
6U VPX boards with Kintex UltraScale FPGA

High-performance co-processor platform

- Front panel digital I/O can be used as a status and control or data interface
- PCI Express interface (Gen. 1, 2, and 3) up to x8
- Optional LVDS port and gigabit serial connections for custom FPGA I/O
- Ruggedized and conduction-cooled versions

Jade® 57800 and 58800 consist of one or two 71800 XMC modules mounted on a VPX carrier board. The 57800 is a 6U board with one 71800 module while the 58800 is a 6U board with two XMC modules rather than one.

In addition to supporting PCI Express Gen. 3 as a native interface, the 57800 and 58800 include optional high-bandwidth serial and parallel connections to the Kintex UltraScale FPGA for custom digital I/O.

THE JADE ARCHITECTURE

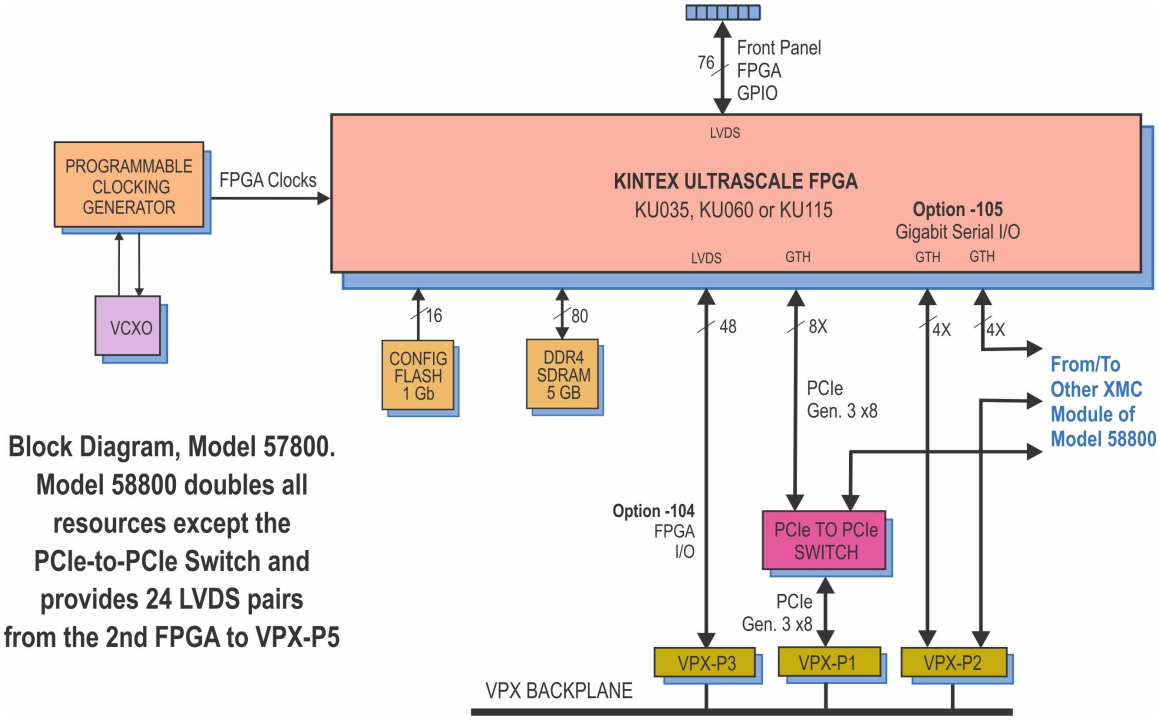
Evolved from the proven designs of Mercury's Cobalt® and Onyx® families, Jade® raises the processing performance while lowering the overall power requirements by building on the Xilinx family of Kintex UltraScale FPGAs. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions as well as providing an ideal platform for user-created intellectual property (IP). Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's interfaces.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's interfaces. The 78800 factory-installed functions include a test signal generator, a metadata generator, a DDR4 SDRAM controller, and DMA engines for moving data on and off the board.

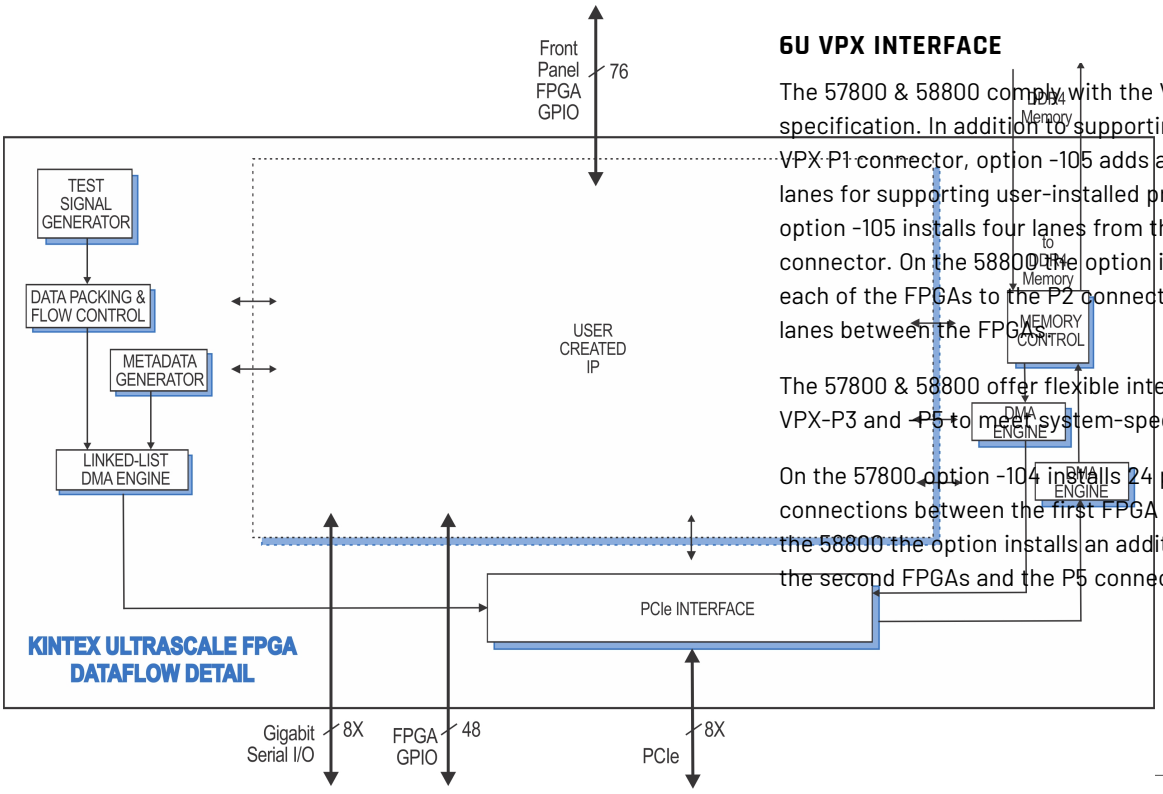
XILINX KINTEX ULTRASCALE FPGAS

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs: KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

57800 BLOCK DIAGRAM



Block Diagram, Model 57800. Model 58800 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5



6U VPX INTERFACE

The 57800 & 58800 comply with the VITA 65.0 6U VPX specification. In addition to supporting PCIe Gen. 3, x8 on the VPX P1 connector, option -105 adds additional gigabit serial lanes for supporting user-installed protocols. On the 57800 option -105 installs four lanes from the FPGA to the P2 connector. On the 58800 the option installs four lanes from each of the FPGAs to the P2 connector and an additional four lanes between the FPGAs.

The 57800 & 58800 offer flexible interface options for the VPX-P3 and P5 to meet system-specific requirements.

On the 57800 option -104 installs 24 pairs of LVDS connections between the first FPGA to the P3 connector. On the 58800 the option installs an addition 24 pairs between the second FPGAs and the P5 connector.

FRONT PANEL DIGITAL I/O INTERFACE

These models include one or two 80-pin front panel connectors that provide 38 or 76 LVDS pairs connected to one or both of the FPGAs. With user IP, these can be utilized for a control and status interface to other components of the system or as a data path.

Kintex UltraScale FPGA Resources			
	XCKU035	XCKU060	XCKU115
System Logic Dells	444,000	726,000	1,451,000
DSP Slices	1,700	2,760	5,520
Block RAM (Mb)	19.0	38.0	75.9

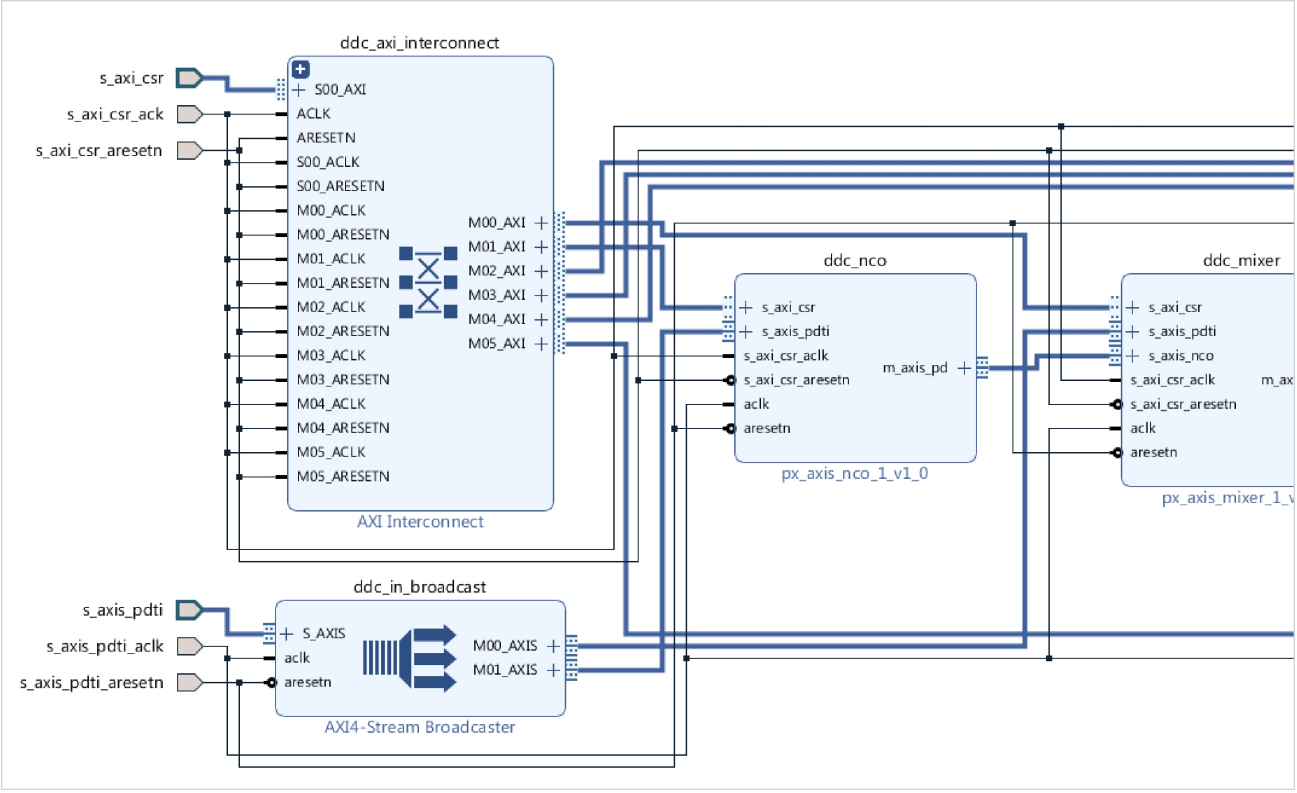
NAVIGATOR DESIGN SUITE

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into the factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

The **Navigator FPGA Design Kit (FDK)** for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Jade product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Jade design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations.

Navigator FDK includes an IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.

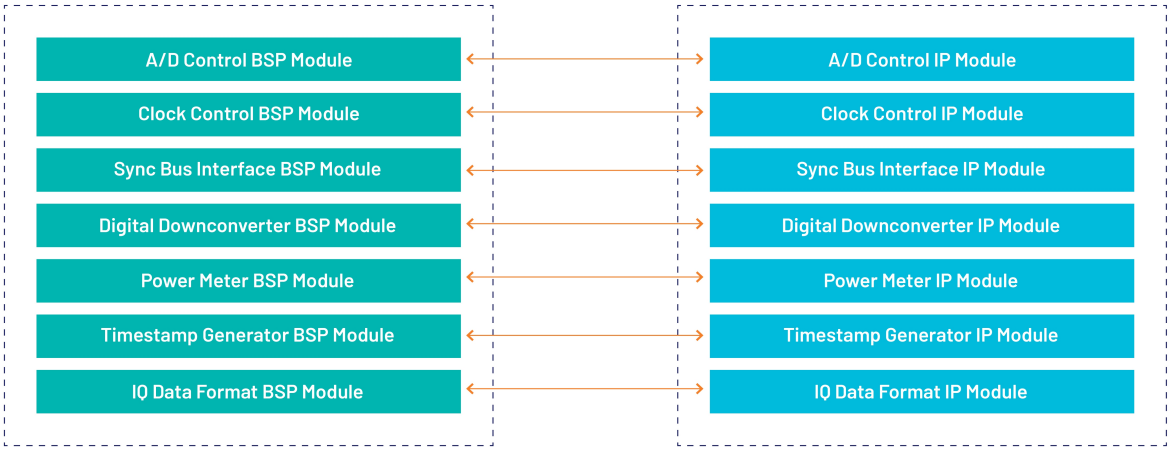
The **Navigator Board Support Package (BSP)** provides software support for Jade boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA. The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.



Navigator IP FPGA Design viewed in IP Integrator

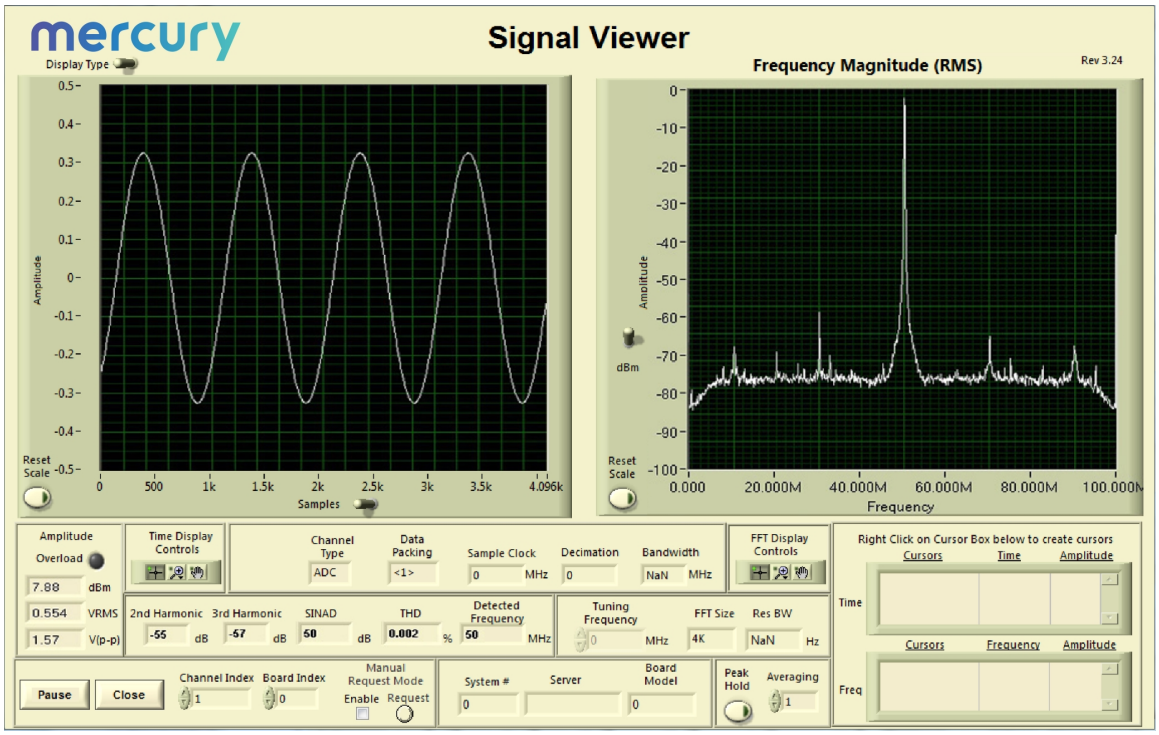
NAVIGATOR BOARD SUPPORT PACKAGE

NAVIGATOR FPGA DESIGN KIT



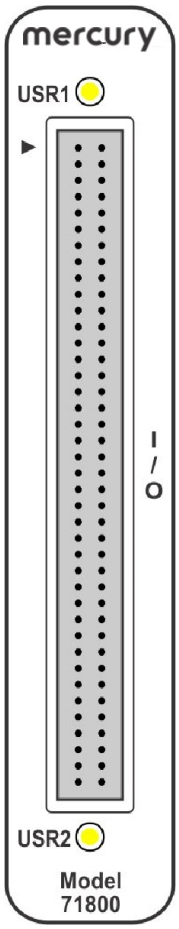
Because all Jade boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the **Signal Viewer**, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Jade board and Navigator BSP and start viewing analog signals immediately.



FRONT PANEL CONNECTIONS

The front panel includes a 80-pin digital input/output connector and two LED indicators.



- **User LEDs:** The two yellow **USR 1** and **USR 2** LEDs indicate Input/Output operating status.
- **Digital I/O Connector:** The 80-pin connector provides 32 digital input/output Data bits, Clock, Data Valid, and Data suspend signals. Three pairs of spare pins are available for user applications.

SPECIFICATIONS

Front Panel Digital I/O (1 or 2)

Connector Type: 80-pin connector, mates to a ribbon cable connector

Signal Quantity: 38 or 76 pairs

Signal Type: LVDS

Field Programmable Gate Array (1 or 2)

Standard: Xilinx Kintex UltraScale XCKU035-2

Option -084: Xilinx Kintex UltraScale XCKU060-2

Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O (1 or 2)

Option -104: provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57800; P3 and P5 connectors, Model 58800

Option -105: provides two 4X gigabit serial connections between the FPGA and the VPX P2 connector to support serial protocols

Memory (1 or 2)

Type: DDR4 SDRAM

Size: 5 GB

Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: VPX board

- Depth: 233.35 mm (9.187 in)
- Height: 170.60 mm (6.717 in)

Weight: Approximately 14 oz (400 grams)

ORDERING INFORMATION

Model	Description
57800	Kintex UltraScale FPGA Coprocessor - 6U VPX
58800	Double Kintex UltraScale FPGA Coprocessors - 6U VPX

Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-105	Gigabit serial FPGA I/O
-702	Air-cooled, Level 2
-763	Conduction-cooled, Level 3

Contact Mercury for compatible option combinations and complete specifications of rugged and conduction-cooled versions. Options may change, so be sure to contact Mercury for the latest information.

DEVELOPMENT SYSTEMS

Mercury offers development systems for Jade products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Jade boards. Please contact Mercury to configure a system that matches your requirements.

FORM FACTORS

Jade products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Jade Model 71800 XMC (Kintex UltraScale FPGA Coprocessor) has the following variants:

Model	
52800	3U VPX board (single XMC)
57800	6U VPX board (single XMC)
58800	6U VPX board (dual XMC)
71800	XMC module
78800	PCIe board (single XMC)

LIFETIME SUPPORT FOR JADE PRODUCTS

Mercury offers worldwide customers shorter development time, reliable, rugged solutions for a variety of environments, reduced costs, and mature software development tools. We offer free lifetime support from our engineering staff, which customers can depend on through phone and email, as well as software updates. Take advantage of our 40 years of experience in delivering high-performance radar, communications, SIGINT, EW, and data acquisition MIL-Aero solutions worldwide.

Corporate Headquarters
50 Minuteman Road
Andover, MA 01810 USA
+1 978.967.1401 tel
+1 866.627.6951 tel
+1 978.256.3599 fax

International Headquarters
Mercury International
Avenue Eugène-Lance, 38
PO Box 584
CH-1212 Grand-Lancy 1
Geneva, Switzerland
+41 22 884 5100 tel

Learn more

Visit: mrcy.com/go/MP57800

For technical details, contact:
mrcy.com/go/CF57800