Jade 54810

LVDS digital I/O
3U VPX board with Kintex UltraScale FPGA

High-performance offload co-processor

- Fully customizable I/O signal status and control interface
- Meets needs from low cost to high performance
- 38 pairs of Configurable LVDS Digital I/O
- Choice of FPGA resources

The Jade® 54810 is designed to work with the Navigator® Design Suite of tools. The combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data processing IP.

In addition to supporting PCI Express Gen. 3 as a native interface, the 54810 includes optional high-bandwidth serial and parallel connections to the Kintex UltraScale FPGA for custom digital I/O.

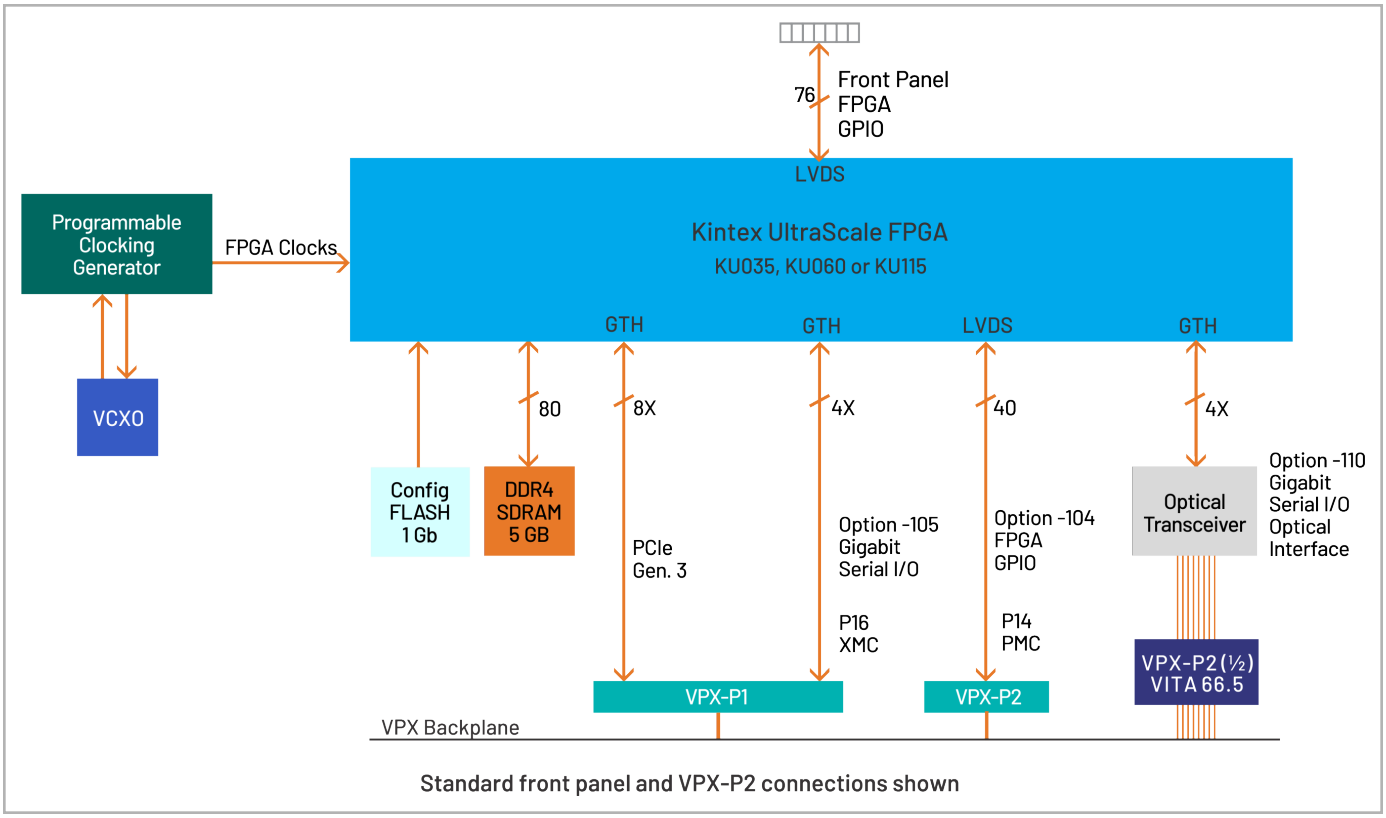
FEATURES

- Supports Xilinx® Kintex® UltraScale™ FPGA
- Front panel digital I/O can be used as a status and control or data interface
- PCI Express interface (Gen. 1, 2 & 3) up to x8
- Compatible with VITA-46, VITA-48 and VITA-65 (OpenVPX™ Specification)
- Optional LVDS and gigabit serial connections for custom FPGA I/O

THE JADE ARCHITECTURE

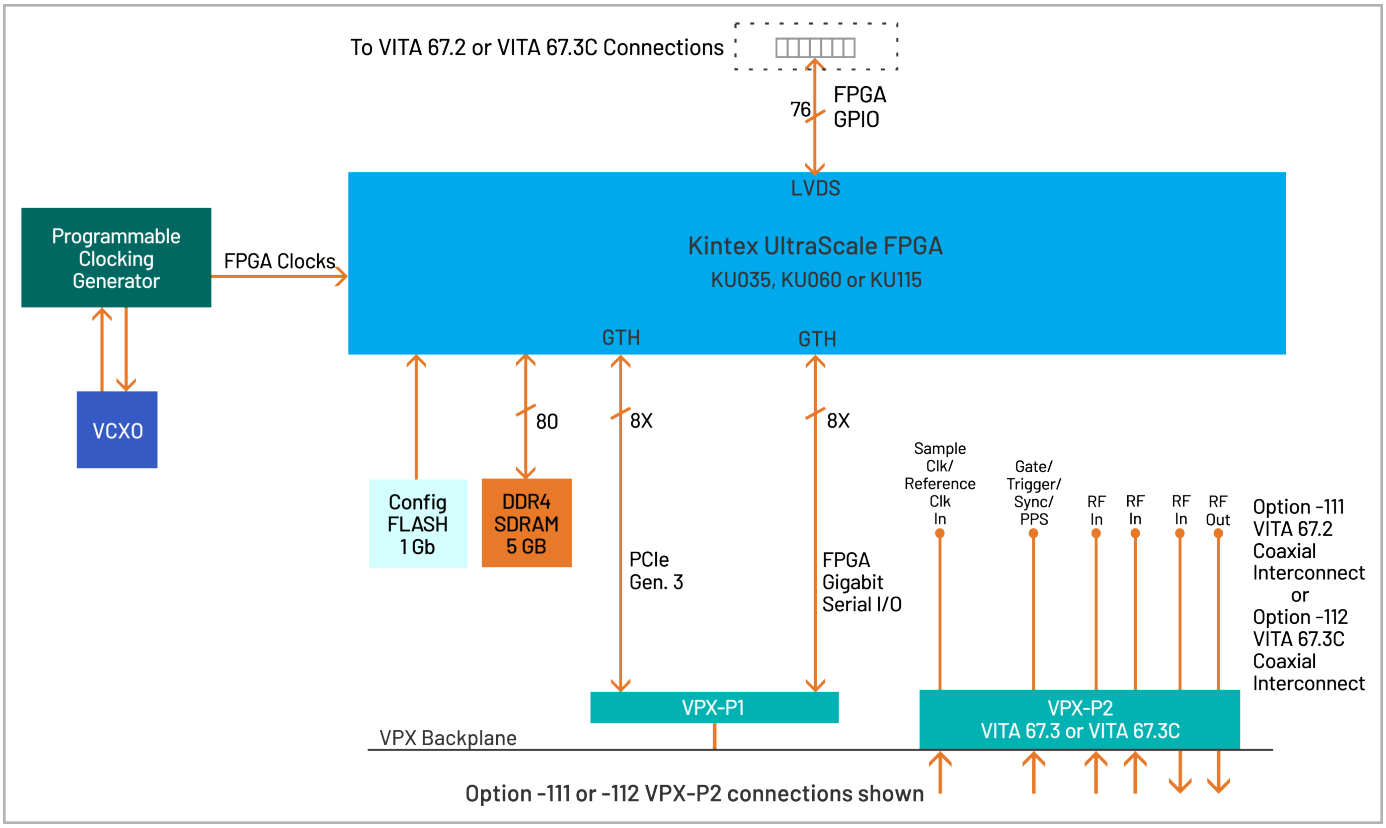
Evolved from the proven designs of Mercury's Cobalt® and Onyx® families, Jade® raises the processing performance while lowering the overall power requirements by building on the Xilinx family of Kintex UltraScale FPGAs. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions as well as providing an ideal platform for user-created intellectual property (IP).

54810 BLOCK DIAGRAM (STANDARD CONFIGURATION AND OPTION -109 SHOWN.)



Standard front panel and VPX-P2 connections shown

54810 BLOCK DIAGRAM (OPTIONS -111 AND -112 SHOWN.)



XILINX KINTEX ULTRASCALE FPGAS

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs: KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

FRONT PANEL DIGITAL I/O INTERFACE

The 54810 includes an 80-pin front panel connector that provides 38 LVDS pairs connected to the FPGA. With user IP, these can be utilized for a control and status interface to other components of the system or as a data path.

MEMORY RESOURCES

The 54810 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Mercury-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI EXPRESS INTERFACE

The 54810 includes an industry standard interface fully compliant with PCI Express Gen. 1, 2, and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

VPX-P2 INTERFACE OPTIONS

When purchased with option -110, the 54810 supports the emerging VITA 66.5 standard and provides four optical duplex lanes to a mating VITA 66.5 backplane connector. With the installation of a serial protocol like 10 or 40 Gigabit Ethernet in the FPGA, the VITA 66.5 interface enables high bandwidth communications between boards or chassis independent of the PCIe interface.

Options -111 and -112 provide analog signal routing through the VPX backplane. Both options replace front panel connectors for RF In, RF Out, Sample Clock/ Reference Clock In and Gate/Trigger/ Sync/PPS In with coax signals that pass through the backplane for connections to other boards or chassis. Option -111 is compatible with VITA 67.2 and option -112 is compatible with VITA 67.3C.

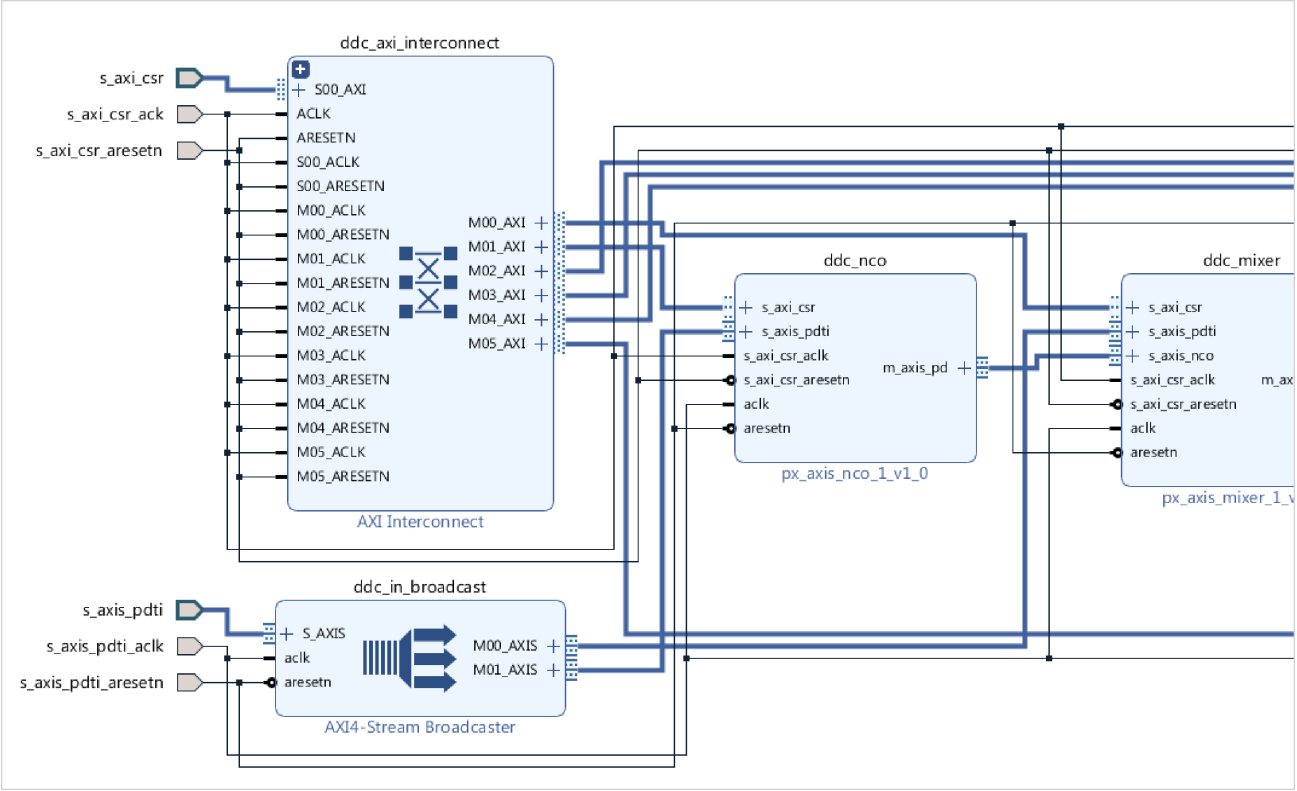
NAVIGATOR DESIGN SUITE

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into the factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

The **Navigator FPGA Design Kit (FDK)** for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Jade product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Jade design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations.

Navigator FDK includes an IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.

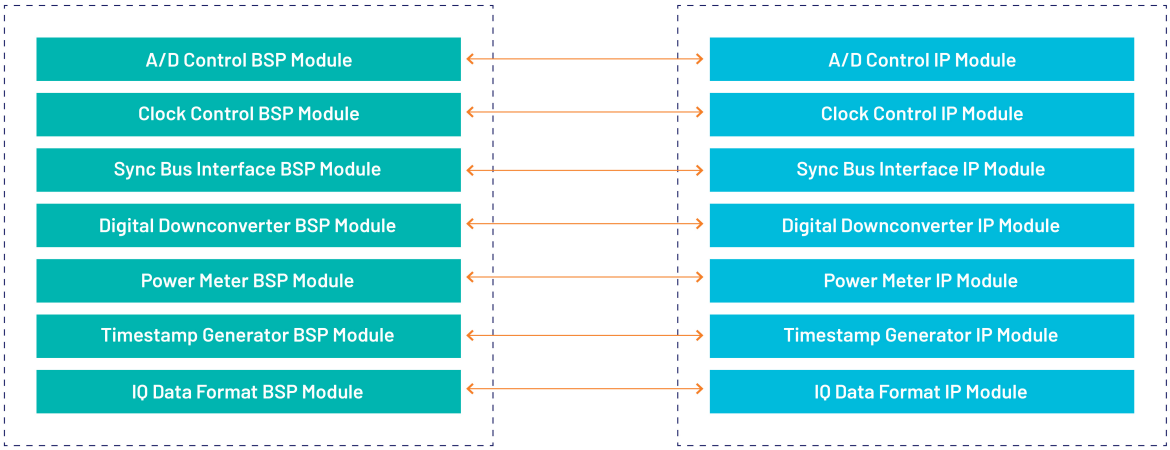
The **Navigator Board Support Package (BSP)** provides software support for Jade boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA. The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.



Navigator IP FPGA Design viewed in IP Integrator

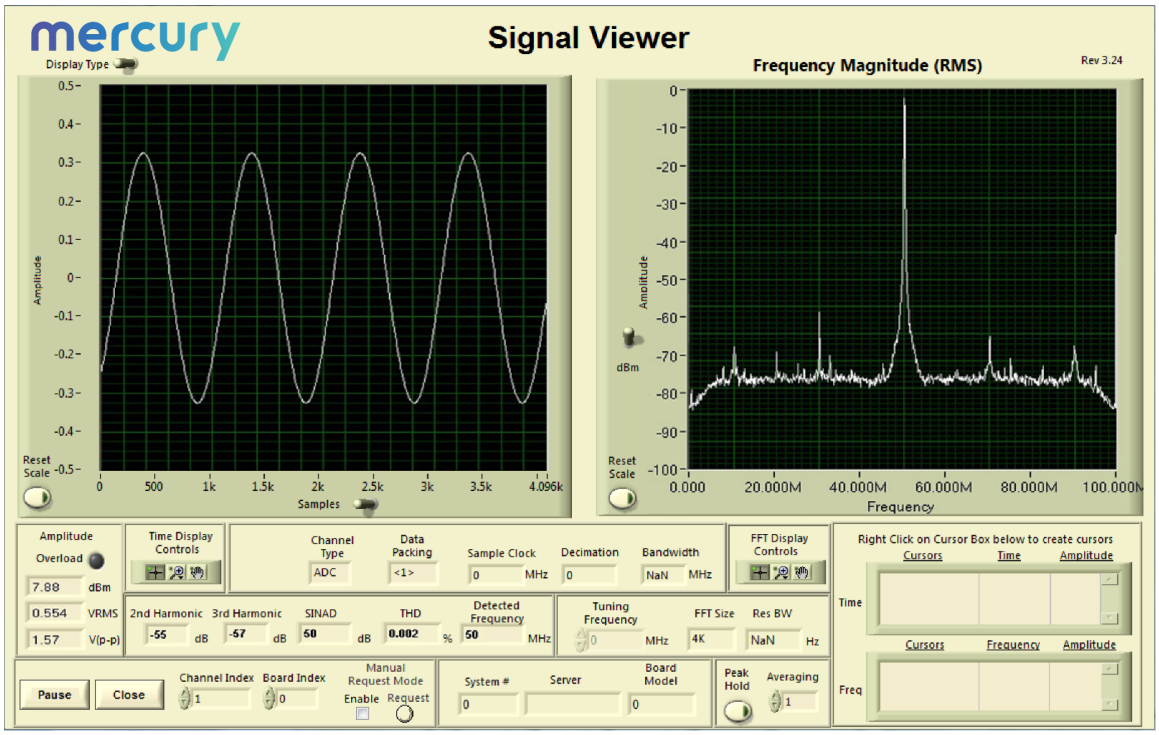
NAVIGATOR BOARD SUPPORT PACKAGE

NAVIGATOR FPGA DESIGN KIT



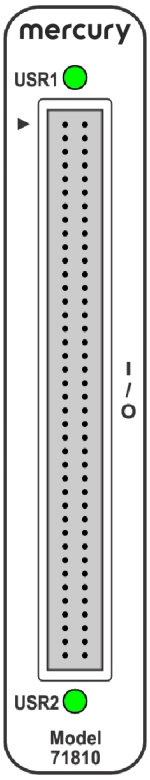
Because all Jade boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the **Signal Viewer**, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Jade board and Navigator BSP and start viewing analog signals immediately.



FRONT PANEL CONNECTIONS

The XMC front panel includes a 80-pin digital input/output connector. The front panel also includes two LED indicators.



- **User LEDs:** The two yellow **USR 1** and **USR 2** LEDs indicate Input/Output operating status.
- **Digital I/O Connector:** The 80-pin connector provides 32 digital input/output Data bits, Clock, Data Valid, and Data suspend signals. Three pairs of spare pins are available for user applications.

SPECIFICATIONS

Front Panel Digital I/O

Connector Type: 80-pin connector, mates to a ribbon cable connector

Signal Quantity: 38 pairs

Signal Type: LVDS

Field Programmable Gate Array

- Standard: Xilinx Kintex UltraScale XCKU035-2
- Option -084: Xilinx Kintex UltraScale XCKU060-2
- Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O

- Option -104: provides 24 pairs of LVDS connections etween the FPGA and the VPX P2 connector for custom I/O (not available with options -111 and -112)
- Option -105: provides an 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols gigabit link to 4X when combined with option -110).
- Option -110: VITA 66.5 interface provides optical 4X duplex lanes
- Option -111: VITA 67.2: digital input/output data bits, clock, data valid, and data suspend
- Option -112: VITA 67.3C: digital input/output data bits, clock, data valid, and data suspend

Memory

Type: DDR4 SDRAM

Size: 5 GB

Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -713: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: 3U VPX board

- Depth: 170.61 mm (6.717 in)
- Height: 100 mm (3.937 in)

Weight: Approximately 14 oz (400 grams)

ORDERING INFORMATION

Model	Description
54810	LVDS Digital I/O 3U VPX with Kintex UltraScale FPGA

Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O
-110	VITA 66.5 interface provides optical 4X duplex lanes
-111	VITA 67.2: digital input/output data bits, clock, data valid, and data suspend
-112	VITA 67.3C: digital input/output data bits, clock, data valid, and data suspend
-702	Air-cooled, Level 2
-763	Conduction-cooled, Level 3

Contact Mercury for compatible option combinations and complete specifications of rugged and conduction-cooled versions. Options may change, so be sure to contact Mercury for the latest information.

DEVELOPMENT SYSTEMS

Mercury offers development systems for Jade products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Jade boards. Please contact Mercury to configure a system that matches your requirements.

FORM FACTORS

Jade products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Jade Model 71810 XMC (LVDS Digital I/O with Kintex UltraScale FPGA) has the following variants:

Model	
54810	3U VPX board (single XMC with optical/backplane RF)
57810	6U VPX board (single XMC)
58810	6U VPX board (dual XMC)
71810	XMC module

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Learn more

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