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Onyx 57760 and 58760

4- or 8-channel 200 MHz, 16-bit A/D
6U VPX board with Virtex-7 FPGA

Complete radar and software radio interface solution

- Radar and software radio receiver
- Communications receiver
- Analog signal interface for data recording
- Wideband data acquisition
- Remote monitoring
- Sensor interfaces

The 57760 and the 58760 consist of one or two 71760 XMC modules mounted on a VPX carrier board. The 57760 is a 6U board with one 71760 module while the 58760 is a 6U board with two XMC modules rather than one.

These models include four or eight A/Ds and four or eight banks of memory.
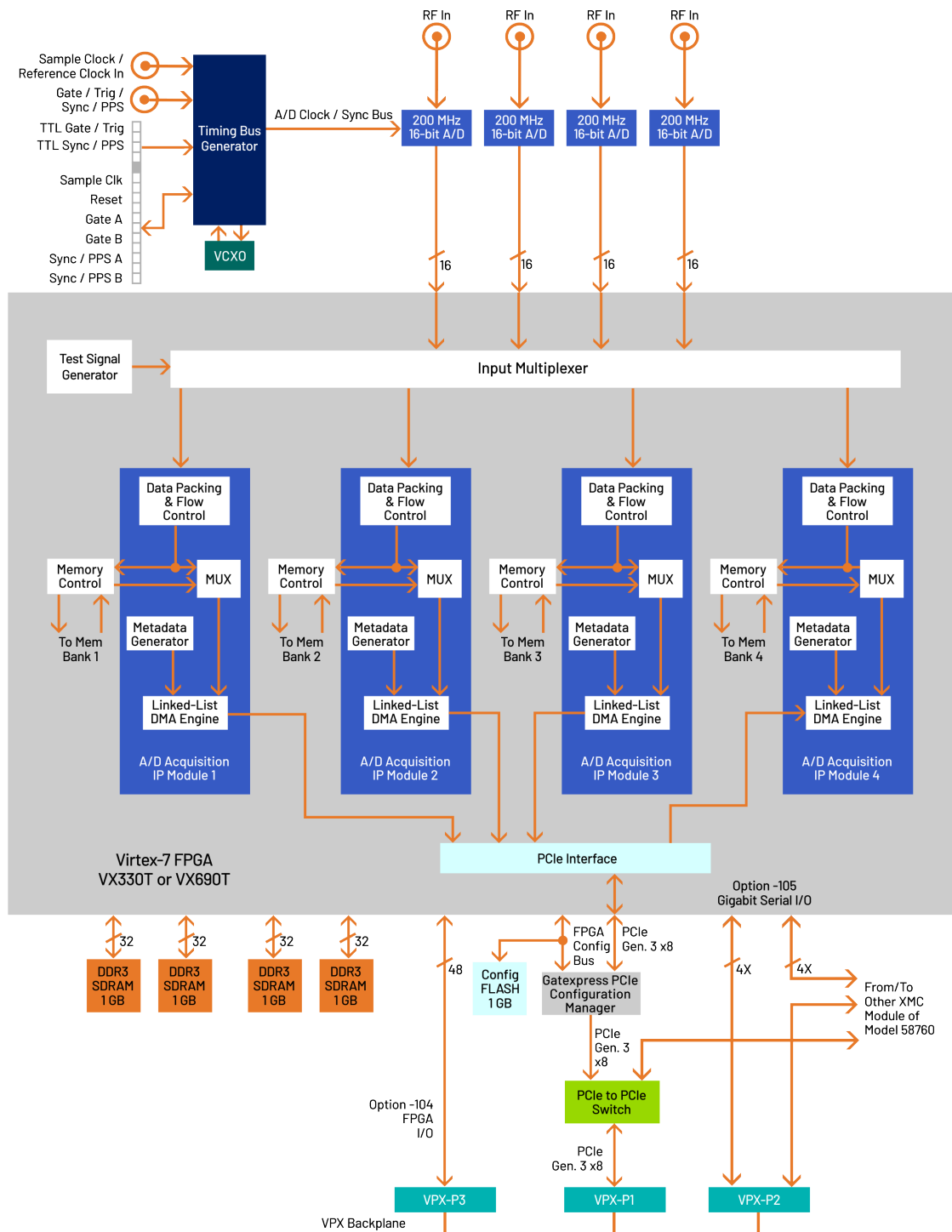
FEATURES

- Supports Xilinx® Virtex®-7 VXT FPGA
- GateXpress® supports dynamic FPGA reconfiguration across PCIe
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight GB of DDR3 SDRAM
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Xilinx® Virtex®-7 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

BLOCK DIAGRAM

Click on a block for more information.

Block diagram 57760 shows half of the 58760. All resources are actually double of what is shown except for the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5.

THE ONYX ARCHITECTURE

Based on the proven design of the Mercury Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as a complete turnkey solution without the need to develop FPGA IP.

EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. The GateFlow FPGA Design Kits include all of the factory-installed modules as document source code. Developers can integrate their own IP with the factory-installed functions or use the GateFlow kit to completely replace the IP with their own.

XILINX VIRTEX-7 FPGA

The Xilinx Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

A/D CONVERTER STAGES

The board's analog interface accepts four or eight full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Xilinx® Virtex®-7 FPGA for signal processing, data capture or for routing to other board resources.

A/D ACQUISITION IP MODULES

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of four A/Ds or the test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

CLOCKING AND SYNCHRONIZATION

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

MEMORY RESOURCES

The Onyx architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI EXPRESS INTERFACE

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

GATEXPRESS FOR FPGA CONFIGURATION

The Onyx architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image:

- The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

- The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

- The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without a host computer reset to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

READYFLOW

Mercury provides ReadyFlow® BSPs (Board Support Packages) for all Cobalt, Onyx, and Flexor products. Available for both Linux and Windows, these packages:

- Provide a path for quick start-up through application completion

- Allow programming at high, intermediate and low levels to meet various needs

- Are illustrated with numerous examples

- Include complete documentation and definitions of all functions

- Include library and example source code.

ReadyFlow BSPs contain C-language examples that can be used to demonstrate the capabilities of Cobalt, Onyx, and Flexor products. These programming examples will help you get an immediate start on writing your own application. They provide sample code that is known to work, giving you a means of verifying that your board set is operational.

COMMAND LINE INTERFACE

The Command Line Interface provides access to pre-compiled executable examples that operate the hardware right out of the box, without the need to write any code. Board-specific hardware operating arguments can be entered in the command line to control parameters: number of channels to enable, sample clock frequency, data transfer size, reference clock frequency, reference clock source, etc.

The Command Line Interface can be used to call an example application from within a larger user application to control the hardware, and parameter arguments are passed to the application for execution. Functions that control data acquisition automatically save captured data to a pre-named host file or are routed to the Signal Analyzer example function for display.

SIGNAL ANALYZER

When used with the Command Line Interface, the Signal Analyzer allows users to immediately start acquiring and displaying A/D data. A full-featured analysis tool, the Signal Analyzer displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD, and SINAD. Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals.
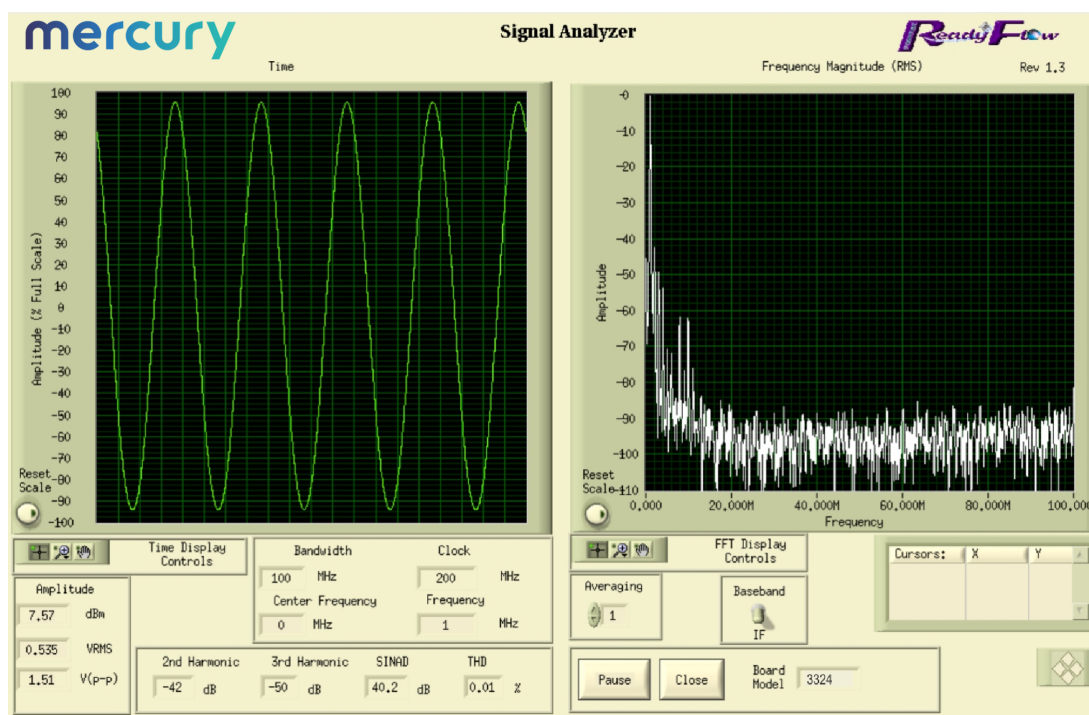
GATEFLOW

The GateFlow® FPGA Design Kit (FDK) allows the user to modify, replace and extend the standard installed functions in the FPGA to incorporate special modes of operation, new control structures, and specialized signal-processing algorithms.

The Cobalt (Virtex-6), Onyx (Virtex-7), and Flexor (Virtex-7) architectures configure the FPGA with standard factory-supplied interfaces including memory controllers, DMA engines, A/D and D/A interfaces, timing and synchronization structures, triggering and gating logic, time stamping and header tagging, data formatting engines, and the PCIe interface. These resources are connected to the User Application Container using well-defined ports that present easy-to-use data and control signals, effectively abstracting the lower-level details of the hardware.

The User Application Container

Shown below is the FPGA block diagram of a typical Cobalt, Onyx or Flexor module. The User Application Container holds a collection of different installed IP modules connected to the various interfaces through the standard ports surrounding the container. The specific IP modules for each product are described in further detail in the datasheet of that product.

The GateFlow FDK provides a complete Xilinx's ISE or Vivado project folder containing all the files necessary for the FPGA developer to recompile the entire project with or without any required changes. VHDL source code for each IP module provides excellent examples of how the IP modules work, how they might be modified, and how they might be replaced with custom IP to implement a specific function.
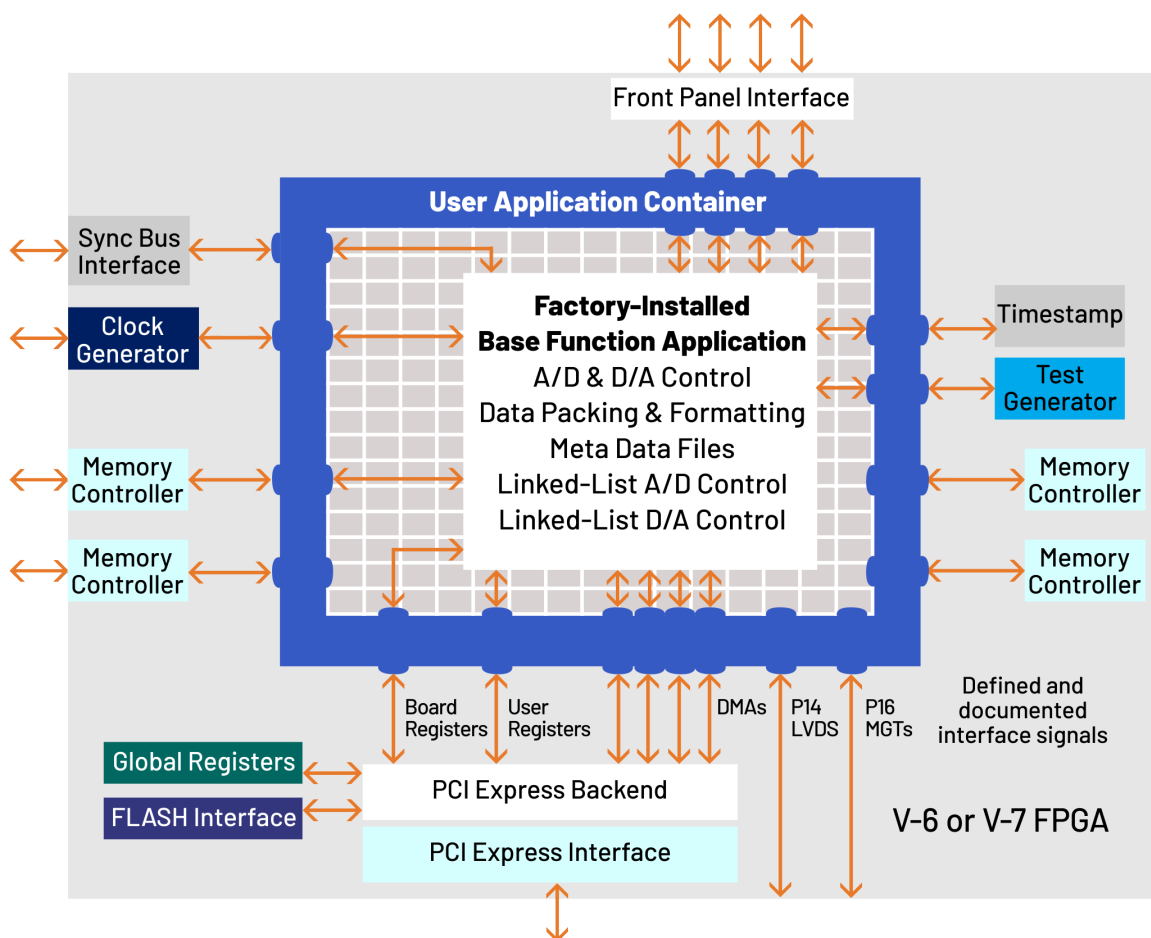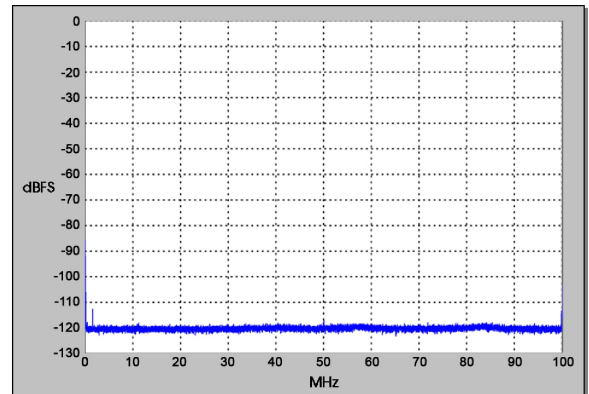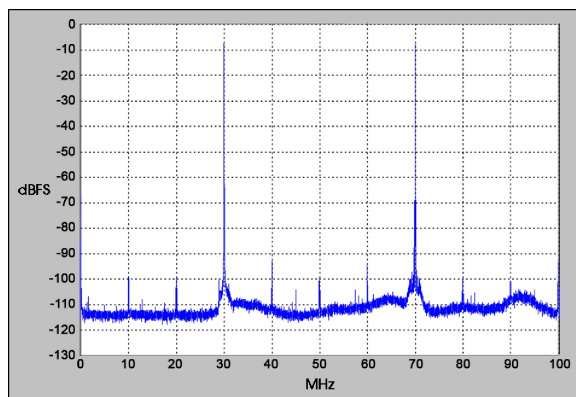
A/D PERFORMANCE

Spurious Free Dynamic Range
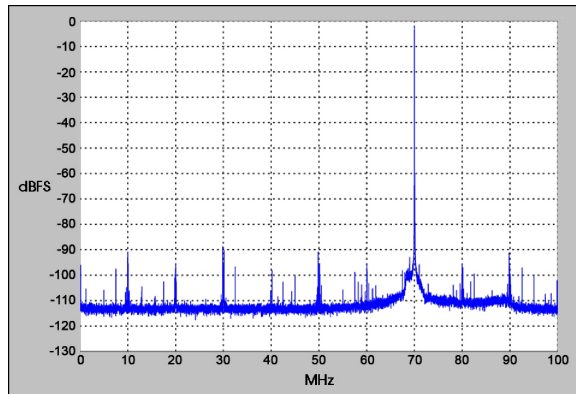
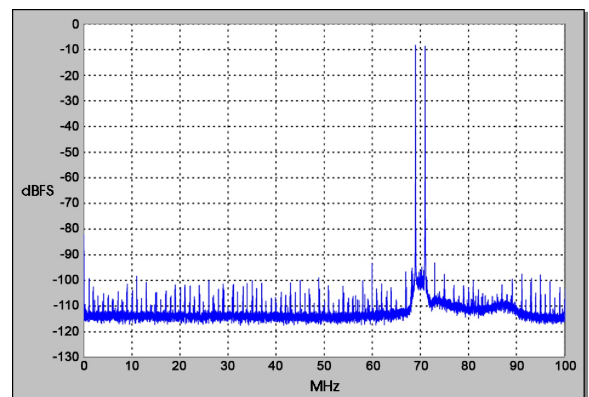f_{in} = 70 MHz, f_s = 200 MHz, Internal Clock

Spurious Pick-up
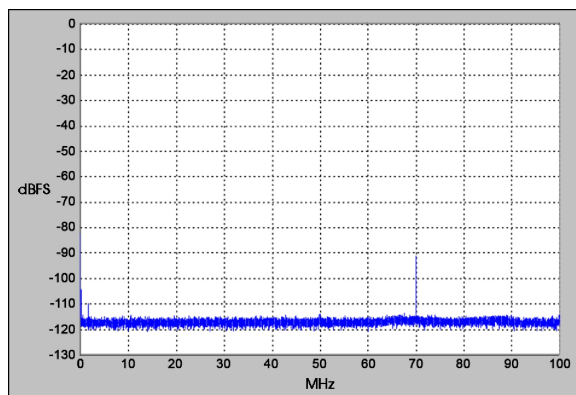

f_s = 200 MHz, Internal Clock

Two-Tone SFDR

f_1 = 30 MHz, f_2 = 70 MHz, f_s = 200 MHz

Two-Tone SFDR

f_1 = 69 MHz, f_2 = 71 MHz, f_s = 200 MHz

Adjacent Channel Crosstalk
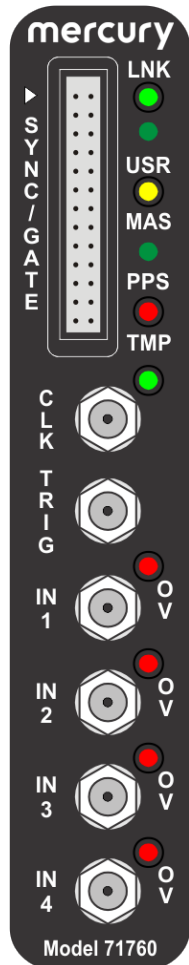

f_{in} Ch2 = 70 MHz, f_s = 200 MHz, Ch 1 shown

Input Frequency Response
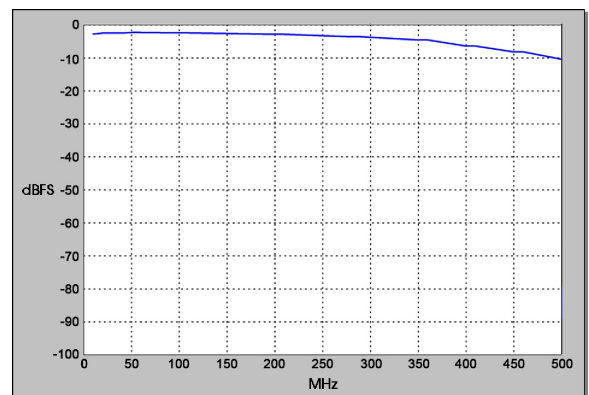
f_s = 200 MHz, Internal Clock

FRONT PANEL CONNECTIONS

The XMC front panel includes six SSMC coaxial connectors and a 26-pin Sync Bus connector for input/output of clock, trigger and analog signals. The front panel also includes ten LEDs.

- **Sync Bus Connector:** The 26-pin Sync Bus front panel connector, labeled **SYNC/GATE**, provides clock, sync, and gate input/output pins for the Sync Bus.

- **Link LED:** The green **LNK** LED blinks when a valid link has been established over the PCIe interface.

- **User LED:** The green **USR** LED is for user applications.

- **MAS LED:** The yellow **MAS** LED illuminates when this model is the Sync Bus Master.

- **PPS LED:** The green **PPS** LED illuminates when a valid PPS signal is detected. The LED will blink at the rate of the PPS signal.

- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the PCB.

- **Clock Input Connector:** One SSMC coaxial connector, labeled **CLK**, for input of an external sample clock.

- **Trigger Input Connector:** The SSMC coaxial connector labeled **TRIG** is for input of an external trigger. The signal must be a LVTTL signal.

- **Analog Input Connectors:** Four SSMC coaxial connectors, labeled **IN 1**, **IN 2**, **IN 3** and **IN 4** are for each ADC input channel.

- **ADC Overload LED:** Four red **OV** (overload) LEDs for each A/D input.

SPECIFICATIONS

57760: 4 A/Ds

58760: 8 A/Ds

Front Panel Analog Signal Inputs (4 or 8)

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters (4 or 8)

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

Sample Clock Sources (1 or 2)

On-board clock synthesizer

Clock Synthesizers (1 or 2)

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference

Timing Bus (1 or 2)

26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Inputs (1 or 2)

Type: Front panel female SSMC connector, LVTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)

- Standard: Xilinx Virtex-7 XC7VX330T-2

- Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O

- Option -104: Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57760; P3 and P5, Model 58760

- Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57760; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58760.

Memory Banks (4 or 8)

Type: DDR3 SDRAM

Size: 1 GB each

Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C

- Storage Temp: -20° to 90° C

- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C

- Storage Temp: -40° to 100° C

- Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C

- Storage Temp: -50° to 100° C

- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions

- Depth: 170.6 mm (6.717 in.)

- Height: 100 mm (3.937 in.)

Weight: VPX Carrier: 110 grams (3.9 oz)

ORDERING INFORMATION

Model	Description
57760	4-Channel 200 MHz 16-bit A/D with Virtex-7 FPGA 6U VPX
58760	8-Channel 200 MHz 16-bit A/D with two Virtex-7 FPGAs - 6U VPX

Options	Description
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O between the FPGA and P3 connector, 57760; P3 and P5 connectors, 58760
-105	Gigabit link between the FPGA and P2 connector, 57760; gigabit links from each FPGA to P2 connector, 78760
-702	Air-cooled, Level 2
-763	Conduction-cooled, Level 3

Contact Mercury for compatible option combinations.

ACCESSORY PRODUCTS

Model	Description
2171	Cable Kit: SSMC to SMA

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FORM FACTORS

Onyx products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Onyx Model 71760 XMC (4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA) has the following variants:

Model	
52760	3U VPX board (single XMC)
57760	6U VPX board (single XMC)
58760	6U VPX board (dual XMC)
71760	XMC module
78760	PCIe board (single XMC)

DEVELOPMENT SYSTEMS

Mercury offers development systems for Onyx products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Onyx boards. Please contact Mercury to configure a system that matches your requirements.

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