Serial RapidIO Sensor IP Core

Industry-Standard, High-Performance, Packet-Based Interconnect Technology

- Provides RapidIO® 2.1 5-GBaud channelized streaming endpoint
- Industry-standard OCP® user interface
- Ideal for guaranteed delivery chip-to-chip communications
- Small footprint
- Targets both Xilinx® v5, v6 and Altera® Stratix® IV

The Serial RapidIO® Sensor IP Core from Mercury Computer Systems is designed for the growing RapidIO market. The core is a high-performance solution that is independent of physical layer designs, implementation tools, and target technology. It is capable of addressing a variety of solutions, including point-to-point and switched applications.

The RapidIO Interconnect Architecture is an industry-standard, high-performance, packet-based interconnect technology that provides a high-speed interconnect between NPUs, CPUs, and DSPs. It addresses the need for a standards-based, high-speed, reliable interconnect and is targeted at the networking, embedded, and storage markets. Serial RapidIO allows chip-to-chip, board-to-board, and system-to-system communications scaling to 16 Gbps and beyond.

As the pioneer of heterogeneous switch fabric-based computing and co-developer of the RapidIO technology, Mercury is uniquely equipped with the system and application expertise, and the support and consulting resources focused on RapidIO. No other supplier of RapidIO IP can provide a proven product with such high performance and flexibility, as well as the long-term system-level testing that Mercury has already conducted on its IP cores.

High-Performance, High-Function Core

Mercury's Serial RapidIO Sensor IP Core provides a focused solution for push-only streaming applications. It is architected to provide an end-to-end solution for designers who need to implement a serial RapidIO-based endpoint solution in either ASICs or FPGAs. The core provides a serial RapidIO interface on the fabric side and an OCP® standard streaming interface on the user side. The database comes with an OVM-based test bench for easy integration into your verification environment.

RapidIO is ideal for use in a variety of communication applications including base stations, edge routers, chip-to-chip, enterprise switches, and other devices requiring a high-speed interface. It can also be incorporated into high-end embedded compute applications.
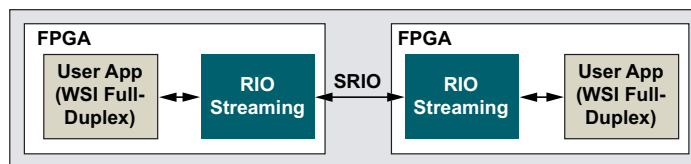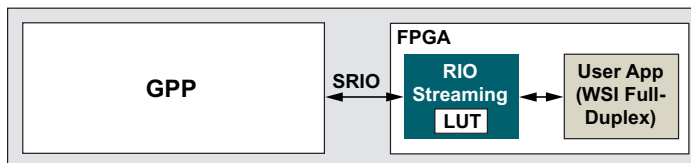

Figure 1. Chip-to-Chip Interconnection
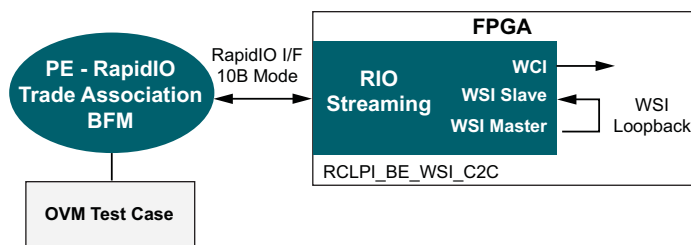

Figure 2. Chip-to-GPP Application

Figure 3. Test Bench Configuration

Interprocessor Communication

Sensor IP Core-enabled FPGAs can communicate directly to your general-purpose processor (GPP). For multicomputer applications that use the Interprocessor Communication System (ICS) library, it reads from or writes to ICS shared memory buffers (SMBs). It also can send signals to the GPP to generate MC semaphores, so controlling applications have the option to poll for completion or block on a semaphore to yield the CPU. Data transfers and synchronization are very similar to inter-GPP communication. For single-processor applications, Mercury's Performance Porting Kit (PPK) can be used to communicate with the Sensor IP Core-enabled FPGA.

Specifications

Language	Verilog® HDL
Synthesis	Synopsys®/Synplicity®/Altera®
IC technology	0.13 micron or better ASIC; Stratix® IV or Xilinx® v5, v6 FPGA
Simulation	Mentor QuestaSim/OVM

Support for:

- Serial specification 1.2 GHz, 2.5 GHz, 3.125 GHz, 5 GHz
- 4x serial interfaces
- 34-bit addressing
- NWRITE, MAILBOX, and CFG operations
- All legal data payload sizes up to 256 bytes

Availability and Serviceability

Available now

Product Options

Single or multi-use license

Soft IP core   RTL source code, synthesis scripts, and so on

Comprehensive documentation package

Compliance

RapidIO Specification, Rev. 2.1 (5 GHz short control symbol)

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