

# Models 5790 and 5890

## Multifrequency clock synthesizers – 6U VPX boards

### Simultaneous synthesis of up to five or ten different clocks

- Eight or 16 SMC clock outputs
- Typical phase noise:  $-105$  dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz



**The 5790 and 5890 generate up to eight or 16 synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems.** The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

### CLOCK SYNTHESIZER CIRCUITS

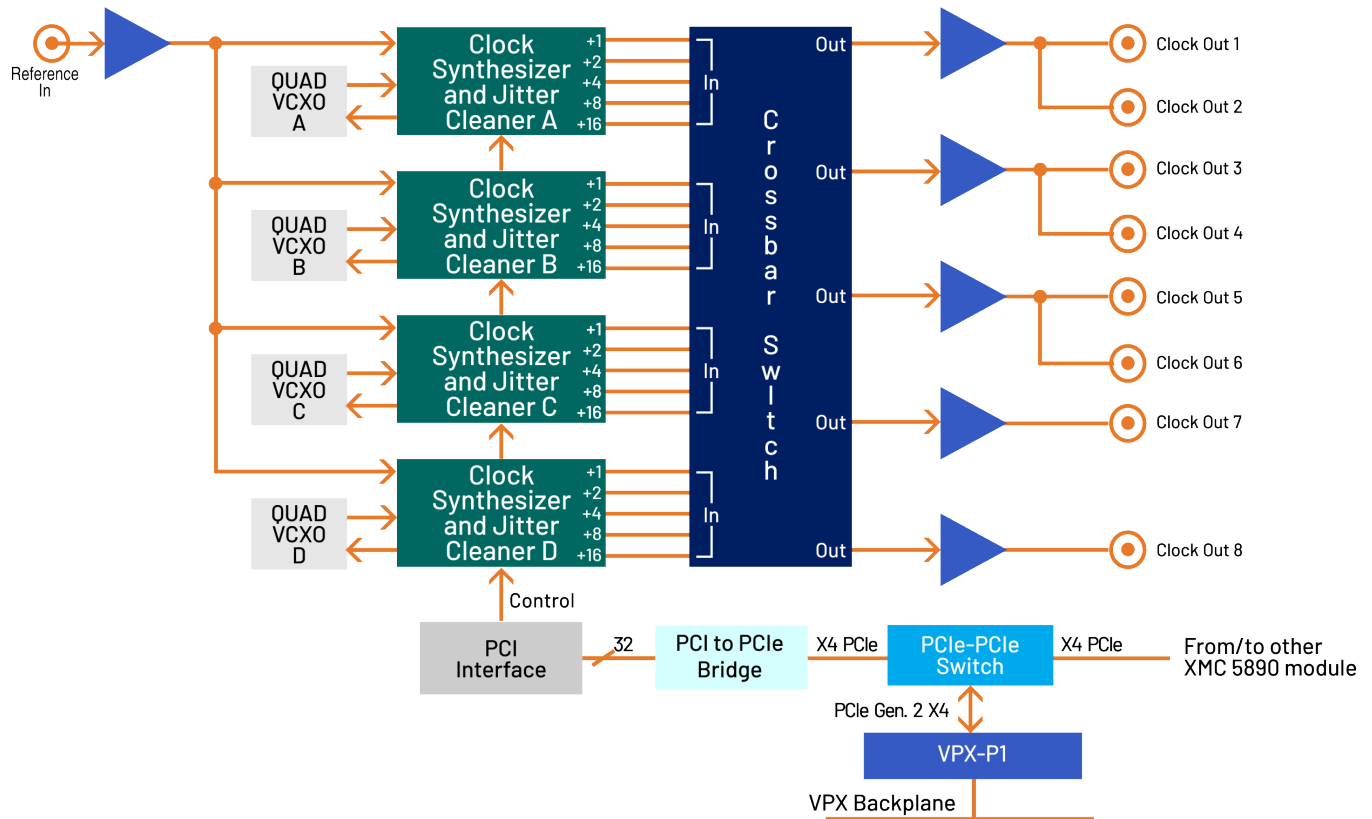
These models use four or eight Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO (Voltage Controlled Crystal Oscillator) to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to generate one of four frequencies between 50 and 700 MHz.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The CDC7005s can output up to five frequencies each and be programmed to route any of these five or 10 frequencies to the board's output drivers and includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight or 16 front panel SMC connectors supply synthesized clock outputs driven from the clock output drivers. This supports a single identical clock to all outputs or up to five or ten different clocks to various outputs.

With four or eight independent quad VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than ten different clock outputs are required simultaneously, multiple 5890's can be used and phase-locked with a 5 to 100 MHz system reference.

BLOCK DIAGRAM



Model 5890 doubles all resources except the PCIe-to-PCIe switch.

## SOFTWARE

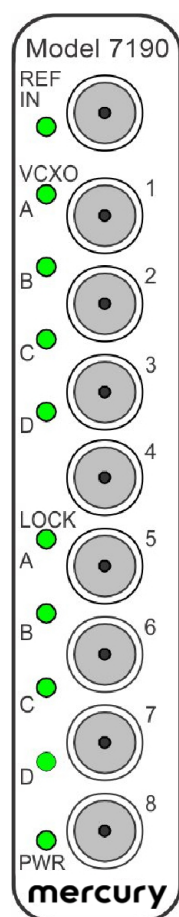
If you are using a Cobalt or Onyx board in conjunction with 5790 or 5890, software support is provided by Mercury's ReadyFlow® Board Support Packages (BSP). There is a separate ReadyFlow BSP to support the Cobalt or Onyx board.

Support for the 5790 or 5890 is provided by the ReadyFlow Board Support Package (BSP) for Model 7190, which has Windows and Linux versions:

- Model 4995A Option 190 Windows ReadyFlow BSP for Model 7190
- Model 4994A Option 190 Linux ReadyFlow BSP for Model 7190

## FRONT PANEL CONNECTIONS

The front panel includes one SMC connector for a reference signal input, eight SMC connectors for clock outputs and ten LED indicators. Please use the cables described in Ordering Information.



- **Reference Input Connector:** One SMC receptacle, labeled **REF IN**, for input of an external reference clock.
- **Clock Output Connectors:** Eight SMC connectors for the Clock signal inputs labeled **CLK 1 - 8**. The clock output signal is within the range of +4 dBm. This output is driven into 50  $\Omega$  output impedance.
- **REF IN LED:** A green LED labeled **REF IN** illuminates when a reference clock input is applied to the board.
- **VCXO LEDs:** Four green LEDs labeled VCXO A-D illuminate when the associated VCXO input is valid (A is for VCXO 1, B for VCXO 2, C for VCXO 3, D for VCXO 4).
- **Lock LEDs:** Four green LEDs labeled LOCK A-D illuminate when the associated VCXO PLL is locked (A is for VCXO 1, B for VCXO 2, C for VCXO 3, D for VCXO 4).
- **Power LED:** A green LED labeled **PWR** illuminates when a +5VDC is applied to the board.

## SPECIFICATIONS

## Front Panel Reference Input

Connector Type: SMC  
 Input Impedance: 50 ohms  
 Reference Frequency: 5 to 100 MHz  
 Input Level: -6 dBm to +10 dBm

## PLL Clock Synthesizers &amp; Jitter Cleaners

Quantity: Model 5790: 4; Model 5890: 8  
 Type: Texas Instruments CDC7005  
 Frequency Dividers: 1, 2, 4, 8 and 16

## Quad VCXOs (Quantity: 4 or 8)

Frequencies per VCXO: 4\*, software-programmable  
 Frequency Range: 50 to 700 MHz  
 Unlocked Accuracy: +20 ppm

## Front Panel Clock Outputs (Quantity: 8 or 16)

Connector Type: SMC  
 Output Impedance: 50 ohms  
 Output Level: +3 dBm @ 700 MHz  
 Typ. Phase Noise: -105 dBc/Hz @ 1 kHz (dependent on reference source stability)

## PCI Express Interface

PCI Express Bus: Gen. 1, 2 : x4, control and status

## Environmental

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.

## Size

233 mm x 160 mm (9.173 in. x 6.299 in.)

## ORDERING INFORMATION

Model	Description
5790*	Multifrequency Clock Synthesizer - 6U VPX Single Density
5890*	Multifrequency Clock Synthesizer - 6U VPX Double Density

\*Specify frequencies of factory-installed quad VCXOs between 50 and 700 MHz. Contact [techsales@mrchy.com](mailto:techsales@mrchy.com) to order specific frequencies.

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