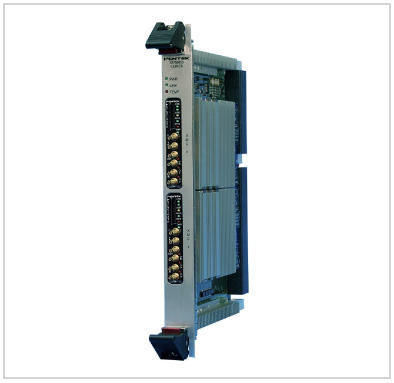
Jade 57851/58851

2- or 4-channel 500 MHz A/D, DDC, DUC
2- or 4-channel 800 MHz D/A
6U VPX boards with Kintex UltraScale FPGA

Complete radar and software radio interface solution

- Radar and communication receiver and transmitter
- Electronic Warfare transponder
- Waveform signal generator
- Wideband data acquisition
- Remote monitoring
- Sensor interfaces



These Jade® models consist of one or two 71851 XMC modules mounted on a VPX carrier board. The 57851 is a 6U board with one 71851 module while the 58851 is a 6U board with two XMC modules rather than one. They include two or four A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, two or four DDCs, one or two DUC, and two or four D/As.

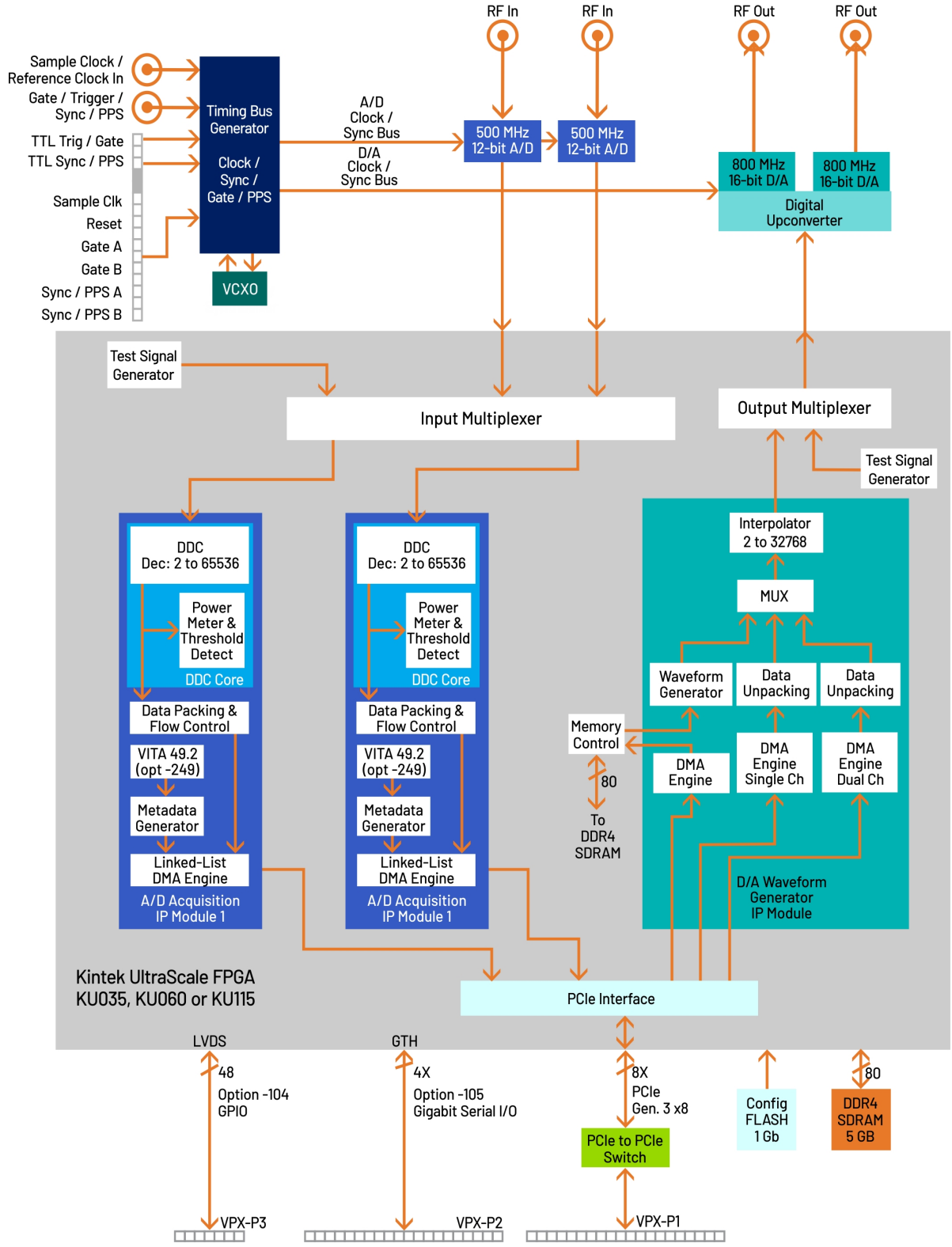
In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

FEATURES

- Xilinx® Kintex® UltraScale™ FPGA
- Two or four 500 MHz 12-bit A/Ds
- Two or four multiband DDCs (digital downconverters)
- One or two DUC (digital upconverters)
- Two or four 800 MHz 16-bit D/As
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express interface (Gen. 1, 2 & 3) up to x8
- Optional LVDS port and gigabit serial connections for custom FPGA I/O
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Optional 400 MHz 14-bit A/Ds
- Ruggedized and conduction-cooled versions
- Navigator Design Suite for software and custom IP development

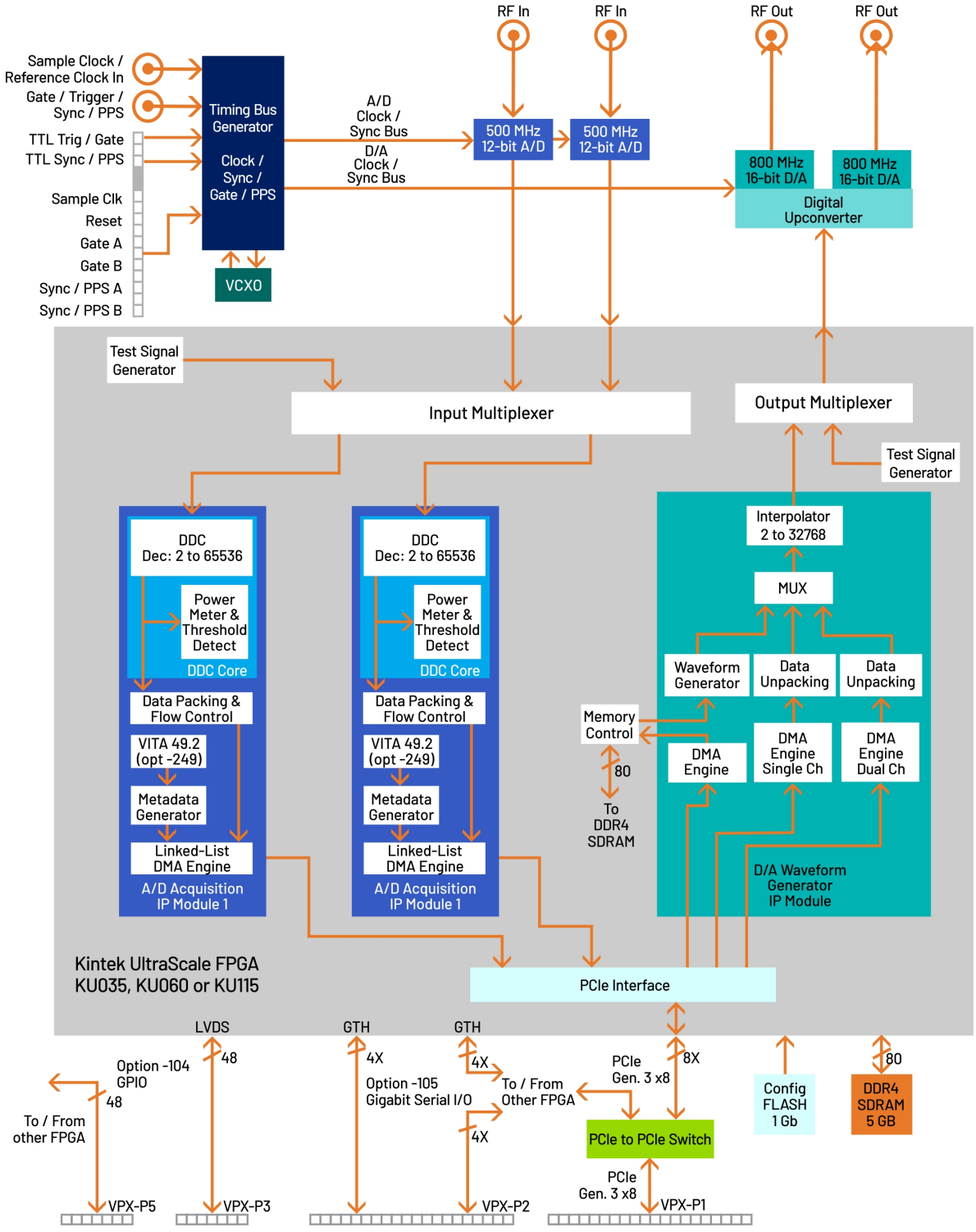
57851 BLOCK DIAGRAM

Click on a block for more information.



58851 BLOCK DIAGRAM

Block diagram shows half of the 58851. All resources are actually double of what is shown except for the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5.



THE JADE ARCHITECTURE

Evolved from the proven designs of Mercury's Cobalt® and Onyx® families, Jade® raises the processing performance while lowering the overall power requirements by building on the Xilinx family of Kintex UltraScale FPGAs. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions as well as providing an ideal platform for user-created intellectual property (IP).

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include two or four A/D acquisition and two or four waveform playback IP modules for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: two or four powerful, programmable DDC IP cores; IP modules for DDR4 SDRAM memory; controllers for data clocking and synchronization functions; test signal generators; programmable interpolators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions thereby saving the time of IP development.

XILINX KINTEX ULTRASCALE FPGAS

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs: KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

A/D CONVERTER STAGE

The board's analog interface accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

Optionally, the Texas Instruments ADS5474 400 MHz, 14-bit A/D may be factory-installed instead of the ADS5463.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other module resources.

A/D ACQUISITION IP MODULES

These models feature two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP CORES

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_S, where f_S is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*fs/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of fs/N.

D/A WAVEFORM PLAYBACK IP MODULES

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. They allow users to easily play back to the dual or quad D/As waveforms stored in either on-board memory or off-board host memory.

DIGITAL UPCONVERTER AND D/A STAGE

A Texas Instruments DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

CLOCKING AND SYNCHRONIZATION

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 57851s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

MEMORY RESOURCES

The architecture of these models supports 5 or 10 GB of DDR4 SDRAM memory. User-installed IP along with the Mercury-supplied DDR4 controller cores within the FPGA can take advantage of the memory for custom applications.

PCI EXPRESS INTERFACE

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

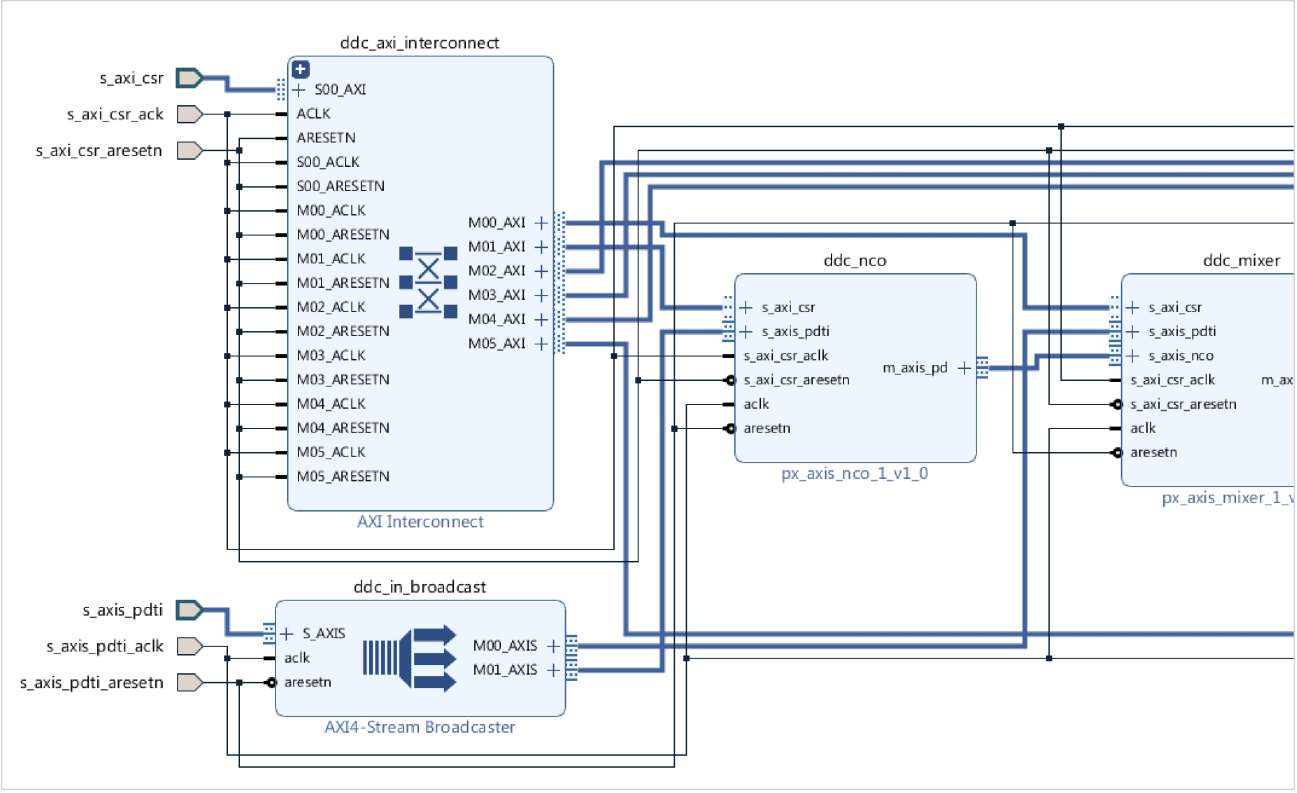
NAVIGATOR DESIGN SUITE

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into the factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

The **Navigator FPGA Design Kit (FDK)** for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Jade product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Jade design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations.

Navigator FDK includes an IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.

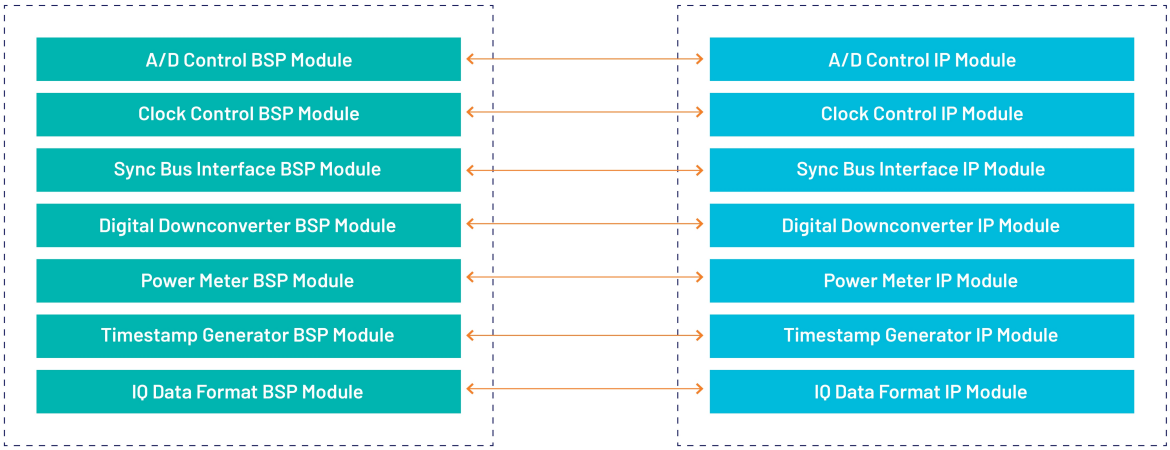
The **Navigator Board Support Package (BSP)** provides software support for Jade boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA. The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.



Navigator IP FPGA Design viewed in IP Integrator

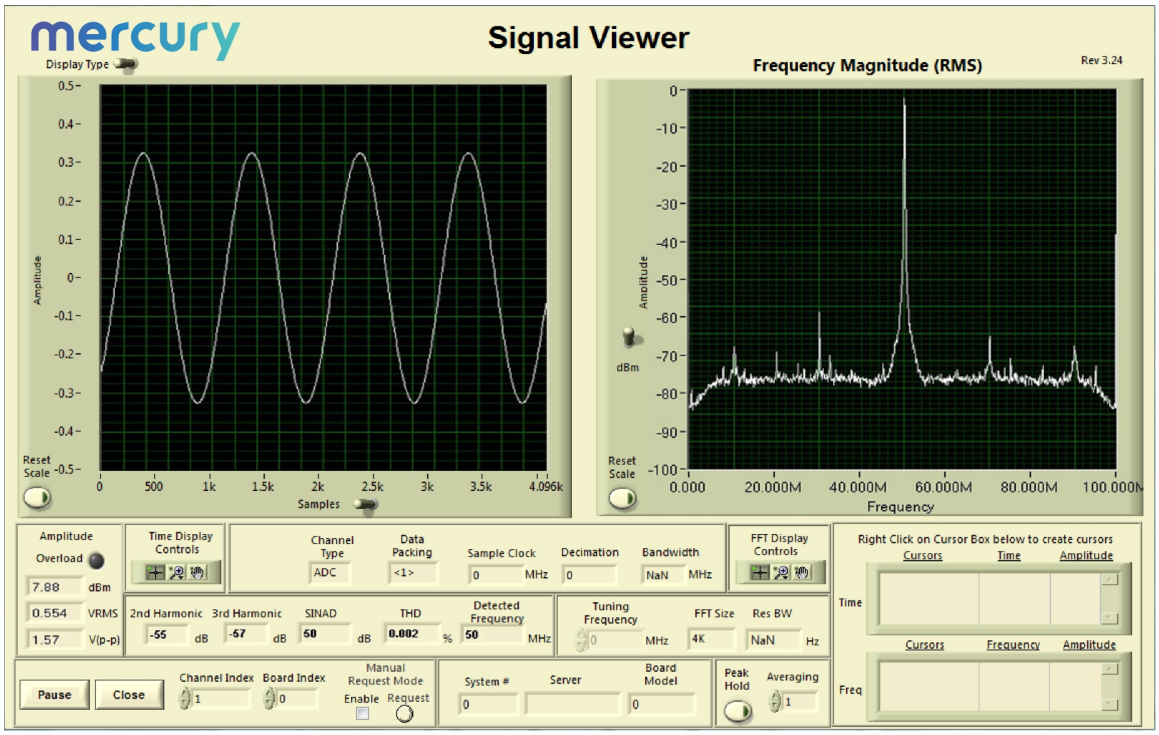
NAVIGATOR BOARD SUPPORT PACKAGE

NAVIGATOR FPGA DESIGN KIT



Because all Jade boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the **Signal Viewer**, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Jade board and Navigator BSP and start viewing analog signals immediately.



FRONT PANEL CONNECTIONS

The front panel includes six SSMC coaxial connectors for clock, PPS, and analog/digital input signals, and a 26-pin Sync Bus input/output connector. The front panel also includes nine LEDs.

- **Sync Bus Connector:** The 26-pin µSync connector, labeled **SYNC/GATE**, provides clock, sync, and gate input/output pins for the Low-Voltage Positive Emitter-Coupled Logic (LVPECL) Sync Bus.
- **Link LED:** The green **LNK** LED indicates the link speed when a valid link has been established over the PCIe interface, as follows: Gen 1 - LED blinks slowly (less than once per second); Gen 2 - LED blinks about once per second; Gen 3 - LED will be constantly on.
- **User LED:** The green **USR** LED is for user applications.
- **Master LED:** The yellow MAS LED illuminates when the 58851 is the Sync Bus Master. When only a single 58851 is used, it must be a Master.
- **PPS LED:** The green **PPS** LED illuminates when a valid PPS signal is detected. The LED will blink at the rate of the PPS signal.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature voltage sensors on the PCB.
- **Clock LED:** The green **CLK** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.
- **Clock Input Connector:** One SSMC coaxial connector, labeled **CLK**, for input of an external sample clock.
- **Trigger Input Connector:** One SSMC coaxial connector, labeled **TRIG**, for input of an external trigger.
- **Analog Output Connectors:** Two SSMC coaxial connectors, labeled **OUT 1** and **OUT 2**: one for each DAC5688 output channel.
- **Analog Input Connectors:** Two SSMC coaxial connectors, labeled **IN 1** and **IN 2**: one for each ADC input channel.
- **DAC Underrun LED:** One red underrun **UR** LED for the D/A output. This LED illuminates when the DAC5688 FIFO is out of data.
- **ADC Overload LEDs:** There are two red **OV** (overload) LEDs: one for each A/D input. Each LED indicates either an analog input overload in the associated ADS5463 (or ADS5474), or an ADC FIFO overrun.

SPECIFICATIONS

57851 Two A/D; 58851 Four A/Ds

Front Panel Analog Signal Inputs (2 or 4)

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converters (standard) (2 or 4)

Type: Texas Instruments ADS5463

Sampling Rate: 20 MHz to 500 MHz

Resolution: 12 bits

A/D Converters (option -014) (2 or 4)

Type: Texas Instruments ADS5474

Sampling Rate: 20 MHz to 400 MHz

Resolution: 14 bits

Digital Downconverters (2 or 4)

Quantity: Two channels

Decimation Range: 2x to 65,536x in three stages of 2x to 32x and one fixed stage of 2

LO Tuning Freq. Resolution: 32 bits, 0 to f_s

LO SFDR: >120 dB

Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: 16-bit coefficients, 24-bit output, with user-programmable coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters (2 or 4)

Type: Texas Instruments DAC5688

Input Data Rate: 250 MHz max.

Output IF: DC to 400 MHz max.

Output Signal: 2-channel real or 1-channel with frequency translation

Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation

Resolution: 16 bits

Digital Interpolator Core (1 or 2)

Interpolation Range: 2x to 32,768x in one stage of 2x to 256x and one stage of 2x to 128x

Total Interpolation Range (D/A and interpolator core combined): 2x to 262,144x

Front Panel Analog Signal Outputs (2 or 4)

Output: Transformer-coupled, front panel female SSMC connectors

Transformer: Coil Craft WBC4-6TLB

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: (1 or 2)

On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer (1 or 2)

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock (1 or 2)

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2)

26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array (1 or 2)

Standard: Xilinx Kintex UltraScale XCKU035-2

Option -084: Xilinx Kintex UltraScale XCKU060-2

Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O

Option -104: provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, 57851; P3 and P5 connectors, 58851.

Option -105: provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols.

Memory (1 or 2)

Type: DDR4 SDRAM

Size: 5 GB

Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: 6U board

- Depth: 233.35 mm (9.187 in)
- Height: 170.60 mm (6.717 in)

Weight: Approximately 14 oz (400 grams)

ORDERING INFORMATION

Model	Description
57851	2-channel 500 MHz A/D with DDCs, DUC with 2-channel 800 MHz D/A, and Kintex UltraScale FPGA - 6U VPX
58851	4-channel 500 MHz A/D with DDCs, DUC with 4-channel 800 MHz D/A, and Kintex UltraScale FPGA - 6U VPX

Options:	
-014	400 MHz, 14-bit A/Ds
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-105	Gigabit serial FPGA I/O
-702	Air-cooled, Level 2
-763	Conduction-cooled, Level 3

Contact Mercury for compatible option combinations and complete specifications of rugged and conduction-cooled versions. Options may change, so be sure to contact Mercury for the latest information.

ACCESSORY PRODUCTS

Model	Description
2171	Cable Kit: SSMC to SMA

FORM FACTORS

Jade products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Jade Model 71851 XMC (2-Channel 500 MHz A/D with DDC and 2-Channel 800 MHz D/A with DUC, Kintex UltraScale FPGA) has the following variants:

Model	
52851	3U VPX board (single XMC)
54851	3U VPX board (single XMC with optical/backplane RF)
57851	6U VPX board (single XMC)
58851	6U VPX board (dual XMC)
71851	XMC module
78851	PCIe board (single XMC)

DEVELOPMENT SYSTEMS

Mercury offers development systems for Jade products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Jade boards. Please contact Mercury to configure a system that matches your requirements.

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