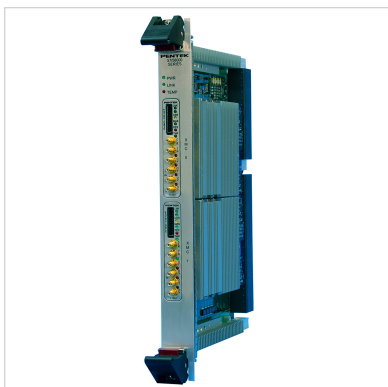


# Cobalt 57660/58660

4- or 8-channel 200 MHz, 16-bit A/D  
6U VPX boards with Virtex-6 FPGA

## Complete radar and software radio interface solution

- Radar and software radio receiver
- Communications receiver
- Analog signal interface for data recording
- Wideband data acquisition
- Remote monitoring
- Sensor interfaces



**Models 57660 and 58660 consist of one or two 71660 XMC modules mounted on a VPX carrier board.** The 57660 is a 6U board with one 71660 module while the 58660 is a 6U board with two XMC modules rather than one.

These models include four or eight A/Ds and four or eight banks of memory.

### FEATURES

- Supports Xilinx® Virtex®-6 LXT and SXT FPGA
- Four or eight 200 MHz 16-bit A/Ds
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 or 64 MB of QDRII+ SRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to [an external system reference](#)
- LVPECL clock/sync bus for [multiboard synchronization](#)
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the FPGA for custom I/O

### THE COBALT ARCHITECTURE

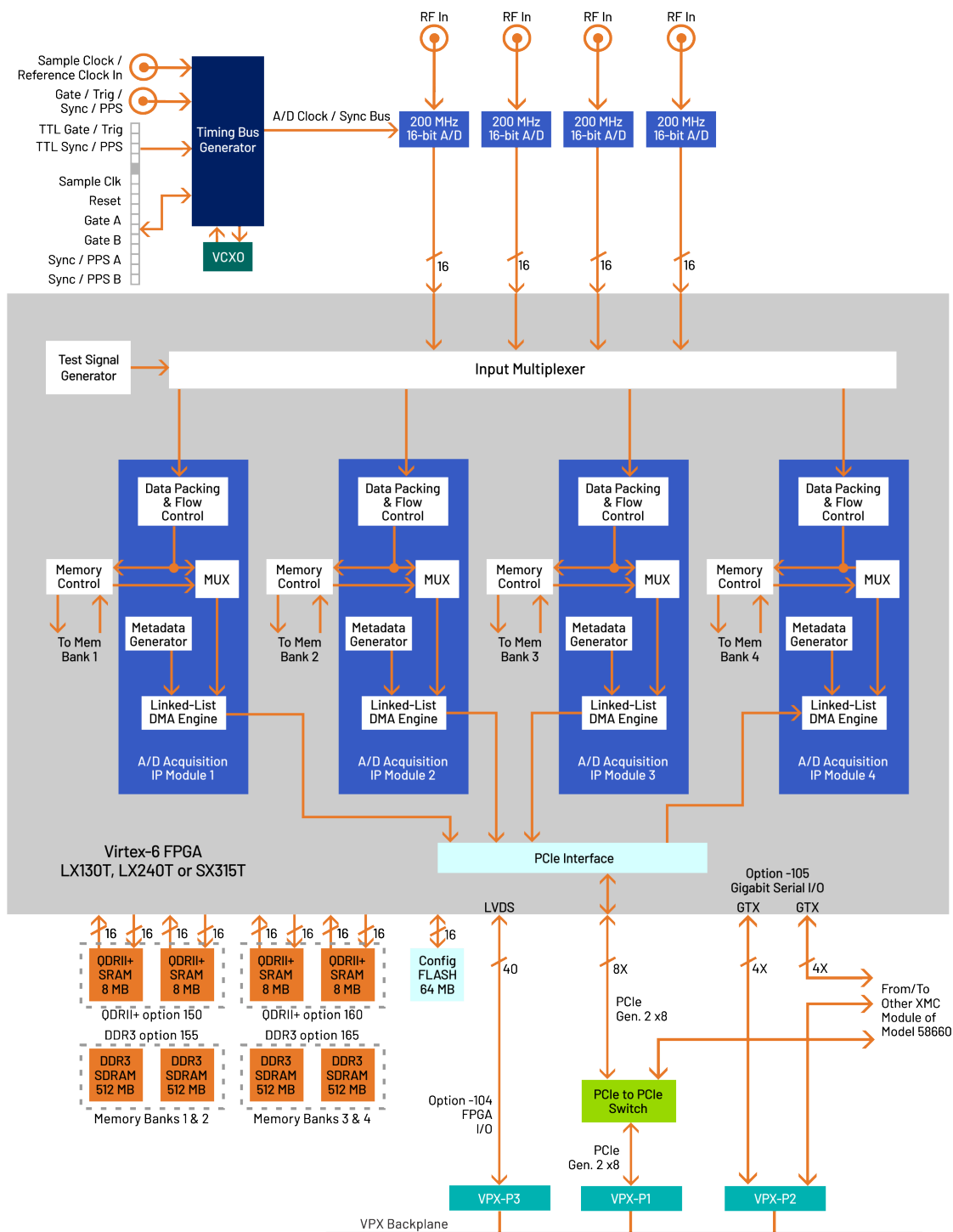
Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop FPGA IP.

## BLOCK DIAGRAM

Click on a block for more information.

Block diagram 57660 shows half of the 58660. All resources are actually double of what is shown except for the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5.



## EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. The GateFlow FPGA Design Kits include all of the factory-installed modules as document source code. Developers can integrate their own IP with the factory-installed functions or use the GateFlow kit to completely replace the IP with their own.

## XILINX VIRTEX-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

## A/D CONVERTER STAGE

The board's analog interface accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

## A/D ACQUISITION MODULES

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These

actions simplify the host processor's job of identifying and executing on the data.

## CLOCKING AND SYNCHRONIZATION

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

## MEMORY RESOURCES

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

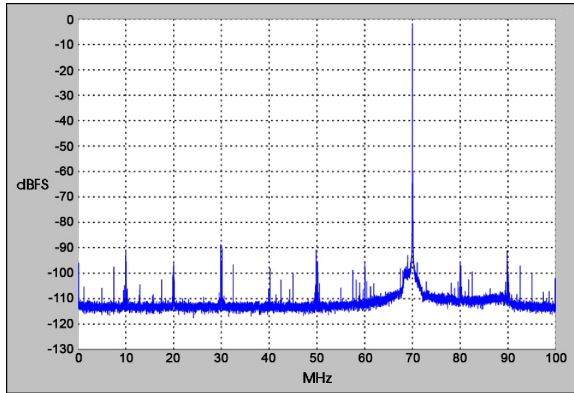
In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

## PCI EXPRESS INTERFACE

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

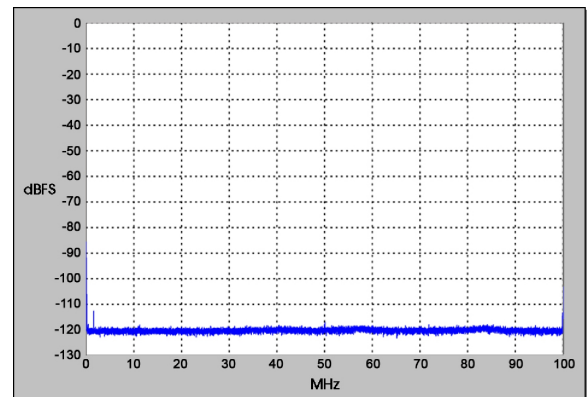
## A/D PERFORMANCE

**Spurious Free Dynamic Range**



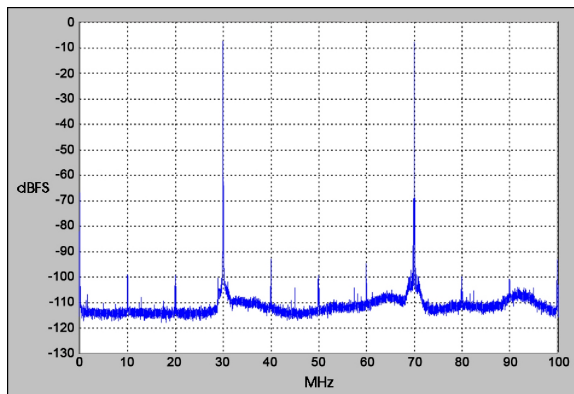
$f_{in} = 70 \text{ MHz}$ ,  $f_s = 200 \text{ MHz}$ , Internal Clock

**Spurious Pick-up**



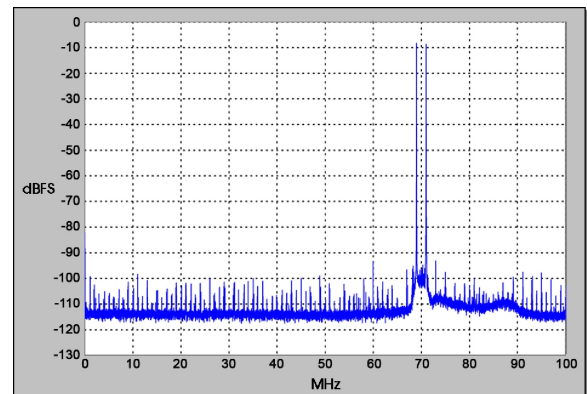
$f_s = 200 \text{ MHz}$ , Internal Clock

**Two-Tone SFDR**



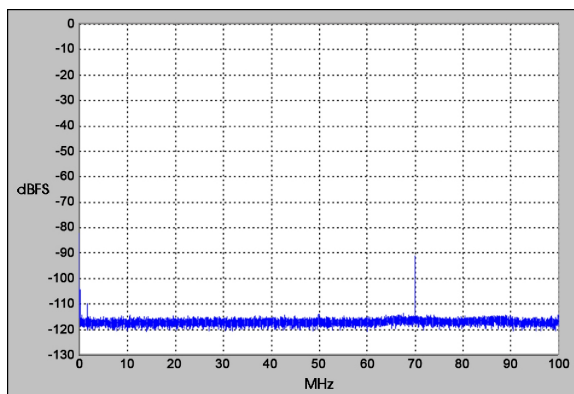
$f_1 = 30 \text{ MHz}$ ,  $f_2 = 70 \text{ MHz}$ ,  $f_s = 200 \text{ MHz}$

**Two-Tone SFDR**



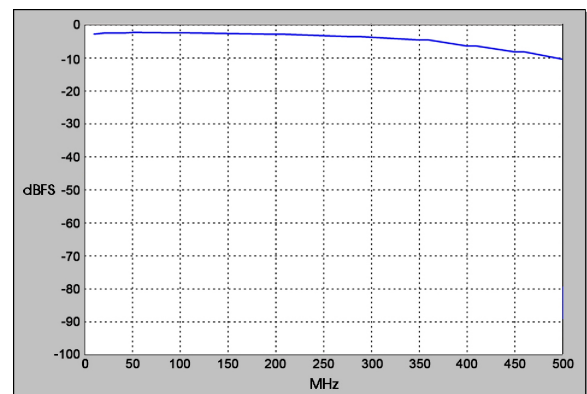
$f_1 = 69 \text{ MHz}$ ,  $f_2 = 71 \text{ MHz}$ ,  $f_s = 200 \text{ MHz}$

**Adjacent Channel Crosstalk**



$f_{in} \text{ Ch2} = 70 \text{ MHz}$ ,  $f_s = 200 \text{ MHz}$ , Ch 1 shown

**Input Frequency Response**



$f_s = 200 \text{ MHz}$ , Internal Clock

## READYFLOW

Mercury provides ReadyFlow<sup>®</sup> BSPs (Board Support Packages) for all Cobalt, Onyx, and Flexor products. Available for both Linux and Windows, these packages:

- Provide a path for quick start-up through application completion
- Allow programming at high, intermediate and low levels to meet various needs
- Are illustrated with numerous examples
- Include complete documentation and definitions of all functions
- Include library and example source code.

ReadyFlow BSPs contain C-language examples that can be used to demonstrate the capabilities of Cobalt, Onyx, and Flexor products. These programming examples will help you get an immediate start on writing your own application. They provide sample code that is known to work, giving you a means of verifying that your board set is operational.

## COMMAND LINE INTERFACE

The Command Line Interface provides access to pre-compiled executable examples that operate the hardware right out of the box, without the need to write any code. Board-specific hardware

operating arguments can be entered in the command line to control parameters: number of channels to enable, sample clock frequency, data transfer size, reference clock frequency, reference clock source, etc.

The Command Line Interface can be used to call an example application from within a larger user application to control the hardware, and parameter arguments are passed to the application for execution. Functions that control data acquisition automatically save captured data to a pre-named host file or are routed to the Signal Analyzer example function for display.

## SIGNAL ANALYZER

When used with the Command Line Interface, the Signal Analyzer allows users to immediately start acquiring and displaying A/D data. A full-featured analysis tool, the Signal Analyzer displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD, and SINAD. Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals.





## GATEFLOW

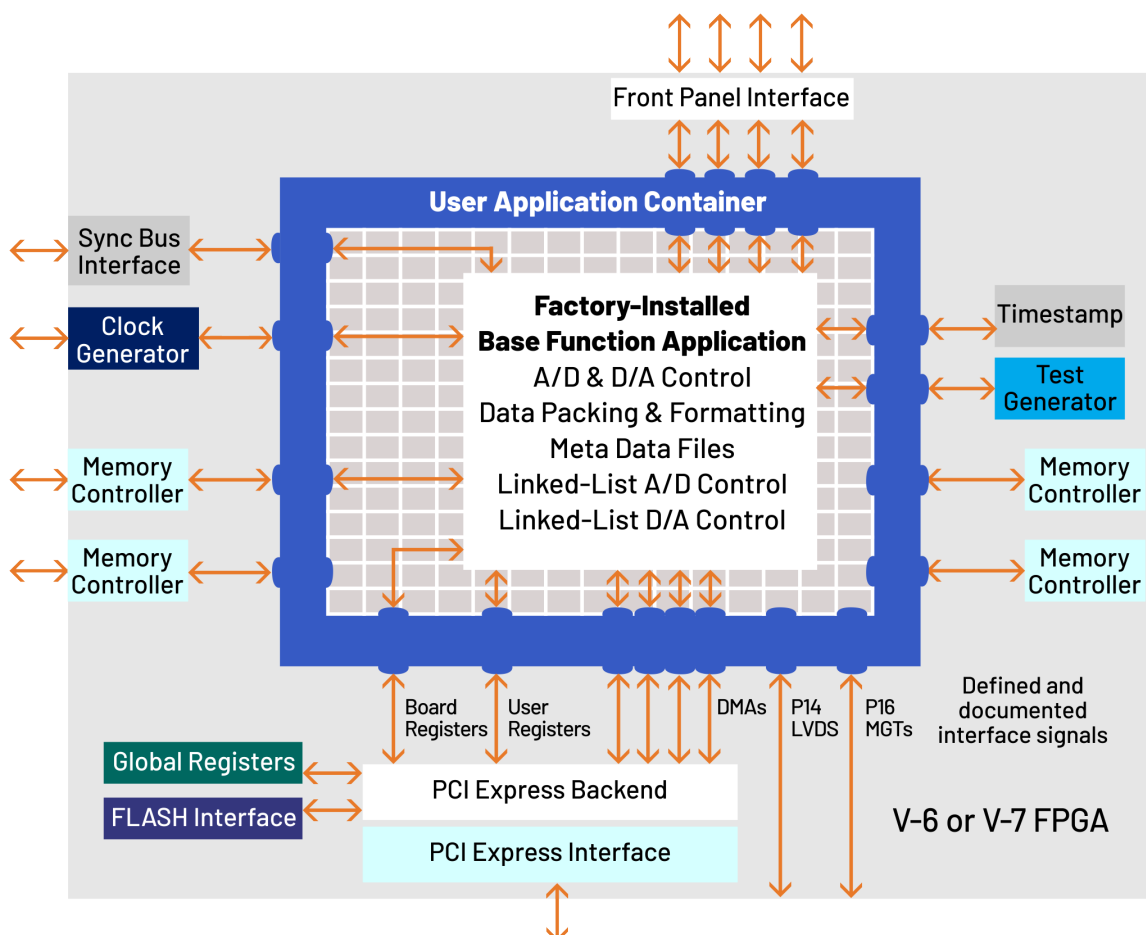
The GateFlow<sup>®</sup> FPGA Design Kit (FDK) allows the user to modify, replace and extend the standard installed functions in the FPGA to incorporate special modes of operation, new control structures, and specialized signal-processing algorithms.

The Cobalt (Virtex-6), Onyx (Virtex-7), and Flexor (Virtex-7) architectures configure the FPGA with standard factory-supplied interfaces including memory controllers, DMA engines, A/D and D/A interfaces, timing and synchronization structures, triggering and gating logic, time stamping and header tagging, data formatting engines, and the PCIe interface. These resources are connected to the User Application Container using well-defined ports that present easy-to-use data and control signals, effectively abstracting the lower-level details of the hardware.

## The User Application Container

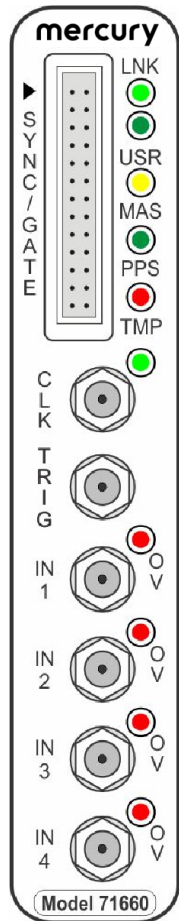
Shown below is the FPGA block diagram of a typical Cobalt, Onyx or Flexor module. The User Application Container holds a collection of different installed IP modules connected to the various interfaces through the standard ports surrounding the container. The specific IP modules for each product are described in further detail in the datasheet of that product.

The GateFlow FDK provides a complete Xilinx's ISE or Vivado project folder containing all the files necessary for the FPGA developer to recompile the entire project with or without any required changes. VHDL source code for each IP module provides excellent examples of how the IP modules work, how they might be modified, and how they might be replaced with custom IP to implement a specific function.



## FRONT PANEL CONNECTIONS

The XMC front panel includes six SSMC coaxial connectors, and a 26-pin µSync Bus connector for input/output of timing and analog signals. The front panel also includes ten LEDs.



- **Sync Bus Connector:** The 26-pin Sync Bus front panel connector labeled **SYNC/GATE** provides clock, sync and gate input/output pins for the Low-Voltage Positive Emitter-Coupled Logic (LVPECL) Sync Bus. When the board is a bus master, these pins output LVPECL Sync Bus signals to other slave units. When the board is a bus Slave, these pins input LVPECL signals from a bus Master.

- **Link LED:** The green **LNK** LED illuminates when a valid link has been established over the PCIe interface.

- **USR LED:** The green **USR** LED is for user applications.

- **Master LED:** the yellow **MAS** LED illuminates when this board is the Sync Bus Master. When only a single board is used, it must be a Master.

- **PPS LED:** the green **PPS** LED illuminates when a valid PPS sign is detected. The LED will blink at the rate of the PPS signal.

- **Over Temperature LED:** The red **TMP** LED illuminates when an over-

temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the PCB.

- **Clock LED:** The green **CLK** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.
- **Clock Input Connector:** One SSMC coaxial connector, labeled **CLK** for the input of an external sample clock.
- **Trigger Input Connector:** The front panel has one SSMC coaxial connector, labeled **TRIG**, for input of an external trigger.
- **Analog Input Connectors:** Four SSMC coaxial connector, labeled **IN 1**, **IN 2**, **IN 3**, and **IN 4** for analog signal inputs, one for each ADC input channel.

- **ADC Overload LEDs:** There are four red **OV** LEDs, one for each A/D input. Use the applicable ADC Data Control Register to select the signal source for each OV LED, either an overload detection in the associated ADS5485, or an ADC FIFO overrun.

## SPECIFICATIONS

57660: 4 A/Ds; 58660: 8 A/Ds

## Front Panel Analog Signal Inputs (4 or 8)

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

## A/D Converters (4 or 8)

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

## Sample Clock Sources (1 or 2)

On-board clock synthesizers

## Clock Synthesizers (1 or 2)

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

## External Clocks (1 or 2)

Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference

## Timing Bus (1 or 2)

26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/ trigger and sync/PPS inputs

## External Trigger Inputs (1 or 2)

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

## Field Programmable Gate Arrays (1 or 2)

- Standard: Xilinx Virtex-6 XC6VLX130T
- Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

**Custom I/O**

- Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, 57660; P3 and P5, 58660
- Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, 57660; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, 58660

**Memory Banks (1 or 2)**

- Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI Express Interface**

PCI Express Bus: Gen. 1 or Gen. 2: x4 or x8

**Environmental**

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

**Physical**

Dimensions:

- Depth: 171 mm (6.717 in.)
- Height: 100 mm (3.937 in.)

Weight: VPX Carrier: 110 grams (3.9 oz)

**ORDERING INFORMATION**

Model	Description
57660	4-Channel 200 MHz A/D with Virtex-6 FPGA - 6U VPX
58660	8-Channel 200 MHz 16-bit A/D with two Virtex-6 FPGAs - 6U VPX

Options	Description
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and P3 connector, 57660; P3 and P5 connectors, 58660
-105	Gigabit link between the FPGA and P2 connector, 57660; gigabit links from each FPGA to P2 connector, 58660
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
-702	Air-cooled, Level 2
-763	Conduction-cooled, Level 3
*This option is always required. Contact Mercury for compatible option combinations.	

**ACCESSORY PRODUCTS**

Model	Description
2171	Cable Kit: SSMC to SMA



## FORM FACTORS

Cobalt products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Cobalt Model 71660 XMC (4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA) has the following variants:

Model	
52660	3U VPX board (single XMC)
57660	6U VPX board (single XMC)
58660	6U VPX board (dual XMC)
71660	XMC module
78660	PCIe board (single XMC)

## DEVELOPMENT SYSTEMS

Mercury offers development systems for Cobalt products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Cobalt boards. Please [contact Mercury](#) to configure a system that matches your requirements.



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