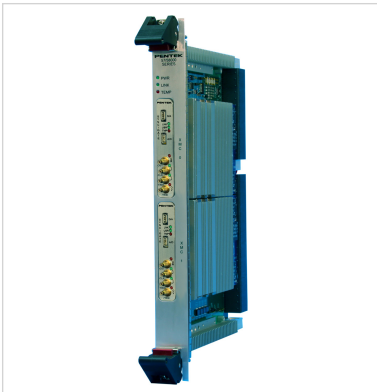


Cobalt 57630/58630

1- or 2-channel 1 GHz A/D, 1- or 2-channel 1 GHz D/A
6U VPX boards with Virtex-6 FPGA

Complete radar and software radio interface solution

- Radar and communication receiver and transmitter
- Electronic Warfare transponder
- Waveform signal generator
- Wideband data acquisition
- Remote monitoring
- Sensor interfaces



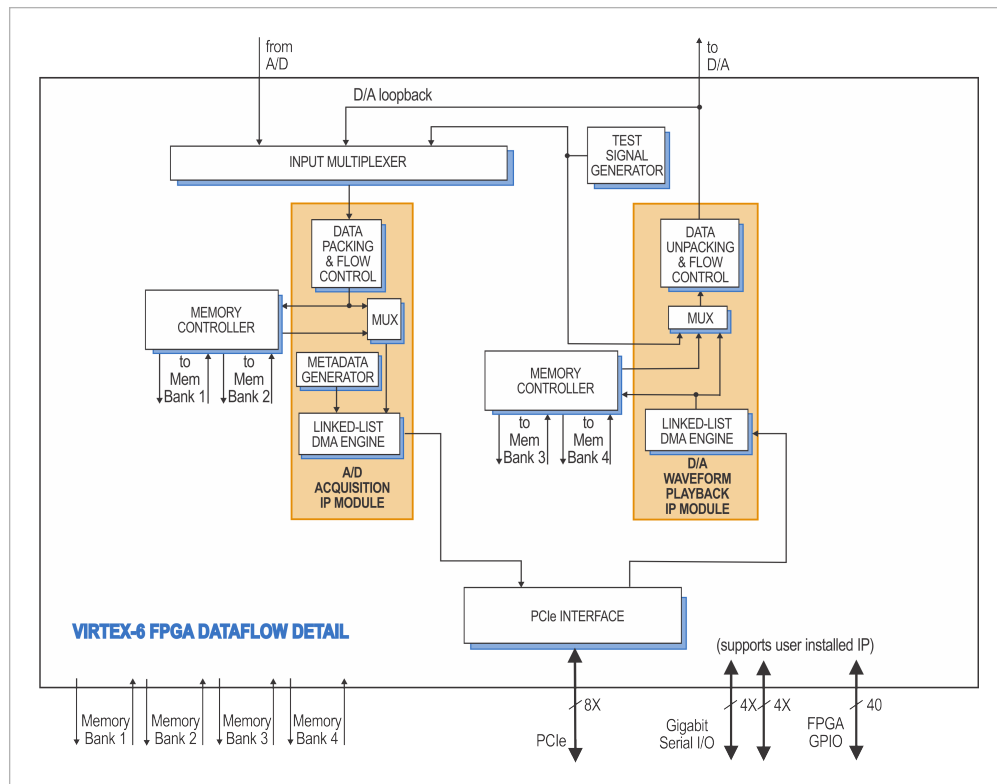
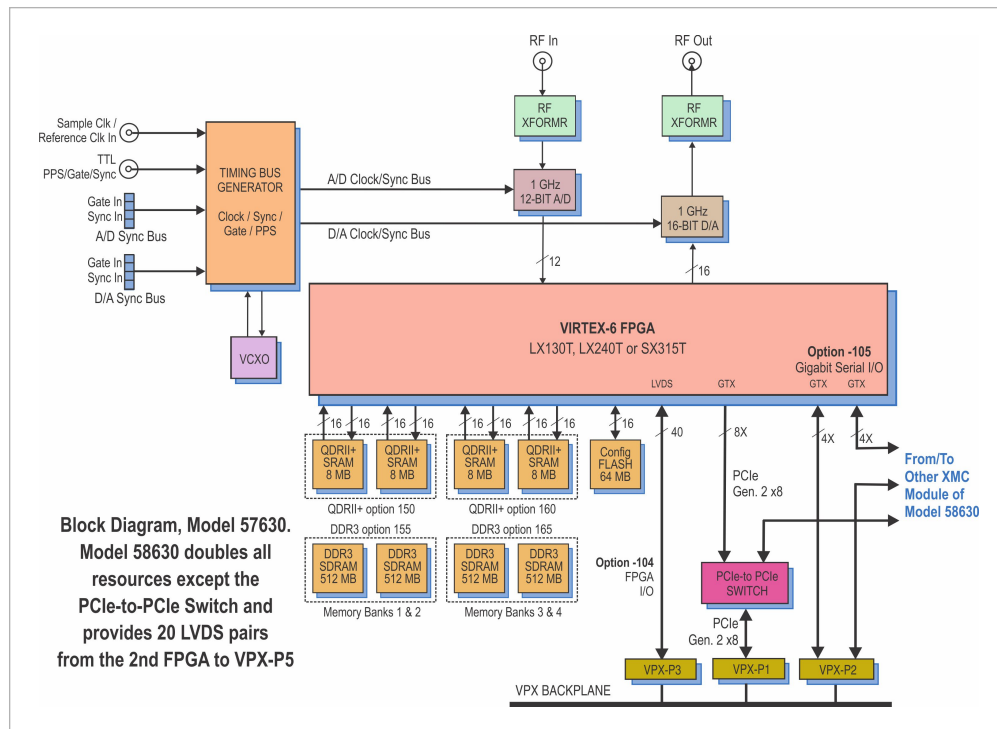
Models 57630 and 58630 consist of one or two Model 71630 XMC modules mounted on a VPX carrier board. The 57630 is a 6U board with one 71630 module while the 58630 is a 6U board with two XMC modules rather than one.

These models include one or two 1 GHz A/D and D/A converters and four or eight banks of memory.

FEATURES

- Supports Xilinx® Virtex®-6 LXT and SXT FPGA
- One or two 1 GHz 12-bit A/D
- One or two 1 GHz 16-bit D/A
- Up to 2 GB or 4 GB of DDR3 SDRAM or: 16 MB or 32 MB of QDRII+ SRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

57630 BLOCK DIAGRAMS



THE COBALT ARCHITECTURE

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's interface. The factory installed functions of these models include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

IP modules for DDR3 SDRAM memories, a controller for all data clocking, a test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as a complete turnkey solutions without the need to develop any FPGA IP.

EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. The GateFlow FPGA Design Kits include all of the factory-installed modules as document source code. Developers can integrate their own IP with the factory-installed functions or use the GateFlow kit to completely replace the IP with their own.

XILINX VIRTEX-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

A/D CONVERTER STAGE

The board's analog interface accepts one or two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into one or two Texas Instruments ADS5400 1 GHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

A/D ACQUISITION MODULES

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Play-back IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A CONVERTER STAGE

These models feature one or two Texas Instruments DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

D/A WAVEFORM PLAYBACK IP MODULES

The factory-installed functions include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 28 individual link entries can be chained together to create complex waveforms with a minimum of programming.

CLOCKING AND SYNCHRONIZATION

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel μ Sync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board's sync and gate/trigger signals.

The 9192 Cobalt Synchronizer can drive multiple μ Sync connectors enabling large, multichannel synchronous configurations. Also, an LVTTTL external gate/trigger input is accepted on a front panel SSMC connector.

MEMORY RESOURCES

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI EXPRESS INTERFACE

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

READYFLOW

Mercury provides ReadyFlow[®] BSPs (Board Support Packages) for all Cobalt, Onyx, and Flexor products. Available for both Linux and Windows, these packages:

- Provide a path for quick start-up through application completion
- Allow programming at high, intermediate and low levels to meet various needs
- Are illustrated with numerous examples
- Include complete documentation and definitions of all functions
- Include library and example source code.

ReadyFlow BSPs contain C-language examples that can be used to demonstrate the capabilities of Cobalt, Onyx, and Flexor products. These programming examples will help you get an immediate start on writing your own application. They provide sample code that is known to work, giving you a means of verifying that your board set is operational.

COMMAND LINE INTERFACE

The Command Line Interface provides access to pre-compiled executable examples that operate the hardware right out of the box, without the need to write any code. Board-specific hardware

operating arguments can be entered in the command line to control parameters: number of channels to enable, sample clock frequency, data transfer size, reference clock frequency, reference clock source, etc.

The Command Line Interface can be used to call an example application from within a larger user application to control the hardware, and parameter arguments are passed to the application for execution. Functions that control data acquisition automatically save captured data to a pre-named host file or are routed to the Signal Analyzer example function for display.

SIGNAL ANALYZER

When used with the Command Line Interface, the Signal Analyzer allows users to immediately start acquiring and displaying A/D data. A full-featured analysis tool, the Signal Analyzer displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD, and SINAD. Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals.



GATEFLOW

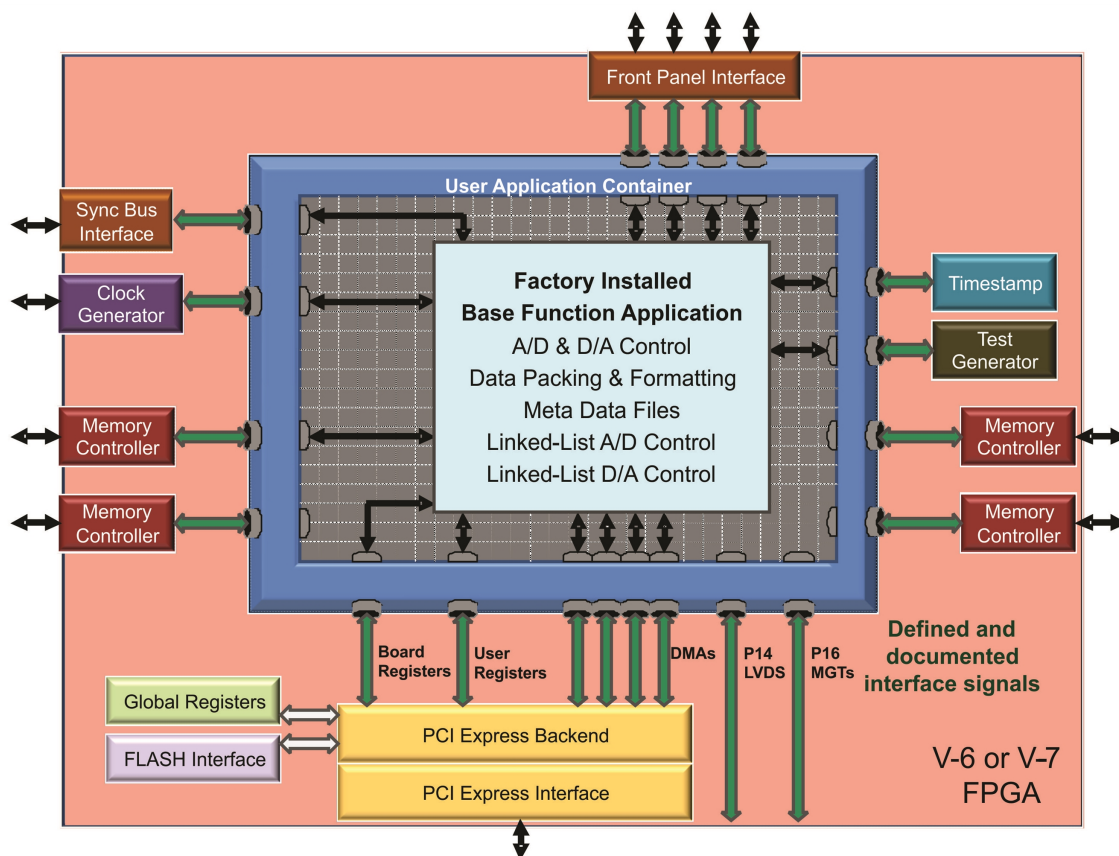
The GateFlow[®] FPGA Design Kit (FDK) allows the user to modify, replace and extend the standard installed functions in the FPGA to incorporate special modes of operation, new control structures, and specialized signal-processing algorithms.

The Cobalt (Virtex-6), Onyx (Virtex-7), and Flexor (Virtex-7) architectures configure the FPGA with standard factory-supplied interfaces including memory controllers, DMA engines, A/D and D/A interfaces, timing and synchronization structures, triggering and gating logic, time stamping and header tagging, data formatting engines, and the PCIe interface. These resources are connected to the User Application Container using well-defined ports that present easy-to-use data and control signals, effectively abstracting the lower-level details of the hardware.

The User Application Container

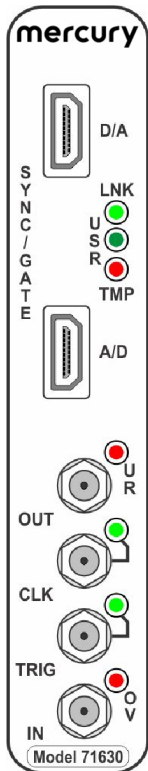
Shown below is the FPGA block diagram of a typical Cobalt, Onyx or Flexor module. The User Application Container holds a collection of different installed IP modules connected to the various interfaces through the standard ports surrounding the container. The specific IP modules for each product are described in further detail in the datasheet of that product.

The GateFlow FDK provides a complete Xilinx's ISE or Vivado project folder containing all the files necessary for the FPGA developer to recompile the entire project with or without any required changes. VHDL source code for each IP module provides excellent examples of how the IP modules work, how they might be modified, and how they might be replaced with custom IP to implement a specific function.



FRONT PANEL CONNECTIONS

The XMC front panel includes two 19-pin µSync connectors, and four SSMC coaxial connectors for input/output of timing and analog signals. The front panel also includes seven LEDs.



- **Sync Bus Connector:** Two 19-pin Sync Bus front panel connectors, labeled **SYNC/GATE**, provide sync, and gate input signals pins for the Sync Bus. The top connector, labeled **D/A** is for DAC timing inputs and the lower connector, labeled **A/D** is for ADC timing inputs.
- **Link LED:** The green **LNK** LED illuminates when a valid link has been established over the PCIe interface
- **User LED:** The green **USR** LED is for user applications.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the printed circuit board (PCB).
- **DAC Underrun LED:** There is one red **UR** (underrun) LED for the D/A output. This LED illuminates when the DAC5681Z FIFO is out of data.
- **Analog Output Connector:** The one SSMC coaxial connect, labeled **OUT**, is for analog signal output from the DAC 5681Z. It is driven by a RF transfer into 50Ω output impedance.
- **Clock Input Connector:** One SSMC coaxial connector, labeled **CLK**, is for input of an external sample clock.
- **Clock LED:** The green **CLK** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed. It is to the right of the **CLK** output
- **Analog Output Connector:** One SSMC coaxial connector, labeled **OUT** for the DAC5681Z output.
- **Trigger Input Connector:** One SSMC coaxial connector, labeled **TRIG** for input of an external gate or trigger signal.
- **PPS LED:** The green LED to the right of the TRIG input illuminates when a valid PPS sign is detected. The LED will blink at the rate of the PPS signal.

- **Analog Input Connector:** One SSMC coaxial connector, labeled **IN** for the ADS5400 input channel.
- **ADC Overload LED:** The red **OV** (overload) LED indicates either an overload in the ADS5400 or an ADC FIFO overrun.

SPECIFICATIONS

57630: 1 A/D, 1 D/A; 58630: 2 A/Ds, 2 D/As

Front Panel Analog Signal Inputs (1 or 2)

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converters (1 or 2)

Type: Texas Instruments ADS5400

Sampling Rate: 100 MHz to 1 GHz

Resolution: 12 bits

D/A Converters (1 or 2)

Type: Texas Instruments DAC5681Z

Input Data Rate: 1 GHz max.

Interpolation Filter: bypass, 2x or 4x

Output Sampling Rate: 1 GHz max.

Resolution: 16 bits

Front Panel Analog Signal Outputs (1 or 2)

Output Type: Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources (1 or 2)

On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)

Clock Source: Selectable from on-board programmable VCXO or front panel external clock

VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz

Synchronization: VCXO can be locked to an external 4 to 200 MHz system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)

Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

Timing Bus (1 or 2)

19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input (1 or 2)

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)

- Standard: Xilinx Virtex-6 XC6VLX130T-2
- Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O

- Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, 57630; P3 and P5, 58630
- Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, 57630; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, 58630A

Memory Banks (1 or 2)

- Option 150: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI Express Interface

PCI Express Bus: Gen. 1 or 2: x4 or x8

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions:

- Depth: 171 mm (6.717 in.)
- Height: 100 mm (3.937 in.)

Weight: VPX Carrier: 110 grams (3.9 oz)

ORDERING INFORMATION

| Model | Description |
|-------|---|
| 57630 | 1 GHz A/D and D/A, Virtex-6 FPGA - 6U VPX |
| 58630 | Two 1 GHz A/D and D/A, with two Virtex-6 FPGAs - 6U VPX |

| Options | Description |
|---------|--|
| -002* | -2 FPGA speed grade |
| -062 | XC6VLX240T FPGA |
| -064 | XC6VSX315T FPGA |
| -104 | LVDS I/O between the FPGA and P3 connector, 57630; P3 and P5 connectors, 58630 |
| -105 | Gigabit link between the FPGA and P2 connector, 57630; gigabit links from each FPGA to P2 connector, 78630 |
| -155 | Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2) |
| -160 | Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4) |
| -165 | Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4) |
| -702 | Air-cooled, Level 2 |
| -763 | Conduction-cooled, Level 3 |

*This option is always required. Contact Mercury for compatible option combinations.

ACCESSORY PRODUCTS

| Model | Description |
|-------|---|
| 2171 | Cable Kit: SSMC to SMA |
| 5792 | High-Speed System Synchronization and Distribution Amplifier - 6U VPX |
| 5892 | High-Speed Synchronizer and Distribution Board |
| 9192 | Rackmount High-Speed System Synchronizer |

DEVELOPMENT SYSTEMS

Mercury offers development systems for Cobalt products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Cobalt boards. Please [contact Mercury](#) to configure a system that matches your requirements.

FORM FACTORS

Cobalt products are available in standard form factors including 3U VPX, 6U VPX, PCIe, and XMC. The Cobalt Model 71630 XMC (1 GHz A/D and D/A with Virtex-6 FPGA) has the following variants:

| Model | |
|-------|---------------------------|
| 52630 | 3U VPX board (single XMC) |
| 57630 | 6U VPX board (single XMC) |
| 58630 | 6U VPX board (dual XMC) |
| 71630 | XMC module |
| 78630 | PCIe board (single XMC) |

LIFETIME SUPPORT FOR COBALT PRODUCTS

Mercury offers worldwide customers shorter development time, reliable, rugged solutions for a variety of environments, reduced costs, and mature software development tools. We offer free lifetime support from our engineering staff, which customers can depend on through phone and email, as well as software updates. Take advantage of our 40 years of experience in delivering high-performance radar, communications, SIGINT, EW, and data acquisition MIL-Aero solutions worldwide.



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Learn more

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For technical details, contact:
mrcy.com/go/CF57630



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