Model 7191

Programmable multifrequency clock synthesizer – PMC module

Ideal for A/D and D/A converter clock sources

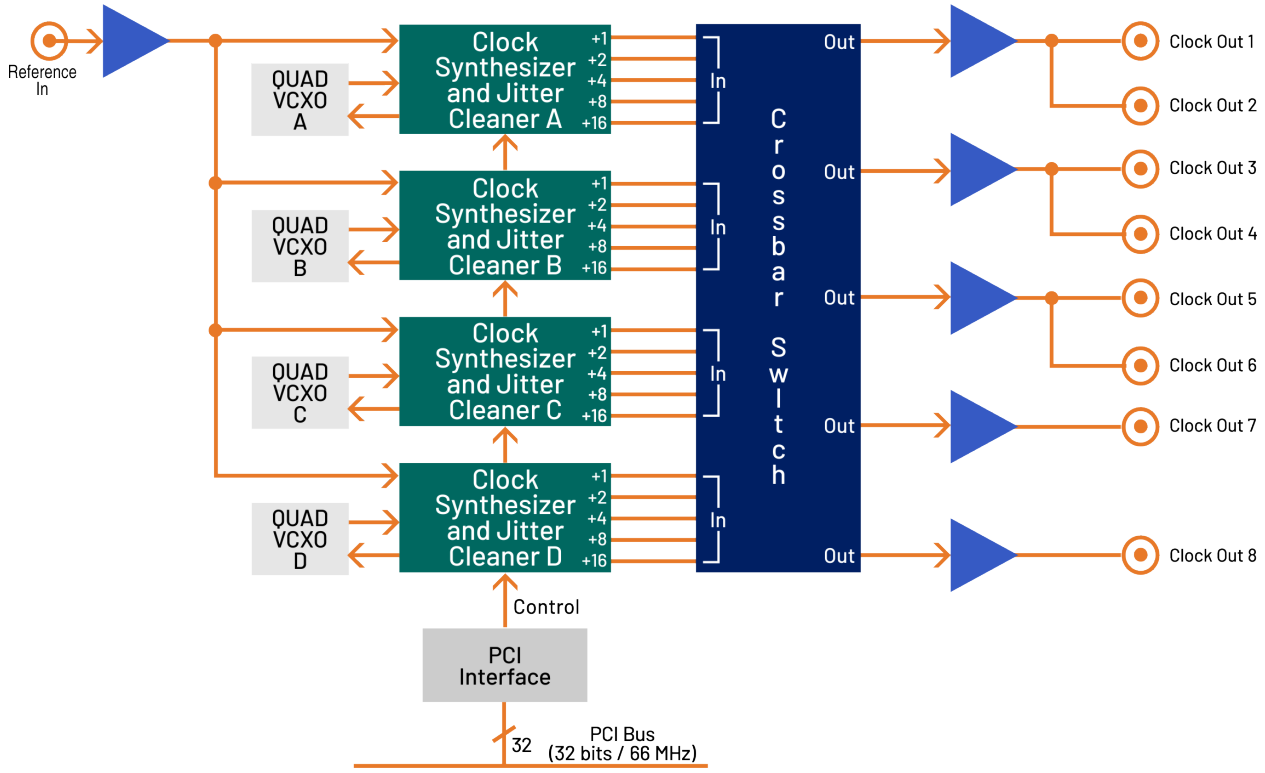
- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Typical phase noise: –105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal

The Model 7191 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

FEATURES

- Input reference frequency of 5 to 100 MHz
- Four programmable VCXOs with 32-bit tuning resolution
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCI bus interface

BLOCK DIAGRAM



CLOCK SYNTHESIZER CIRCUITS

The 7191 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to generate one of four frequencies between 50 and 700 MHz with a 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7191 can be programmed to route any of these 20 frequencies to the module's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

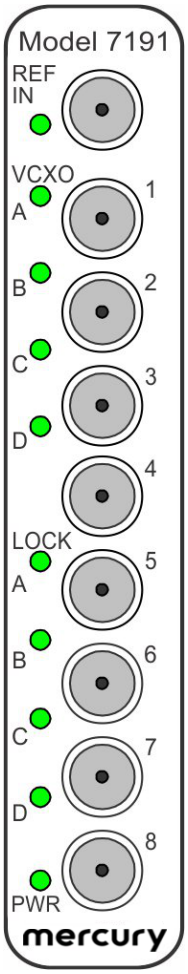
With four independently programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7191's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI INTERFACE

The Model 7191 uses an industry-standard 32-bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. The interface allows reading and writing of status and control signals for setup, operation and monitoring of the module.

FRONT PANEL CONNECTIONS

The front panel includes one SMC connector for a reference signal input, eight SMC connectors for clock outputs and ten LED indicators. Please use the cables described in Ordering Information.



- **Reference Input Connector:** One SMC receptacle, labeled **REF IN**, for input of an external reference clock.
- **Clock Output Connectors:** Eight SMC connectors for the Clock signal inputs labeled **CLK 1 - 8**. The clock output signal is within the range of +4 dBm. This output is driven into 50 Ω output impedance.
- **REF IN LED:** A green LED labeled **REF IN** illuminates when a reference clock input is applied to the board.
- **VCXO LEDs:** Four green LEDs labeled **VCXO A-D** illuminate when the associated VCXO input is valid (A is for VCXO 1, B for VCXO 2, C for VCXO 3, D for VCXO 4).
- **Lock LEDs:** Four green LEDs labeled **LOCK A-D**illuminate when the associated VCXO PLL is locked (**A** is for VCXO 1, **B** for VCXO 2, **C** for VCXO 3, **D** for VCXO 4).
- **Power LED:** A green LED labeled **PWR** illuminates when a +5VDC is applied to the board.

SPECIFICATIONS

Front Panel Reference Input

Connector Type: SMC

Input Impedance: 50 ohms

Reference Frequency: 5 to 100 MHz

Input Level: -6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaner

Quantity: 4

Type: Texas Instruments CDC7005

Frequency Dividers: 1, 2, 4, 8 and 16

Programmable VXCOs (Quantity: 4)

Frequency Range: 50 to 700 MHz

Tuning Resolution: 32 bits

Unlocked Accuracy: ±20 ppm

Front Panel Clock Outputs (Quantity: 8)

Connector Type: SMC

Output Impedance: 50 ohms

Output Level: +3 dBm @ 700 MHz

Typ. Phase Noise: –105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI Interface

PCI Bus: 32-bit, 66 MHz (supports 33 MHz)

Operation: control and status interface

Environmental

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.

Size

Standard PMC module: 2.91 in. x 5.87 in.

ORDERING INFORMATION

Model	Description
7191*	Programmable Multifrequency Clock Synthesizer - PMC

*Specify frequencies of factory-installed programmable VCXOs between 50 and 700 MHz. Contact techsales@mrcy.com to order specific frequencies.

ACCESSORY PRODUCTS

Model	Description
2891	Timing bus cables

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