

128Kx8 MONOLITHIC SRAM

SMD 5962-96691

WMS128K8-XXX



FEATURES

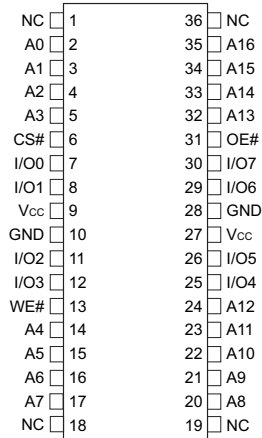
- Access Times 15, 17, 20, 25, 35, 45, 55ns
- Revolutionary, Center Power/Ground Pinout JEDEC Approved
 - 32 lead Ceramic SOJ (Package 101)
 - 36 lead Ceramic Flat Pack (Package 226)
- Evolutionary, Corner Power/Ground Pinout JEDEC Approved
 - 32 pin Ceramic DIP (Package 300)
 - 32 lead Ceramic SOJ (Package 101)
 - 32 lead Ceramic Flat Pack (Package 206)
- 32 pin, Rectangular Ceramic Leadless Chip Carrier (Package 601)
- MIL-STD-883 Compliant Devices Available
- Commercial, Industrial and Military Temperature Range
- 5 Volt Power Supply
- Low Power CMOS
- 2V Data Retention Devices Available (Low Power Version)
- TTL Compatible Inputs and Outputs

This product is subject to change without notice.

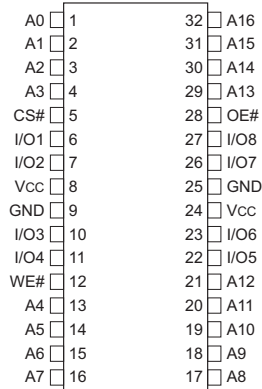
Revolutionary Pinout

Evolutionary Pinout

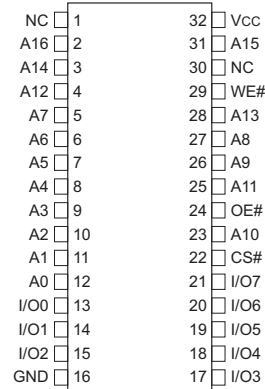
36 FLAT PACK
Top View



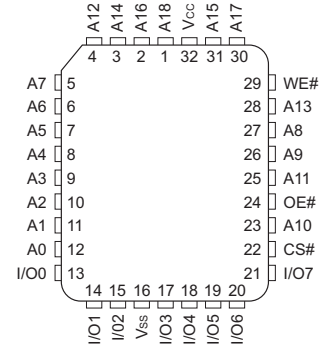
32 CSOJ (DR)
Top View



32 DIP
32 CSOJ (DE)
32 FLATPACK (FE)
Top View



32 CLCC
Top View



Pin Description

| | |
|--------|-------------------|
| A0-16 | Address Inputs |
| I/O0-7 | Data Input/Output |
| CS | Chip Select |
| OE | Output Enable |
| WE | Write Enable |
| Vcc | +5.0V Power |
| GND | Ground |

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Min | Max | Unit |
|--------------------------------|------------------|------|----------------------|------|
| Operating Temperature | T _A | -55 | +125 | °C |
| Storage Temperature | T _{STG} | -65 | +150 | °C |
| Signal Voltage Relative to GND | V _G | -0.5 | V _{CC} +0.5 | V |
| Junction Temperature | T _J | | 150 | °C |
| Supply Voltage | V _{CC} | -0.5 | 7.0 | V |

TRUTH TABLE

| CS# | OE# | WE# | Mode | Data I/O | Power |
|-----|-----|-----|-------------|----------|---------|
| H | X | X | Standby | High Z | Standby |
| L | L | H | Read | Data Out | Active |
| L | X | L | Write | Data In | Active |
| L | H | H | Out Disable | High Z | Active |

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Unit |
|------------------------|-----------------|------|-----------------------|------|
| Supply Voltage | V _{CC} | 4.5 | 5.5 | V |
| Input High Voltage | V _{IH} | 2.2 | V _{CC} + 0.3 | V |
| Input Low Voltage | V _{IL} | -0.5 | +0.8 | V |
| Operating Temp. (Mil.) | T _A | -55 | +125 | °C |

CAPACITANCET_A = +25°C

| Parameter | Symbol | Condition | Package | Speed (ns) | Max | Unit |
|--------------------|------------------|-----------------------------------|---|------------|-----|------|
| Input capacitance | C _{IN} | V _{IN} = 0V, f = 1.0MHz | 32 Pin CSOJ, DIP, Flat Pack Evolutionary | 15 to 55 | 20 | pF |
| | | | 36 Pin Flat Pack and 32 Pin CSOJ Revolutionary | 15 to 25 | 12 | pF |
| | | | | 35 to 55 | 20 | pF |
| Output capacitance | C _{OUT} | V _{OUT} = 0V, f = 1.0MHz | 32 Pin CSOJ, DIP, Flat Pack Evolutionary | 15 to 55 | 20 | pF |
| | | | 36 Pin Flat Pack and 32 Pin CSOJ Revolutionary | 15 to 55 | 12 | pF |
| | | | | 35 to 55 | 20 | pF |
| | | | 32 Pin CLCC | 15 to 55 | 15 | pF |

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICSV_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ +125°C

| Parameter | Symbol | Conditions | -15 | | -17 | | -20 | | -25 | | -35 | | -45 | | -55 | | Units |
|--------------------------|-----------------|---|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-------|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Input Leakage Current | I _{LI} | V _{CC} = 5.5, V _{IN} = GND to V _{CC} | | 10 | | 10 | | 10 | | 10 | | 10 | | 10 | | 10 | μA |
| Output Leakage Current | I _{LO} | CS# = V _{IH} , OE# = V _{IH} , V _{OUT} = GND to V _{CC} | | 10 | | 10 | | 10 | | 10 | | 10 | | 10 | | 10 | μA |
| Operating Supply Current | I _{CC} | CS# = V _{IL} , OE# = V _{IH} , f = 5MHz, V _{CC} = 5.5 | | 150 | | 150 | | 150 | | 150 | | 150 | | 150 | | 150 | mA |
| Standby Current | I _{SB} | CS# = V _{IH} , OE# = V _{IH} , f = 5MHz, V _{CC} = 5.5 | | 20 | | 20 | | 20 | | 15 | | 15 | | 15 | | 15 | mA |
| Output Low Voltage | V _{OL} | I _{OL} = 2.1mA, V _{CC} = 4.5 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | V |
| Output High Voltage | V _{OH} | I _{OH} = -1.0mA, V _{CC} = 4.5 | 2.4 | | 2.4 | | 2.4 | | 2.4 | | 2.4 | | 2.4 | | 2.4 | | V |

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V

AC CHARACTERISTICS

V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ 125°C

| Parameter Read Cycle | Symbol | -15 | | -17 | | -20 | | -25 | | -35 | | -45 | | -55 | | Unit |
|------------------------------------|-------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | t _{RC} | 15 | | 17 | | 20 | | 25 | | 35 | | 45 | | 55 | | ns |
| Address Access Time | t _{AA} | | 15 | | 17 | | 20 | | 25 | | 35 | | 45 | | 55 | ns |
| Output Hold from Address Change | t _{OH} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Chip Select Access Time | t _{ACS} | | 15 | | 17 | | 20 | | 25 | | 35 | | 45 | | 55 | ns |
| Output Enable to Output Valid | t _{OE} | | 10 | | 10 | | 12 | | 15 | | 20 | | 25 | | 30 | ns |
| Chip Select to Output in Low Z | t _{CLZ} ¹ | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| Output Enable to Output in Low Z | t _{OLZ} ¹ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Chip Disable to Output in High Z | t _{CHZ} ¹ | | 10 | | 10 | | 10 | | 12 | | 20 | | 20 | | 20 | ns |
| Output Disable to Output in High Z | t _{OHZ} ¹ | | 10 | | 10 | | 10 | | 12 | | 20 | | 20 | | 20 | ns |

1. This parameter is guaranteed by design but not tested.

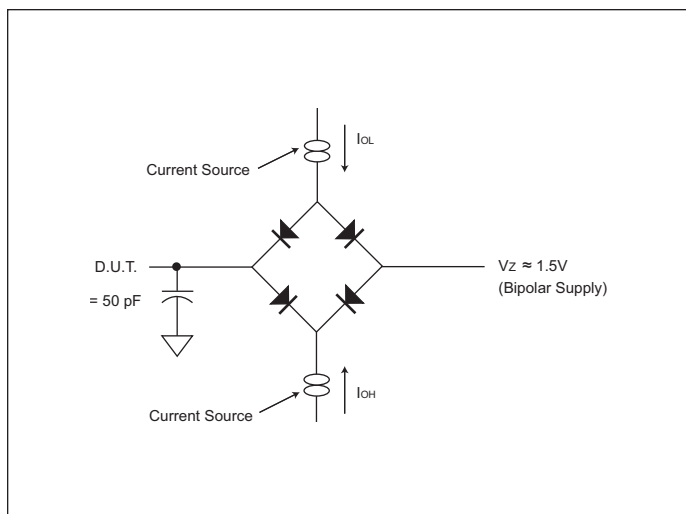
AC CHARACTERISTICS

V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ 125°C

| Parameter Write Cycle | Symbol | -15 | | -17 | | -20 | | -25 | | -35 | | -45 | | -55 | | Unit |
|----------------------------------|-------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | t _{WC} | 15 | | 17 | | 20 | | 25 | | 35 | | 45 | | 55 | | ns |
| Chip Select to End of Write | t _{CW} | 14 | | 14 | | 15 | | 20 | | 25 | | 30 | | 45 | | ns |
| Address Valid to End of Write | t _{AW} | 14 | | 15 | | 15 | | 20 | | 25 | | 30 | | 45 | | ns |
| Data Valid to End of Write | t _{DW} | 10 | | 10 | | 12 | | 15 | | 20 | | 25 | | 25 | | ns |
| Write Pulse Width | t _{WP} | 14 | | 14 | | 15 | | 20 | | 25 | | 30 | | 45 | | ns |
| Address Setup Time | t _{AS} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Address Hold Time | t _{AH} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Output Active from End of Write | t _{OW} ¹ | 3 | | 3 | | 3 | | 3 | | 4 | | 4 | | 4 | | ns |
| Write Enable to Output in High Z | t _{WHZ} ¹ | | 10 | | 10 | | 12 | | 15 | | 20 | | 25 | | 25 | ns |
| Data Hold Time | t _{DH} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT



AC TEST CONDITIONS

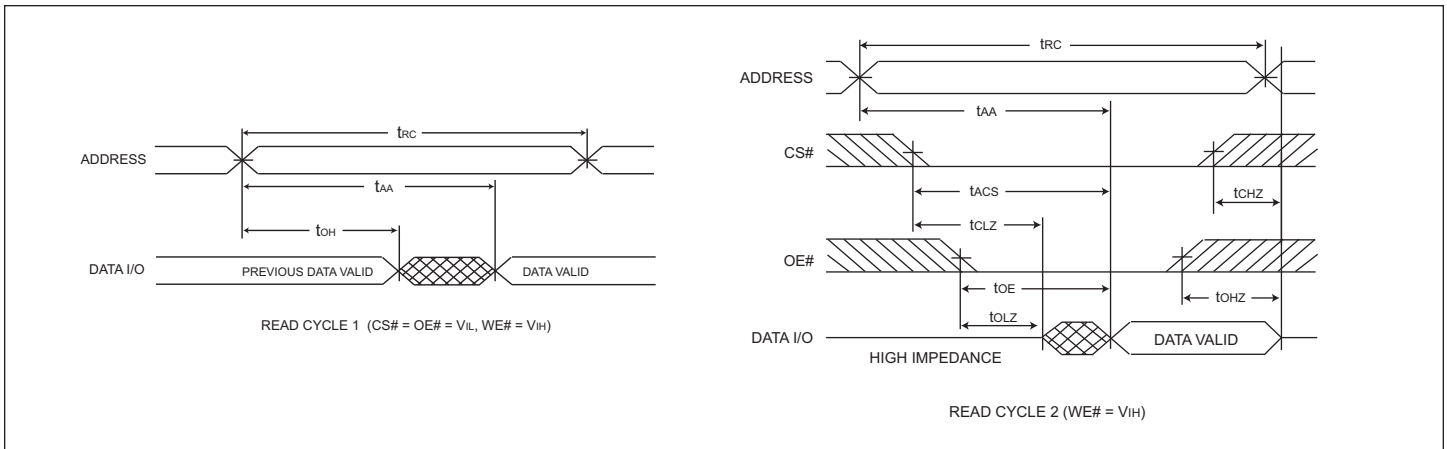
| Parameter | Typ | Unit |
|----------------------------------|--|------|
| Input Pulse Levels | V _{IL} = 0, V _{IH} = 3.0 | V |
| Input Rise and Fall | 5 | ns |
| Input and Output Reference Level | 1.5 | V |
| Output Timing Reference Level | 1.5 | V |

NOTES:

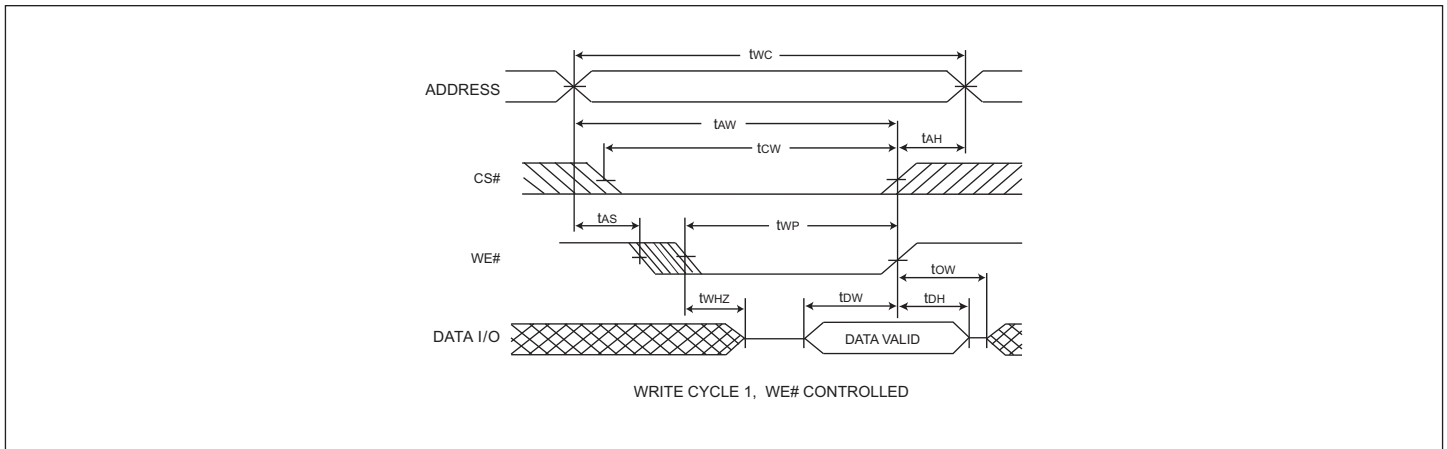
V_Z is programmable from -2V to +7V.I_{OL} & I_{OH} programmable from 0 to 16mA.Tester Impedance Z₀ = 75Ω.V_Z is typically the midpoint of V_{OH} and V_{OL}.I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.

ATE tester includes jig capacitance.

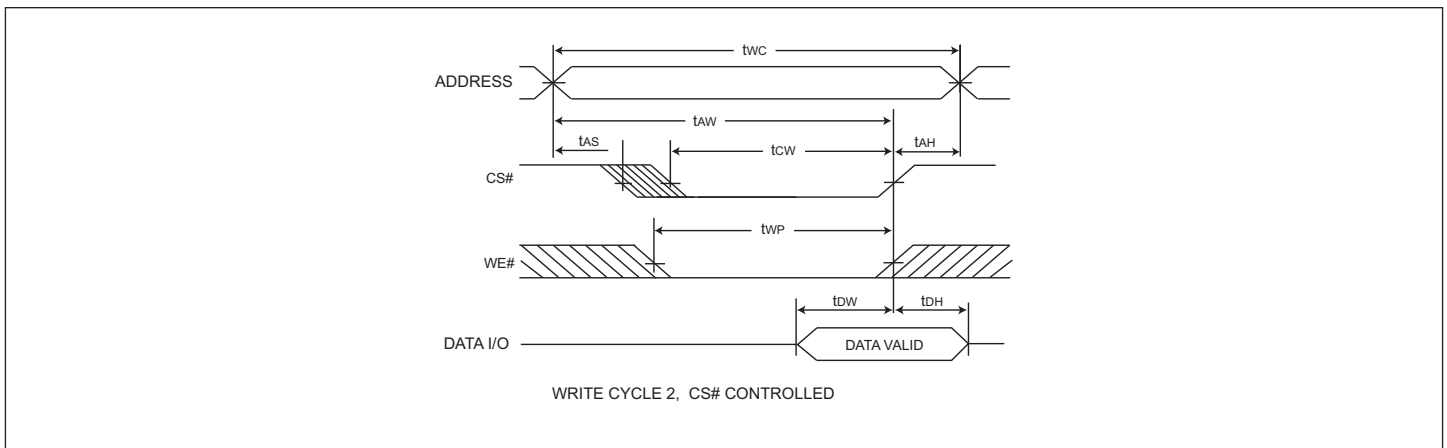
TIMING WAVEFORM – READ CYCLE



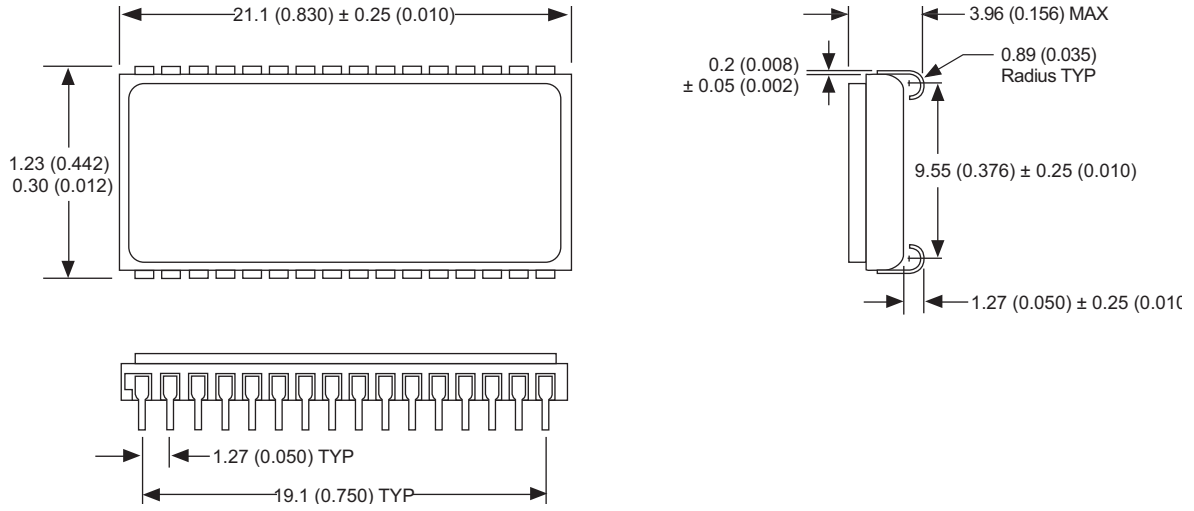
WRITE CYCLE – WE# CONTROLLED



WRITE CYCLE – CS# CONTROLLED

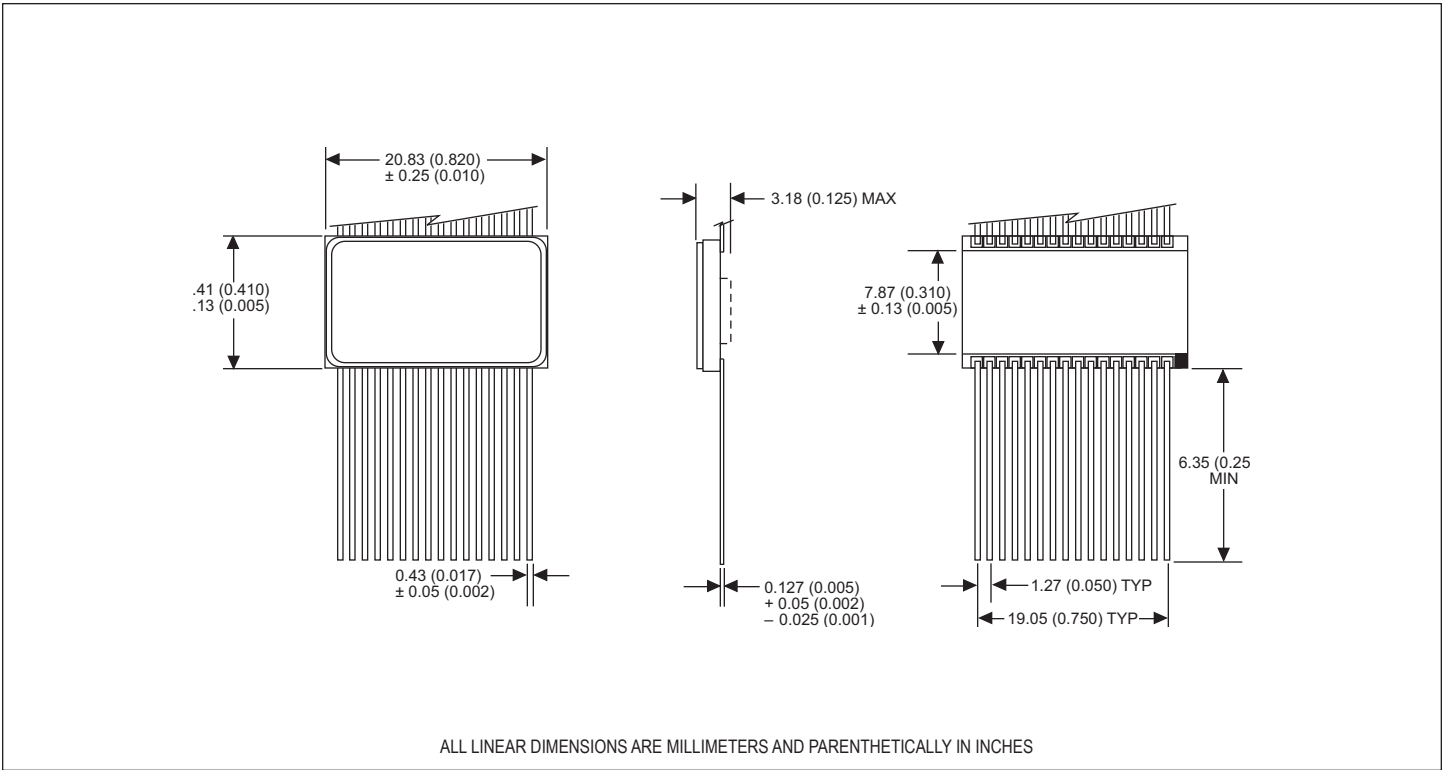


PACKAGE 101 – 32 LEAD, CERAMIC SOJ

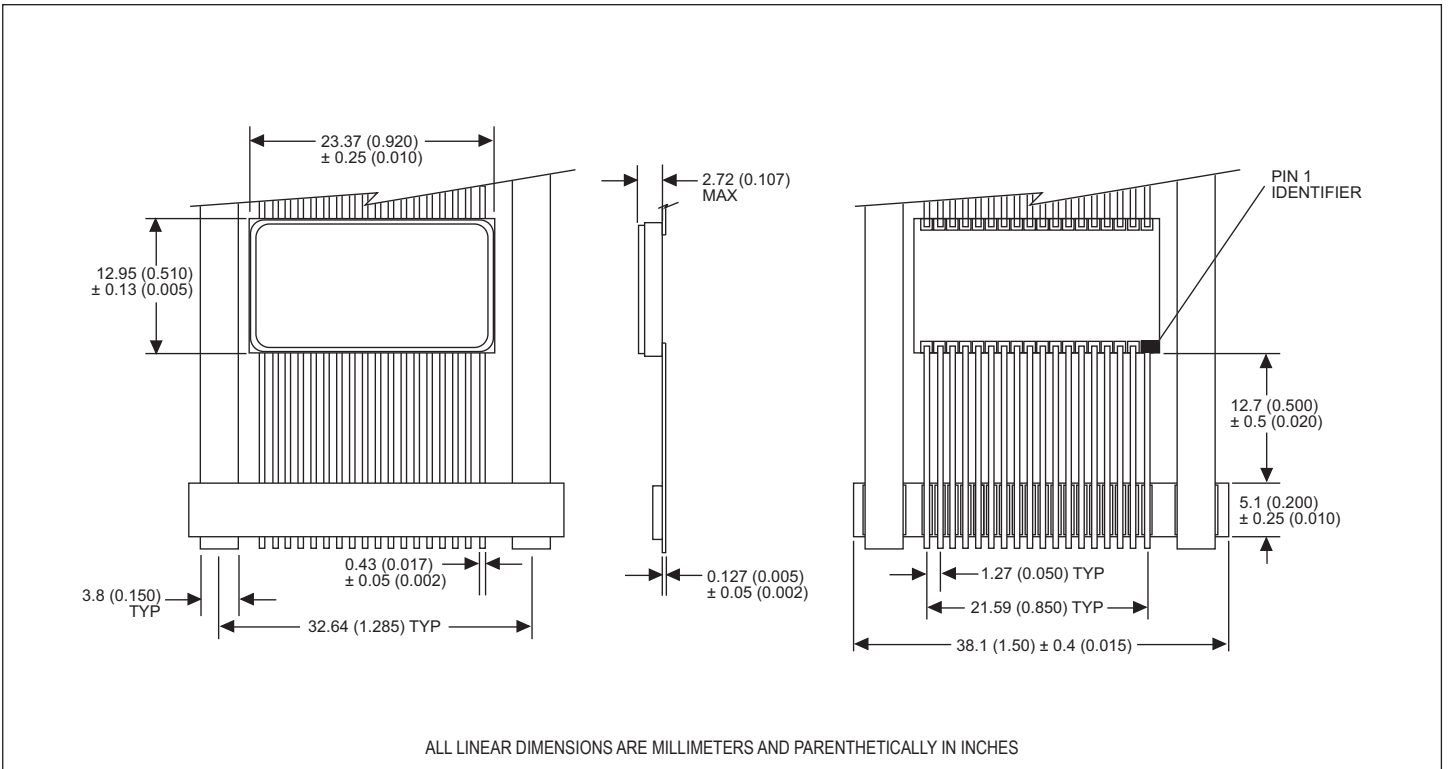


ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

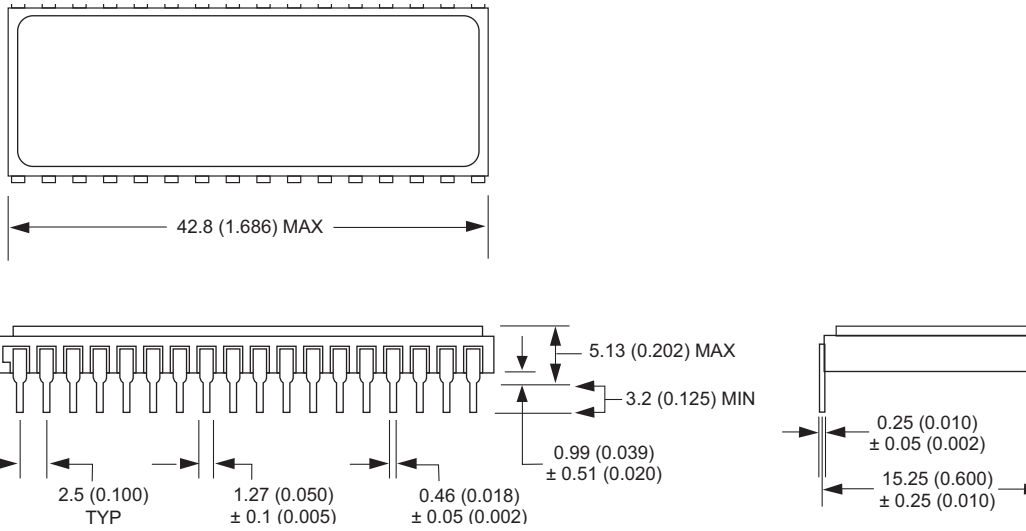
PACKAGE 206 – 32 LEAD, CERAMIC FLAT PACK



PACKAGE 226 – 36 LEAD, CERAMIC FLAT PACK

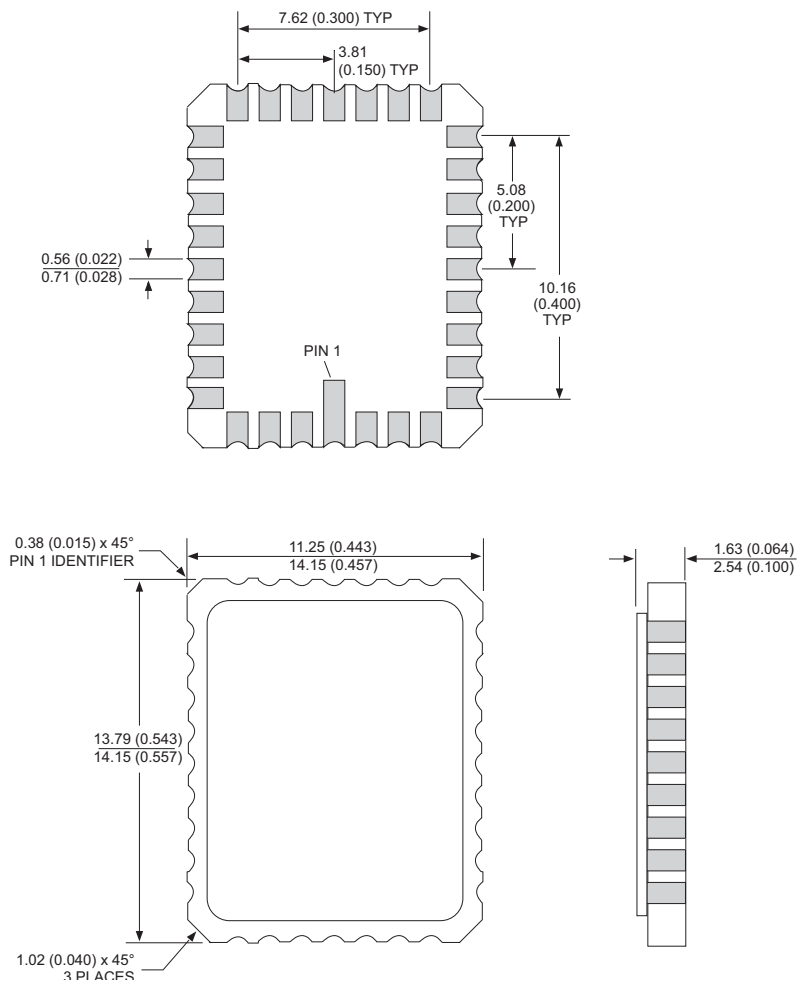


PACKAGE 300 – 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 601 – 32 PIN, RECTANGULAR CERAMIC LEADLESS CHIP CARRIER



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

DATA RETENTION CHARACTERISTICS

-55°C ≤ T_A ≤ +125°C
Low Power L Version Only

| Parameter | Symbol | Conditions | Min | Max | Units |
|-------------------------------|--------------------|------------------------------|-----|-----|-------|
| Data Retention Supply Voltage | V _{DR} | CS# ≥ V _{CC} - 0.2V | 2.0 | 5.5 | V |
| Data Retention Current | I _{CCDR3} | V _{CC} = 2V | | 400 | μA |

ORDERING INFORMATION

W M S 128K8 X - XXX X X X

MICROSEMI CORPORATION _____

MONOLITHIC _____

SRAM _____

ORGANIZATION, 128K x 8 _____

IMPROVEMENT MARK _____

L = Low Power for 2V Data Retention

ACCESS TIME (ns) _____

PACKAGE: _____

- C = 32 Pin Ceramic .600" DIP (Package 300)
- CL = 32 Pin Rectangular Ceramic Leadless Chip Carrier (Package 601)
- DE = 32 Lead Ceramic SOJ (Package 101) Evolutionary
- DR = 32 Lead Ceramic SOJ (Package 101) Revolutionary
- F = 36 Lead Ceramic Flat Pack (Package 226)
- FE = 32 Lead Ceramic Flat Pack (Package 220)

DEVICE GRADE: _____

- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

LEAD FINISH: _____

- Blank = Gold plated leads
- A = Solder dip leads

| Device Type | Speed | Package | SMD No. |
|--------------------------|-------|------------------------|------------------|
| 128K x 8 SRAM Monolithic | 55ns | 32 lead SOJ Revol (DR) | 5962-96691 05HUX |
| 128K x 8 SRAM Monolithic | 45ns | 32 lead SOJ Revol (DR) | 5962-96691 06HUX |
| 128K x 8 SRAM Monolithic | 35ns | 32 lead SOJ Revol (DR) | 5962-96691 07HUX |
| 128K x 8 SRAM Monolithic | 25ns | 32 lead SOJ Revol (DR) | 5962-96691 08HUX |
| 128K x 8 SRAM Monolithic | 20ns | 32 lead SOJ Revol (DR) | 5962-96691 09HUX |
| 128K x 8 SRAM Monolithic | 17ns | 32 lead SOJ Revol (DR) | 5962-96691 10HUX |
| 128K x 8 SRAM Monolithic | 15ns | 32 lead SOJ Revol (DR) | 5962-96691 11HUX |
| 128K x 8 SRAM Monolithic | 55ns | 32 lead SOJ Evol (DE) | 5962-96691 05HTX |
| 128K x 8 SRAM Monolithic | 45ns | 32 lead SOJ Evol (DE) | 5962-96691 06HTX |
| 128K x 8 SRAM Monolithic | 35ns | 32 lead SOJ Evol (DE) | 5962-96691 07HTX |
| 128K x 8 SRAM Monolithic | 25ns | 32 lead SOJ Evol (DE) | 5962-96691 08HTX |
| 128K x 8 SRAM Monolithic | 20ns | 32 lead SOJ Evol (DE) | 5962-96691 09HTX |
| 128K x 8 SRAM Monolithic | 17ns | 32 lead SOJ Evol (DE) | 5962-96691 10HTX |
| 128K x 8 SRAM Monolithic | 15ns | 32 lead SOJ Evol (DE) | 5962-96691 11HTX |
| 128K x 8 SRAM Monolithic | 55ns | 32 pin DIP (C) | 5962-96691 05HYX |
| 128K x 8 SRAM Monolithic | 45ns | 32 pin DIP (C) | 5962-96691 06HYX |
| 128K x 8 SRAM Monolithic | 35ns | 32 pin DIP (C) | 5962-96691 07HYX |
| 128K x 8 SRAM Monolithic | 25ns | 32 pin DIP (C) | 5962-96691 08HYX |
| 128K x 8 SRAM Monolithic | 20ns | 32 pin DIP (C) | 5962-96691 09HYX |
| 128K x 8 SRAM Monolithic | 17ns | 32 pin DIP (C) | 5962-96691 10HYX |
| 128K x 8 SRAM Monolithic | 15ns | 32 pin DIP (C) | 5962-96691 11HYX |
| 128K x 8 SRAM Monolithic | 55ns | 36 pin Flatpack (F) | 5962-96691 05HXX |
| 128K x 8 SRAM Monolithic | 45ns | 36 pin Flatpack (F) | 5962-96691 06HXX |
| 128K x 8 SRAM Monolithic | 35ns | 36 pin Flatpack (F) | 5962-96691 07HXX |
| 128K x 8 SRAM Monolithic | 25ns | 36 pin Flatpack (F) | 5962-96691 08HXX |
| 128K x 8 SRAM Monolithic | 20ns | 36 pin Flatpack (F) | 5962-96691 09HXX |
| 128K x 8 SRAM Monolithic | 17ns | 36 pin Flatpack (F) | 5962-96691 10HXX |
| 128K x 8 SRAM Monolithic | 15ns | 36 pin Flatpack (F) | 5962-96691 11HXX |

Document Title

128Kx8 MONOLITHIC SRAM, SMD 5962-96691

Revision History

| Rev # | History | Release Date | Status |
|--------------|---|---------------------|---------------|
| Rev 6 | Changes (Pg. 1-11) 6.1 Change document layout from White Electronic Designs to Microsemi 6.2 Add document Revision History page | March 2011 | Final |
| Rev 7 | Changes (Pg. All) (ECN 10156) 7.1 Change document layout from Microsemi to Mercury Systems | August 2016 | Final |