128Kx32 SRAM MODULE
SMD 5962-93187 & 5962-95595

WS128K32-XXX

FEATURES

- Access Times of 15, 17, 20, 25, 35, 45, 55ns
- MIL-STD-883 Compliant Devices Available
- Packaging
  - 66 pin, PGA Type, 1.075" square, Hermetic Ceramic HIP (Package 400)
  - 68 lead, 40mm CQFP (G4T)[1], 3.56mm (0.140") (Package 502)
  - 68 lead, 22.4mm CQFP (G2U), 3.56mm (0.140"), (Package 510)
  - 68 lead, 22.4mm (0.880") square, CQFP (G2L), 5.08mm (0.200") high, (Package 528)
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight:
  WS128K32-XG2UX - 8 grams typical
  WS128K32-XG2LX - 8 grams typical
  WS128K32-XH1X - 13 grams typical
  WS128K32-XG4TX[1] - 20 grams typical
- Devices are upgradeable to 512Kx32

This product is subject to change without notice.

FIGURE 1 – PIN CONFIGURATION FOR WS128K32N-XH1X

Top View

1	12	23		34	45	56
I/O8	WE2#	I/O15		I/O24	VCC	I/O31
I/O9	CS2#	I/O14		I/O25	CS4#	I/O30
I/O10	GND	I/O13		I/O26	WE4#	I/O29
A13	I/O11	I/O12		A6	I/O27	I/O28
A14	A10	OE#		A7	A3	A0
A15	A11	NC		NC	A4	A1
A16	A12	WE1#		A8	A5	A2
NC	VCC	I/O7		A9	WE3#	I/O23
I/O0	CS1#	I/O6		I/O16	CS3#	I/O22
I/O1	NC	I/O5		I/O17	GND	I/O21
I/O2	I/O3	I/O4		I/O18	I/O19	I/O20
11	22	33		44	55	66

Pin Description

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
WE1-4#	Write Enables
CS1-4#	Chip Selects
OE#	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

Block Diagram

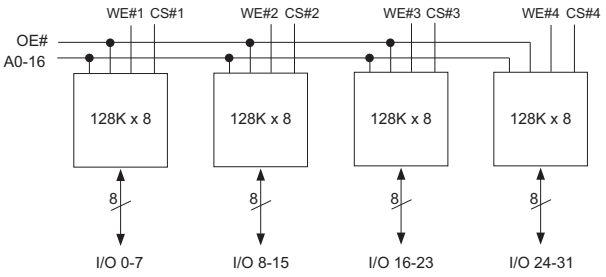
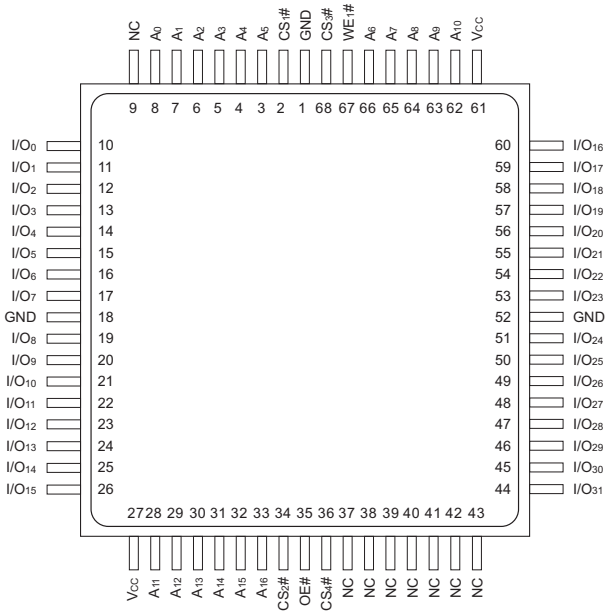


FIGURE 2 – PIN CONFIGURATION FOR WS128K32-XG4TX[1]

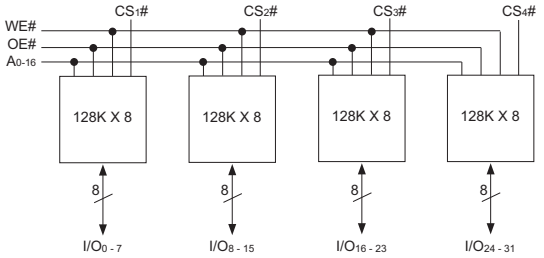
Top View



Pin Description

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
WE1-4#	Write Enables
CS1-4#	Chip Selects
OE#	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

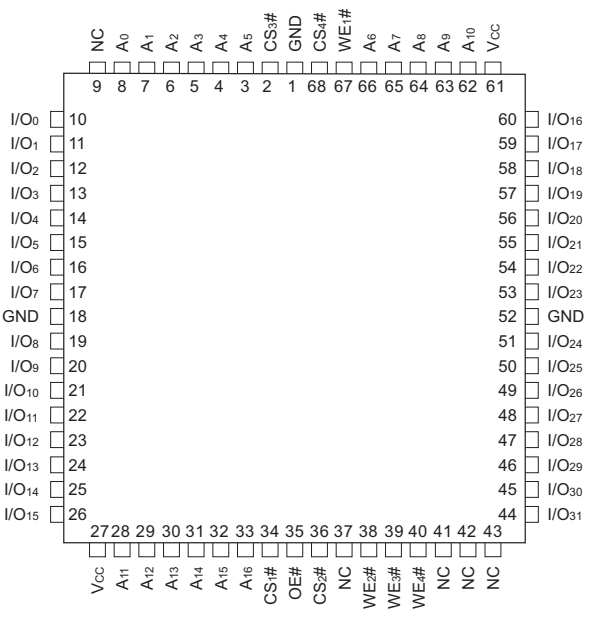
Block Diagram



Note 1: Package Not Recommended For New Design

FIGURE 3 – PIN CONFIGURATION FOR WS128K32-XG2UX AND WS128K32-XG2LX

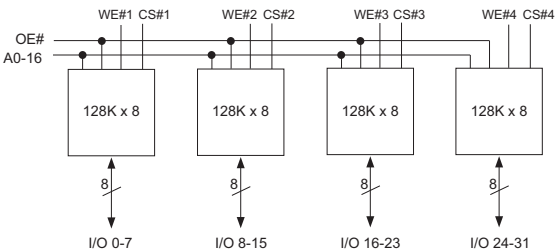
Top View



Pin Description

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
WE1-4#	Write Enables
CS1-4#	Chip Selects
OE#	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

Block Diagram



Note 1: Package Not Recommended For New Design

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	V_{CC}+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp (Mil)	T_A	-55	+125	°C

TRUTH TABLE

CS	OE	WE	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C_{OE}	V_{IN} = 0V, f = 1.0 MHz	50	pF
WE_{1-4}# capacitance	C_{WE}	V_{IN} = 0V, f = 1.0 MHz		pF
HIP (PGA) H1			20	
CQFP G4T			50	
CQFP G2U/G2L			20	
CS_{1-4}# capacitance	C_{CS}	V_{IN} = 0V, f = 1.0 MHz	20	pF
Data# I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Sym	Conditions	-15		-17		-20		-25		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10		10		10		10	µA
Output Leakage Current	I_{LO}	CS# = V_{IH}, OE# = V_{IH}, V_{OUT} = GND to V_{CC}		10		10		10		10	µA
Operating Supply Current	I_{CC}	CS# = V_{IL}, OE# = V_{IH}, f = 5MHz, V_{CC} = 5.5		600		600		600		600	mA
Standby Current	I_{SB}	CS# = V_{IH}, OE# = V_{IH}, f = 5MHz, V_{CC} = 5.5		80		80		80		60	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = 4.5		0.4		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = 4.5	2.4		2.4		2.4		2.4		V

Parameter	Sym	Conditions	-35		-45		-55		Units
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10		10		10	µA
Output Leakage Current	I_{LO}	CS# = V_{IH}, OE# = V_{IH}, V_{OUT} = GND to V_{CC}		10		10		10	µA
Operating Supply Current	I_{CC}	CS# = V_{IL}, OE# = V_{IH}, f = 5MHz, V_{CC} = 5.5		600		600		600	mA
Standby Current	I_{SB}	CS# = V_{IH}, OE# = V_{IH}, f = 5MHz, V_{CC} = 5.5		60		60		60	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = 4.5		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = 4.5	2.4		2.4		2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS (For WS128K32L-XXX Only)

-55°C ≤ T_A ≤ +125°C, -40°C ≤ T_A ≤ +85°C

Characteristic	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage	V_{CC}	V_{CC} = 2.0V	2	-	-	V
Data Retention Quiescent Current	I_{CCDR}	CS ³ V_{CC} -0.2V	-	1	2	mA
Chip Disable to Data Retention Time (1)	T_{CDR}	V_{IN} ³ V_{CC} -0.2V	0	-	-	ns
Operation Recovery Time (1)	T_R	or V_{IN} 0.2V	TRC		-	ns

NOTE: Parameter guaranteed, but not tested.

AC CHARACTERISTICS

V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter Read Cycle	Symbol	-15		-17		-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		17		20		25		35		45		55		ns
Address Access Time	t_{AA}		15		17		20		25		35		45		55	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		0		0		0		ns
Chip Select Access Time	t_{ACS}		15		17		20		25		35		45		55	ns
Output Enable to Output Valid	t_{OE}		10		10		12		15		20		25		30	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	3		3		3		3		3		3		3		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		12		12		12		12		15		20		20	ns
Output Disable to Output in High Z	t_{OHZ}[1]		12		12		12		12		15		20		20	ns

1. This parameter is guaranteed by design but not tested.

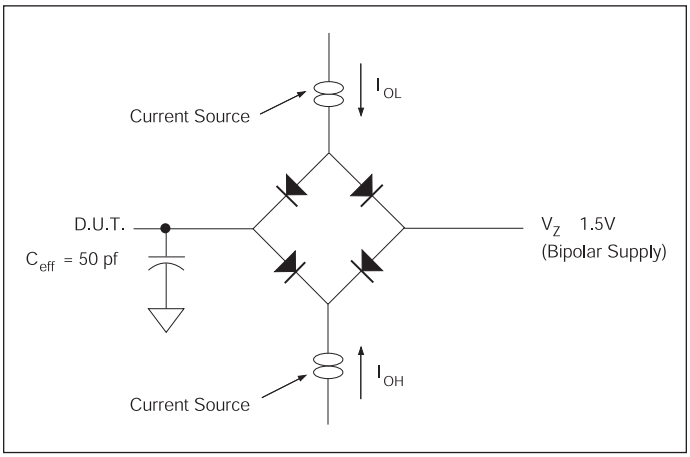
AC CHARACTERISTICS

V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter Write Cycle	Symbol	-15		-17		-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		17		20		25		35		45		55		ns
Chip Select to End of Write	t_{CW}	14		14		15		20		25		30		45		ns
Address Valid to End of Write	t_{AW}	14		15		15		20		25		30		45		ns
Data Valid to End of Write	t_{DW}	10		10		12		15		20		25		25		ns
Write Pulse Width	t_{WP}	14		14		15		20		25		30		45		ns
Address Setup Time	t_{AS}	0		0		0		0		0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		0		0		0		0		ns
Output Active from End of Write	t_{OW}[1]	3		3		3		3		4		4		4		ns
Write Enable to Output in High Z	t_{WHZ}[1]		10		10		12		15		20		25		25	ns
Data Hold Time	t_{DH}	0		0		0		0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

FIGURE. 4 – AC TEST CIRCUIT



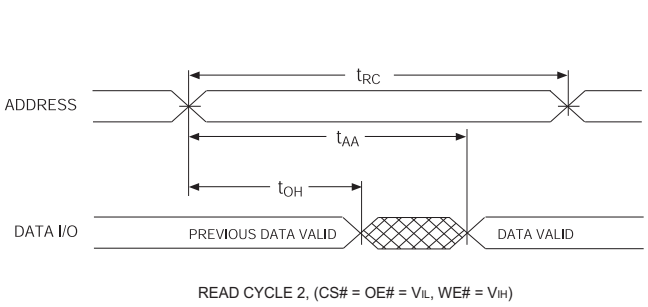
AC Test Conditions

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

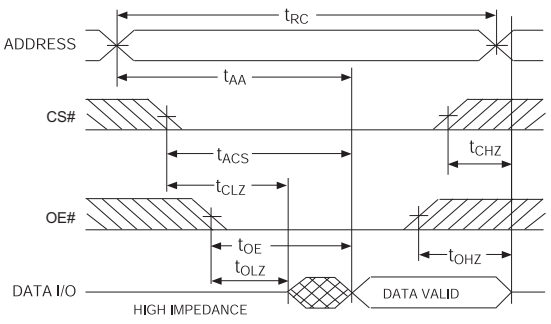
Notes:

V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIGURE 5 – TIMING WAVEFORM - READ CYCLE

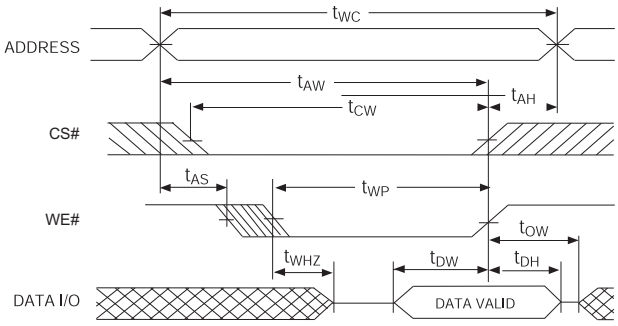


READ CYCLE 2, (CS# = OE# = V_{IL}, WE# = V_{IH})



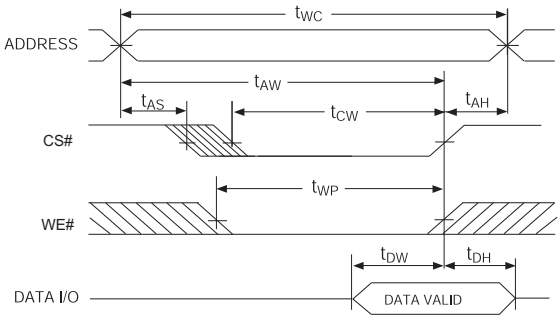
READ CYCLE 2 (WE# = V_{IH})

FIGURE 6 – WRITE CYCLE - WE# CONTROLLED



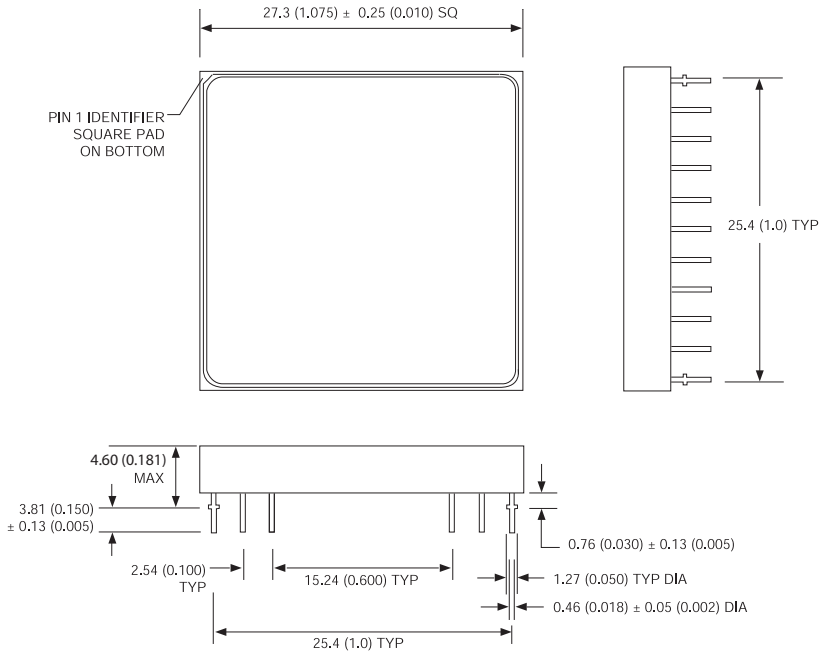
WRITE CYCLE 2, CS# CONTROLLED

FIGURE 7 – WRITE CYCLE - CS# CONTROLLED



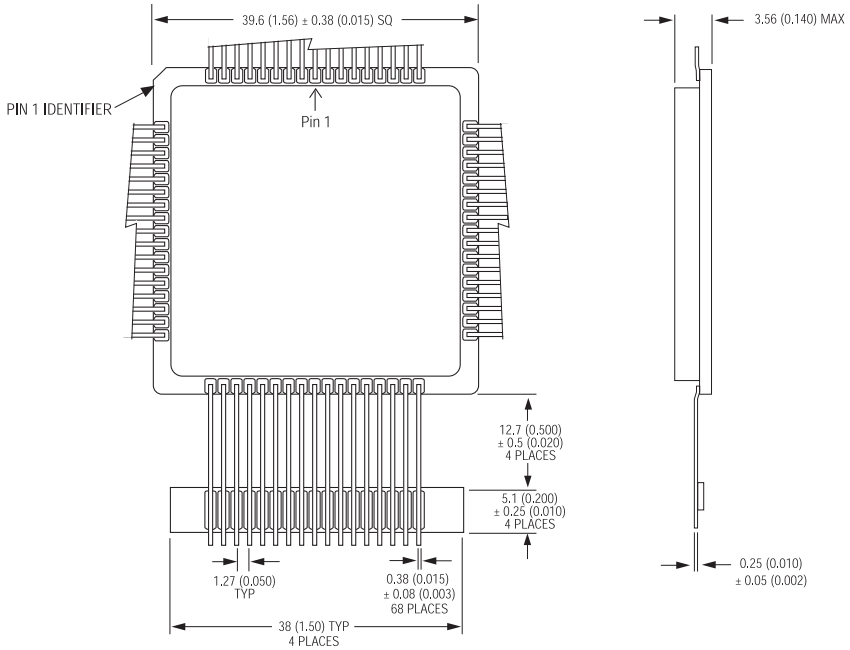
WRITE CYCLE 2, CS# CONTROLLED

PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

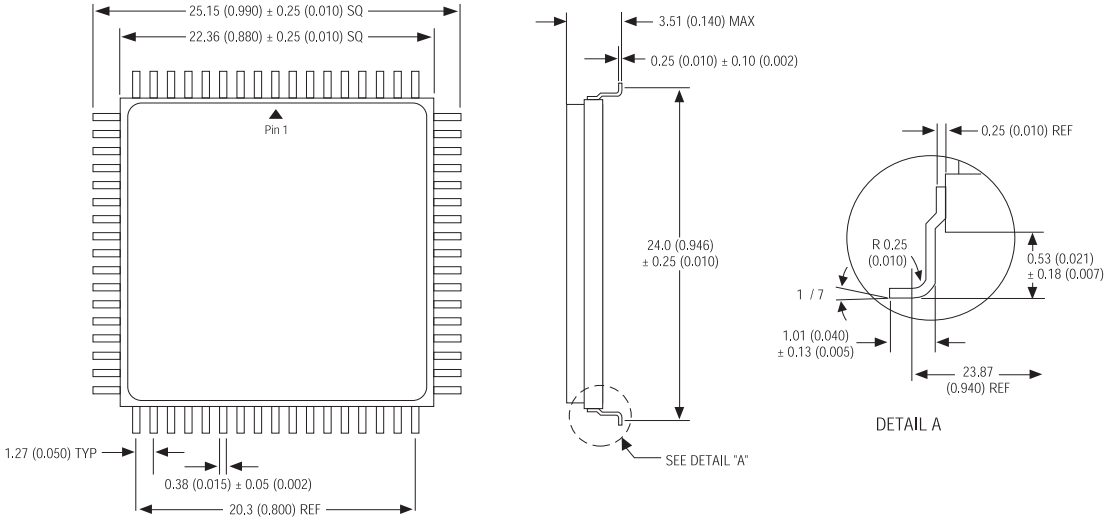
PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)[1]



Note 1: Package Not Recommended For New Design

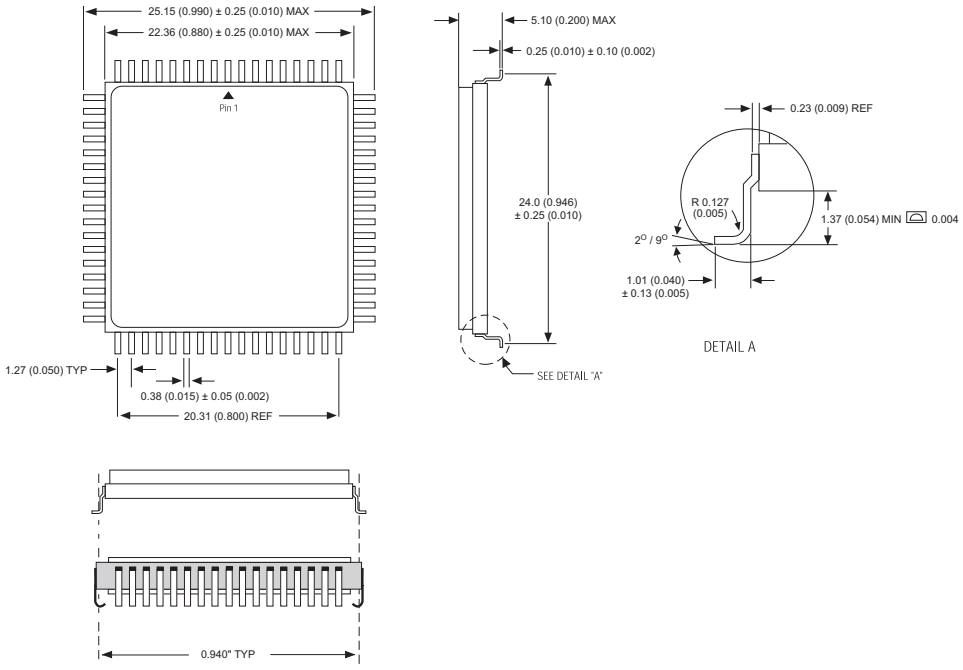
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 510: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2U)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 528: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2L)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W S 128K32 X - XXX X X X

MERCURY SYSTEMS

SRAM

ORGANIZATION, 128Kx32
User configurable as 256Kx16 or 512Kx8

IMPROVEMENT MARK:
N = No Connect at pin 8, 21, 28 and 39 in HIP for Upgrades
L = Low Power*

ACCESS TIME (ns)

PACKAGE TYPE:
H1 = 1.075" sq. Ceramic Hex-In-line Package, HIP (Package 400)
G2U = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 510)
G2L = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 528)
G4T** = 40 mm Low Profile CQFP (Package 502)

DEVICE GRADE:
Q = Military Grade***
M = Military Screened -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0°C to +70°C

LEAD FINISH:
Blank = Gold plated leads
A = Solder dip leads

* Package Not Recommended For New Designs
** Low Power Data Retention only available in G2U, G2L, PackageTypes
*** This product is processed the same as the 5962-XXXXXHXX product but all test and mechanical requirements are per the Mercury Systems data sheet.

DEVICE TYPE	SPEED	PACKAGE	SMD NO.
128K x 32 SRAM Module	55ns	66 pin HIP (H1)	5962-93187 05H4X
128K x 32 SRAM Module	45ns	66 pin HIP (H1)	5962-93187 06H4X
128K x 32 SRAM Module	35ns	66 pin HIP (H1)	5962-93187 07H4X
128K x 32 SRAM Module	25ns	66 pin HIP (H1)	5962-93187 08H4X
128K x 32 SRAM Module	20ns	66 pin HIP (H1)	5962-93187 09H4X
128K x 32 SRAM Module	17ns	66 pin HIP (H1)	5962-93187 10H4X
128K x 32 SRAM Module	15ns	66 pin HIP (H1)	5962-93187 11H4X
128K x 32 SRAM Module	55ns	68 lead CQFP Low Profile (G4T)[1]	5962-95595 05HYX[1]
128K x 32 SRAM Module	45ns	68 lead CQFP Low Profile (G4T)[1]	5962-95595 06HYX[1]
128K x 32 SRAM Module	35ns	68 lead CQFP Low Profile (G4T)[1]	5962-95595 07HYX[1]
128K x 32 SRAM Module	25ns	68 lead CQFP Low Profile (G4T)[1]	5962-95595 08HYX[1]
128K x 32 SRAM Module	20ns	68 lead CQFP Low Profile (G4T)[1]	5962-95595 09HYX[1]
128K x 32 SRAM Module	17ns	68 lead CQFP Low Profile (G4T)[1]	5962-95595 10HYX[1]
128K x 32 SRAM Module	15ns	68 lead CQFP Low Profile (G4T)[1]	5962-95595 11HYX[1]
128K x 32 SRAM Module	55ns	68 lead CQFP/J (G2U)	5962-95595 05HMX
128K x 32 SRAM Module	45ns	68 lead CQFP/J (G2U)	5962-95595 06HMX
128K x 32 SRAM Module	35ns	68 lead CQFP/J (G2U)	5962-95595 07HMX
128K x 32 SRAM Module	25ns	68 lead CQFP/J (G2U)	5962-95595 08HMX
128K x 32 SRAM Module	20ns	68 lead CQFP/J (G2U)	5962-95595 09HMX
128K x 32 SRAM Module	17ns	68 lead CQFP/J (G2U)	5962-95595 10HMX
128K x 32 SRAM Module	15ns	68 lead CQFP/J (G2U)	5962-95595 11HMX
128K x 32 SRAM Module	55ns	68 lead CQFP/J (G2L)	5962-95595 05HAX
128K x 32 SRAM Module	45ns	68 lead CQFP/J(G2L)	5962-95595 06HAX
128K x 32 SRAM Module	35ns	68 lead CQFP/J(G2L)	5962-95595 07HAX
128K x 32 SRAM Module	25ns	68 lead CQFP/J(G2L)	5962-95595 08HAX
128K x 32 SRAM Module	20ns	68 lead CQFP/J(G2L)	5962-95595 09HAX
128K x 32 SRAM Module	17ns	68 lead CQFP/J(G2L)	5962-95595 10HAX
128K x 32 SRAM Module	15ns	68 lead CQFP/J(G2L)	5962-95595 11HAX

Note 1: Package Not Recommended For New Design

Document Title

128Kx32 SRAM MODULE, SMD 5962-93187

Revision History

Rev #	History	Release Date	Status
Rev 18	Changes (Pg. 1-10) 18.1 Change document layout from White Electronic Designs to Microsemi 18.2 Add document Revision History page	May 2011	Final
Rev 19	Change (Pg. 8) 19.1 Changed Device Grade "Q" description from "MIL-STD-883 Compliant" to "MIL-PRF-38534 Class H Compliant."	May 2014	Final
Rev 20	Change (Pg. 8) 20.1 Changed Device Grade "Q" description from "MIL-PRF-38534 Class H Compliant." to "Military Grade."	August 2014	Final
Rev 21	Changes (Pg. All) (ECN 10156) 21.1 Change document layout from Microsemi to Mercury Systems	August 2016	Final