

512Kx32 SRAM 3.3V Multichip Package



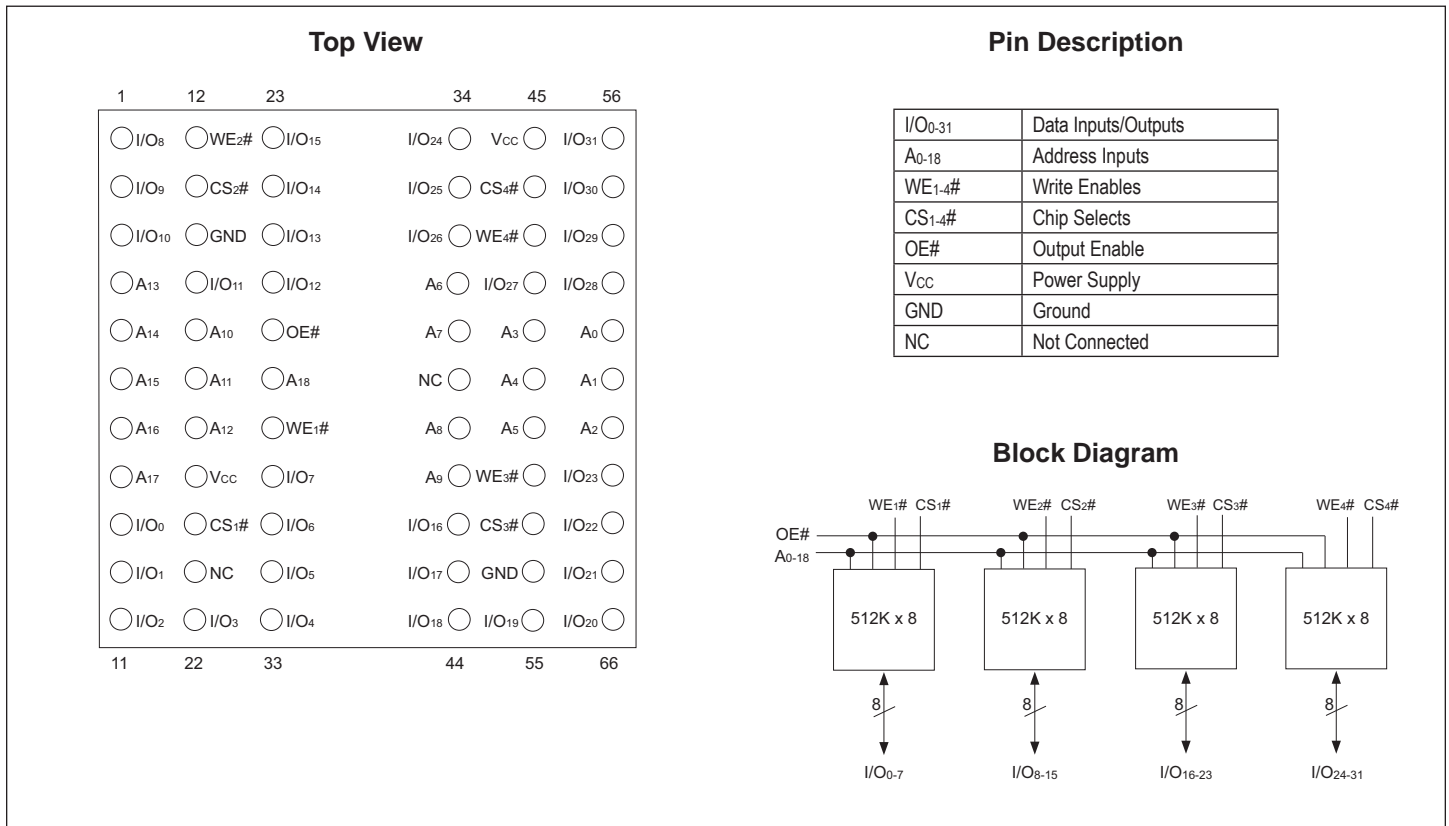
WS512K32V-XXX

FEATURES

- Access Times of 15, 17, 20ns
- Low Voltage Operation
- Packaging
 - 66-pin, PGA Type, 1.075 inch square, Hermetic Ceramic HIP (Package 400)
 - 8 lead, 22.4mm (0.880 inch) CQFP, (G2U), 3.56mm (0.140"), (Package 510)
- Organized as 512Kx32; User Configurable as 2x512Kx16 or 4x512Kx8
- Commercial, Industrial and Military Temperature Ranges
- Low Voltage Operation:
 - 3.3V ± 10% Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Fully Static Operation:
 - No clock or refresh required.
- Three State Output.
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
 - WS512K32V-XG2UX - 8 grams typical
 - WS512K32NV-XH1X - 13 grams typical

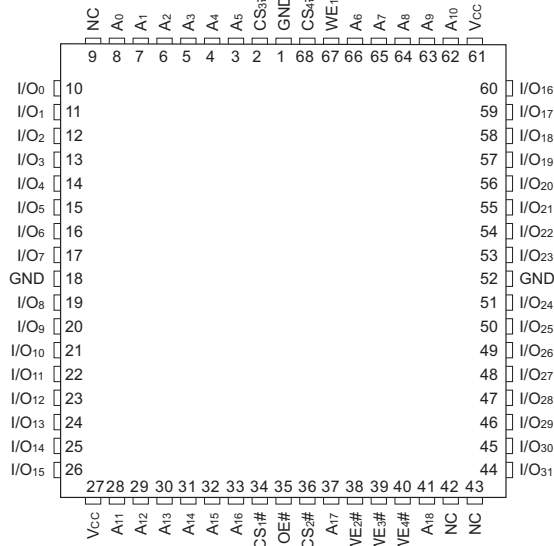
* This product is subject to change without notice.

PIN CONFIGURATION FOR WS512K32NV-XH1X



PIN CONFIGURATION FOR WS512K32V-XG2UX

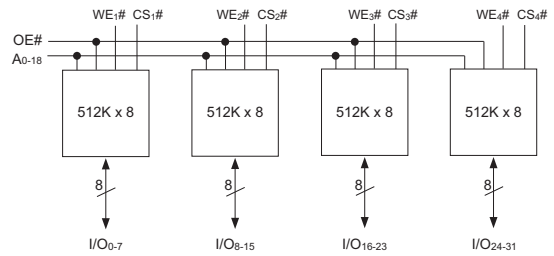
Top View



Pin Description

I/O ₀₋₃₁	Data Inputs/Outputs
A ₀₋₁₈	Address Inputs
WE _{1-4#}	Write Enables
CS _{1-4#}	Chip Selects
OE#	Output Enable
V _{CC}	Power Supply
GND	Ground
NC	Not Connected

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	4.6	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	4.6	V

TRUTH TABLE

CS	OE	WE	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	3.0	3.6	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C _{OE}	V _{IN} = 0V, f = 1.0 MHz	50	pF
WE ₁₋₄ # capacitance HIP (PGA) CQFP G2U	C _{WE}	V _{IN} = 0V, f = 1.0 MHz	20	pF
CS ₁₋₄ # capacitance	C _{CS}	V _{IN} = 0V, f = 1.0 MHz	20	pF
Data# I/O capacitance	C _{I/O}	V _{I/O} = 0V, f = 1.0 MHz	20	pF
Address input capacitance	C _{AD}	V _{IN} = 0V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

V_{CC} = 3.3V ± 0.3V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I _{LI}	V _{IN} = GND to V _{CC}		10	µA
Output Leakage Current	I _{LO}	CS# = V _{IH} , OE# = V _{IH} , V _{OUT} = GND to V _{CC}		10	µA
Operating Supply Current	I _{CC} x 32	CS# = V _{IL} , OE# = V _{IH} , f = 5MHz, V _{CC} = 3.6		400	mA
Standby Current	I _{SB}	CS# = V _{IH} , OE# = V _{IH} , f = 5MHz, V _{CC} = 3.6		200	mA
Output Low Voltage	V _{OL}	I _{OL} = 4.0mA		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V.
Contact factory for low power option.

AC CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	15		17		20		ns
Address Access Time	t _{AA}		15		17		20	ns
Output Hold from Address Change	t _{OH}	0		0		0		ns
Chip Select Access Time	t _{ACS}		15		17		20	ns
Output Enable to Output Valid	t _{OE}		8		8		10	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	1		1		1		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	0		0		0		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		8		8		10	ns
Output Disable to Output in High Z	t _{OHZ} ¹		8		8		10	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	15		17		20		ns
Chip Select to End of Write	t _{CW}	12		12		14		ns
Address Valid to End of Write	t _{AW}	12		12		14		ns
Data Valid to End of Write	t _{DW}	9		9		10		ns
Write Pulse Width	t _{WP}	12		14		14		ns
Address Setup Time	t _{AS}	0		0		0		ns
Address Hold Time	t _{AH}	0		0		0		ns
Output Active from End of Write	t _{OW} ¹	2		3		3		ns
Write Enable to Output in High Z	t _{WHZ} ¹		8		8		9	ns
Data Hold Time	t _{DH}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT

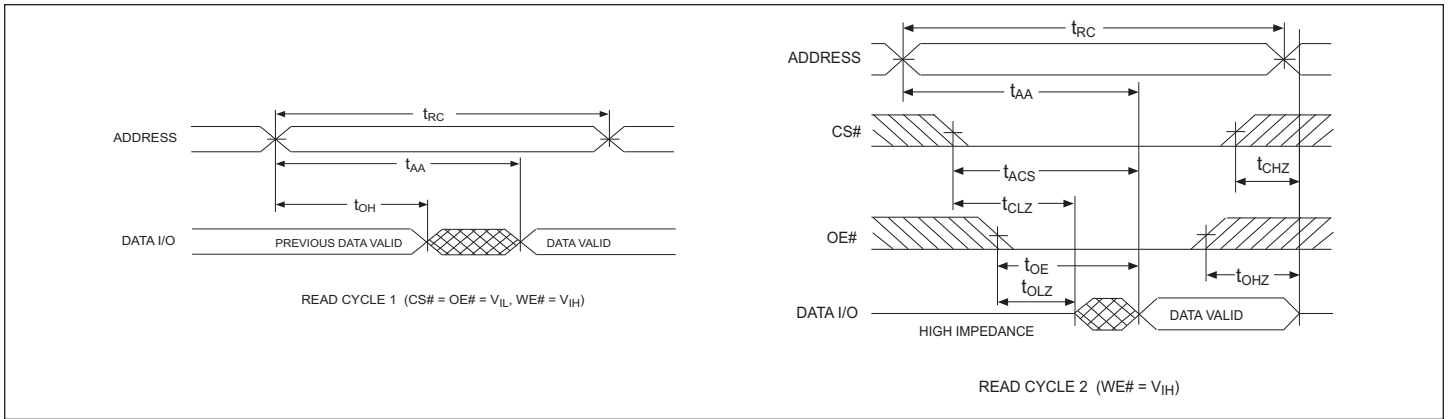
V_Z = 1.5V
(Bipolar Supply)

AC Test Conditions

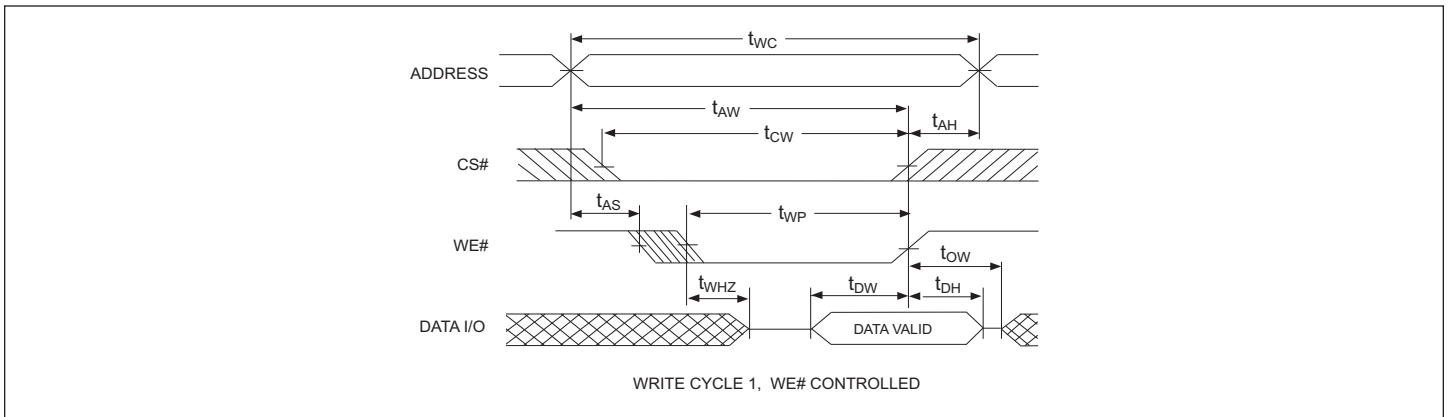
Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:
 V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
 Tester Impedance Z₀ = 75 Ω.
 V_Z is typically the midpoint of V_{OH} and V_{OL}.
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.

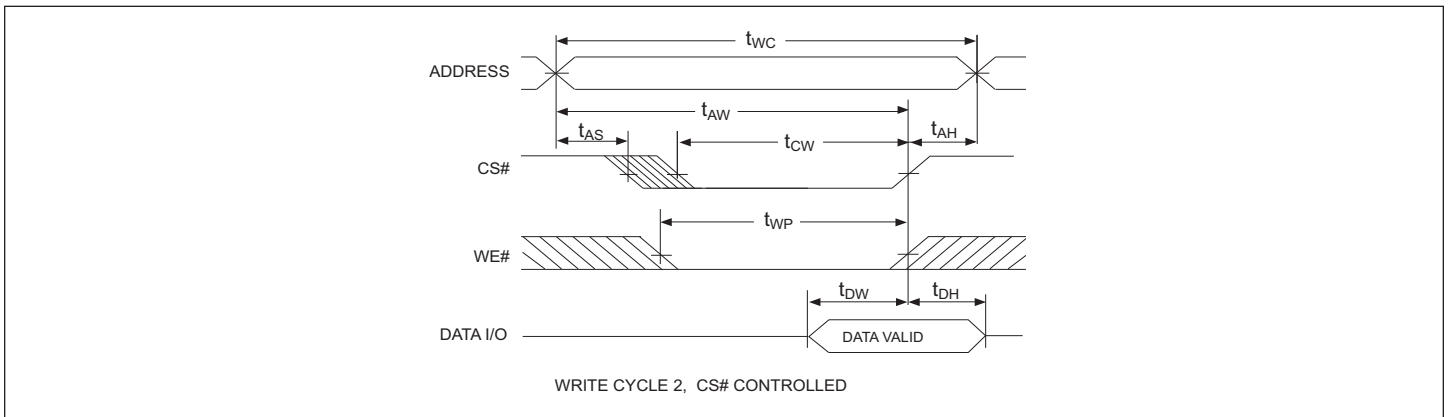
TIMING WAVEFORM – READ CYCLE



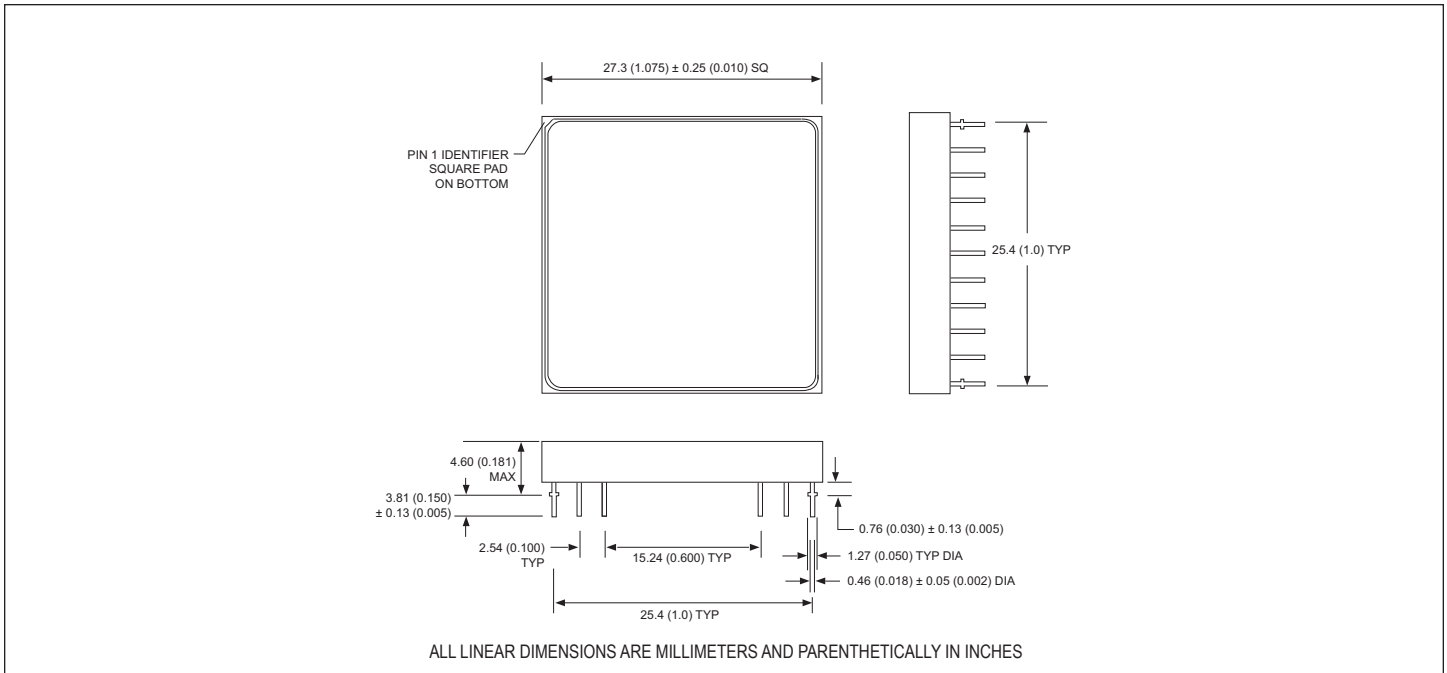
WRITE CYCLE – WE# CONTROLLED



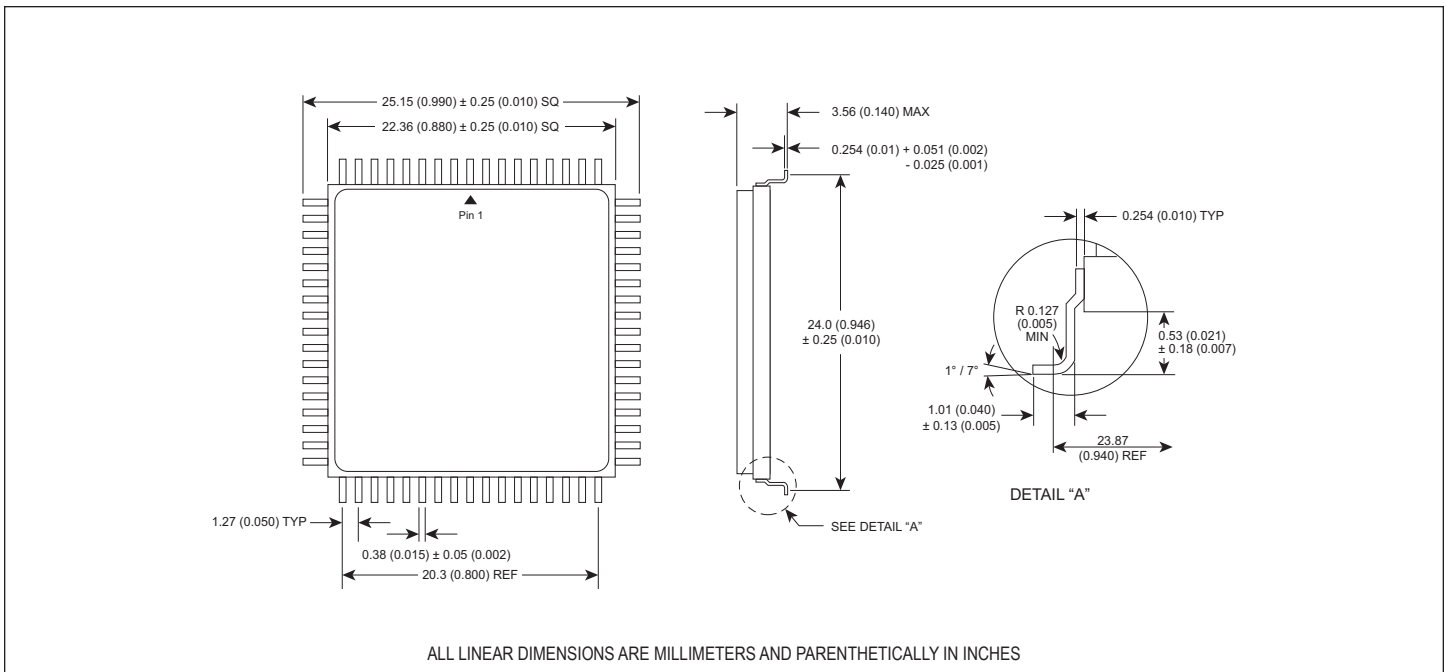
WRITE CYCLE – CS# CONTROLLED



PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



PACKAGE 510: 68 LEAD, LOW PROFILE CERAMIC QUAD FLAT PACK, CQFP (G2U)



ORDERING INFORMATION

W S 512K 32 X V - XXX X X X

MERCURY SYSTEMS

SRAM

ORGANIZATION, 512Kx32

User configurable as 2x512Kx16 or 4x512Kx8

IMPROVEMENT MARK:

N = No Connect at pin 21 and 39 in HIP for Upgrades (H1 only)

Low Voltage Supply 3.3V ± 10%

ACCESS TIME (ns)

PACKAGE TYPE:

H1 = 1.075" sq. Ceramic Hex In Line Package, HIP (Package 400)
G2U = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 510)

DEVICE GRADE:

M = Military -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0°C to +70°C

LEAD FINISH:

Blank = Gold plated leads
A = Solder dip leads

Document Title

512Kx32 SRAM 3.3V MULTICHIP PACKAGE

Revision History

Rev #	History	Release Date	Status
Rev 14	Changes (Pg. 6) (ECN 9936) 14.1 Add document Revision History page 14.2 Update package dimensions	April 2016	Final
Rev 15	Changes (Pg. All) (ECN 10156) 15.1 Change document layout from Microsemi to Mercury Systems	August 2016	Final